This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TWC.2020.3040226, IEEE Transactions on Wireless Communications

Full-Duplexing with SDR Devices: Algorithms, FPGA Implementation and Real-Time Results

Lauri Anttila, *Member, IEEE,* Vesa Lampu, Seyed Ali Hassani, *Student Member, IEEE,* Pablo Pascual Campo, *Student Member, IEEE,* Dani Korpi, *Member, IEEE,* Matias Turunen, Sofie Pollin, *Senior Member, IEEE,* and Mikko Valkama, *Senior Member, IEEE*

***Abstract*—In this paper, we present a novel nonlinear digital self-interference canceller algorithm, its implementation details on a software-defined radio (SDR) platform, and performance results of real-time full-duplex experiments on both device and link level. The canceller algorithm is based on an augmented Hammerstein model, with a nonlinear part modeling the transmitter non-idealities followed by a linear filter to model the self-interference (SI) channel. The nonlinear part includes a spline-based model for the nonlinear power amplifier, a polynomial model for baseband nonlinearities, as well as models for I/Q mismatch and LO leakage. The canceller is implemented on an FPGA as a part of an OFDM transceiver testbed for real-time measurements. Extensive real-time measurements show excellent performance: (1) the digital canceller, together with an RF isolator, can suppress the SI to within 1-2 dB's of the receiver noise floor, with total SI suppression of up to 103 dB; (2) digital cancellation of up to 46 dB is evidenced, which is among the highest real-time cancellations in literature; (3) system-level measurements with OFDM signals demonstrate the benefit of utilizing the proposed canceller in a two-way communication scenario, showing up to 90% increase in sum-rate compared to half-duplex communication.**

***Keywords*—Full-duplex, self-interference cancellation, FPGA implementation, software-defined radio.**

I. Introduction

FULL-duplexing can theoretically double the spectral efficiency of bidirectional communication links, when compared to systems using time-division or frequency-division duplexing, while also facilitating lower latencies and simplified usage of spectral resources [1]–[3]. Recently, full-duplex technology has also been used to enable joint communications and radar, where simultaneous data transmission and environmental sensing within a common radio system is pursued [4]–[6]. Therefore, full-duplex technology is of great interest when designing and building next-generation wireless systems and networks. The recent survey in [3] gives an excellent overview of in-band full-duplex technologies and systems.

The implementation of full-duplex (FD) communications has historically been deemed impossible due to the strong self-interference (SI), i.e., the transmit signal leakage to the simultaneously operating receiver (RX), which can be 100-120 dB stronger than the weak received signal, thus saturating the receiver [1], [2]. SI cancellation technology is therefore key to the adoption of FD. Typically, the suppression of the SI needs to be done in several stages, in various domains, as is shown in Fig. 1 [1]. The propagation-domain suppression techniques are passive in nature, and refer to using antenna designs or related beamforming algorithms, or an isolator such as a circulator or electrical balance duplexer, to attenuate the propagation of the SI signal to the receiver antenna(s). Active analog cancellation is the next line of defense, implemented usually at the receiver low-noise amplifier (LNA) input, or if the radio frequency (RF) front-end can tolerate the impinging self-interference, it can also be implemented at intermediate frequency (IF)/baseband before the analog-to-digital conversion [7]. Two main types of analog cancellers have been proposed, one which taps the power amplifier (PA) signal and modifies its amplitude and phase to cancel the SI [8]–[10], and the other type where the cancellation signal is generated in the digital domain and converted to proper analog form through an auxiliary transmitter (TX) [11], [12]. The last stage of SI cancellation is digital, and its aim is to clean the remaining SI from the received signal, and in the best case, to push it below the noise floor. The remainder of this paper focuses on digital cancellation algorithm design and implementation, while in the experiments, two different RF isolation/cancellation solutions are considered.

The cancellation of the SI may seem like a simple matter, since the own TX signal is known. However, first of all, there is significant frequency and time selectivity in the observed SI, caused by reflections both inside the device and from nearby surroundings, which vary over time. These need to be taken into account, and in digital cancellation solutions, this is typically achieved through adaptive finite impulse

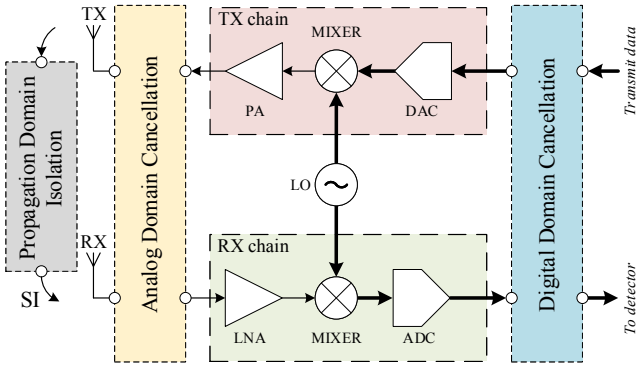


Fig. 1. Simplified model of a full-duplex transceiver system with the relevant sources of distortion and forms of SI cancellation shown.

Manuscript received April 03, 2020; revised August 31, 2020; accepted November 09, 2020.

This work was supported by the European Union's Horizon 2020 research and innovation program under grant agreement No. 732174 (ORCA, Extension #4) and by the Academy of Finland under the project 301820.

L. Anttila, V. Lampu, P. Pascual Campo, M. Turunen and M. Valkama are with the Department of Electrical Engineering, Tampere University, Tampere, Finland. e-mail: lauri.anttila@tuni.fi

S.A. Hassani and S. Pollin are with the Department of Electrical Engineering, KU Leuven, Belgium.

D. Korpi was with the Department of Electrical Engineering, Tampere University. Currently, he is with Nokia Bell Labs, Espoo, Finland.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TWC.2020.3040226, IEEE Transactions on Wireless Communications

response (FIR) filters. Second, under hardware impairments such as power amplifier and baseband nonlinearities and in-phase/quadrature (I/Q) mismatch, the induced distortions can strongly contribute to the observed SI, making purely linear cancellation insufficient [8], [13]–[15]. Therefore, digital cancellation solutions in real-world devices need to model the relevant hardware impairments, in addition to the linear SI channel, in order to reach sufficient cancellation accuracy. The transmitter PA nonlinearity and I/Q mismatch are generally considered the most significant impairments [13]–[15], under the assumption that RF domain isolation is sufficient to protect the receiver from saturation. On some platforms, also the transmitter baseband nonlinearities may limit the performance [16].

Digital cancellation algorithms accounting for these impairments have been proposed in earlier literature [8], [15]–[26]. The works in [8], [17], [26] focused on the power amplifier induced nonlinear distortion and its digital cancellation; [20]–[22] opted to linearize the PA with digital predistortion, and utilized simpler SI models in digital cancellation; in [18], [19], receiver LNA distortions were considered; [15], [27] studied the effects of I/Q mismatches on both TX and RX sides, and proposed cancellation algorithms for them. Some works have also considered multiple impairments [16], [23]–[25]. In [24], the authors considered receiver LNA and baseband nonlinearities, as well as PA nonlinearities, in a full-duplex multiple-input multiple-output (FD-MIMO) system. However, only 3rd order polynomial models were considered. In [23], I/Q imbalances and PA nonlinearities of the transmitter were modelled with a general polynomial formalism, in an FD-MIMO system context with antenna crosstalk; however, the complexity of the proposed linear-in-parameters models was very high. In [16], I/Q imbalances of the transmitter and receiver, as well as baseband nonlinearities of the transmitter, were considered in SI cancellation. A neural network based model was proposed in [25], along with a field-programmable gate array (FPGA) implementation of the prediction part of the model. This model can effectively account for arbitrary nonlinearities in the SI signal, but is plagued by a high learning/fitting complexity, which is generally unsuitable for real-time implementation. Besides [23], [25], there are no fully digital canceller models which can model all the relevant impairments of a direct-conversion transmitter: baseband nonlinearity, I/Q mismatch, and PA nonlinearity.

In recent years, several research groups have demonstrated the feasibility of full-duplex technology experimentally, see, e.g., [8], [11], [28], [29]. Most of the published experimental works, however, have relied on offline digital self-interference cancellation on a host computer, and only few truly real-time implementations exist [3]. The only real-time implementations published so far, where actual real-time experiments are conducted, are, to the authors' knowledge, [29]–[33]. Out of these, nonlinear digital SI cancellation has been implemented only in [31]. These papers will be discussed in more details in Section V-A.

The main contributions and novelties of this work are summarized below.

- We propose a low-complexity adaptive digital SI cancellation solution capable of cancelling distortions induced by the power amplifier, the baseband nonlinearities, the I/Q mismatch, and the local oscillator (LO) leakage of the TX.
- We present implementation details of the algorithm on an FPGA, showing that efficient realization of the algorithm is possible on FPGA.
- We present real-time cancellation performance results with the implemented canceller, obtaining up to 46 dB of digital cancellation and up to 103 dB of total isolation, both of which are record numbers for real-time implementations of nonlinear FD systems.
- We illustrate the FD gains through real-time bidirectional link level measurements, obtaining up to 90 % increase in the sum-rate.

Altogether, this work demonstrates that overall real-time isolation numbers exceeding 100 dB can be achieved in nonlinear SDR devices with limited computational resources.

The remainder of this paper is organized as follows. Section II introduces models for the most prevalent impairments of direct-conversion transmitters and shows an analysis of the impairments of the prototype platform using measured data. In Section III, a novel digital SI canceller algorithm is proposed, based on the analysis in Section II. Gradient-based learning rules for the parameter updates are also shown here. Section IV introduces the prototype testbed and canceller real-time FPGA implementation related details. Section V presents real-time experimentation of the implemented canceller, including SI suppression and link-level performance results. Finally, Section VI concludes the paper.

Mathematical Notation

This paper adopts complex-valued baseband system modeling. Time-dependent variables are expressed as lowercase italic letters with a generic index, e.g. $z[n]$. Vectors and matrices are presented by boldfaced letters, in lowercase and in uppercase, respectively, e.g. $\mathbf{v} \in \mathbb{C}^{L\times 1}$ and $\mathbf{M} \in \mathbb{C}^{L\times W}$. Time-dependency is marked by an index subscript, e.g. $\mathbf{M}_n$. Transpose, Hermitian transpose and complex conjugate operators are denoted as $(\cdot)^T$, $(\cdot)^H$ and $(\cdot)^*$, respectively.

II. Modelling and Analysis of Direct-Conversion Transmitter Impairments

In this section, we carry out modelling of the main impairments of direct-conversion transmitters, and analyze the self-interference measured from an FD testbed implemented on the Universal Software Radio Peripheral (USRP) platform using these models. Fig. 1 showed a simplified FD transceiver utilizing direct-conversion architecture. We make two assumptions about the system: (1) the TX-RX isolation is sufficient, such that the RX nonlinearities are not excited, and (2) the RX I/Q mismatch is calibrated or digitally compensated, for example using the techniques in [34]. These allow us to focus on the transmitter side impairments, which are more difficult to pre-calibrate or compensate.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TWC.2020.3040226, IEEE Transactions on Wireless Communications

A. TX Impairment Models

The direct-conversion transmitter is known to suffer mainly from the following types of impairments:

- *PA nonlinearity*; power amplifiers exhibit nonlinearity when power-efficient operation (near saturation) is sought
- *I/Q image*; due to amplitude and phase mismatches between I and Q branches
- *Baseband nonlinearity*; stemming from nonlinearities in digital-to-analog converters (DACs) and baseband amplification stages
- *LO leakage*; the local oscillator signal leaks to the TX output

Power amplifier nonlinearity is typically modelled with complex-valued polynomial based models [35]. With input $x[n]$, the output of a P-th order baseband model is given as

$$s[n] = \sum_{\substack{p=1 \\ p \text{ odd}}}^{P} \alpha_p^{\text{PA}} x[n]|x[n]|^{p-1}, \tag{1}$$

where α_p^{PA} are the polynomial coefficients.

I/Q mismatch refers to amplitude mismatches between I and Q branches, and the phase error in the LO signals of the TX and RX mixers while up- or downconverting with an I/Q mixer [36], [37]. The result of such mismatches is a mirror image of the original signal, which, in a direct-conversion architecture context, occupies the same band as the original signal. LO leakage is another well-known issue in direct-conversion transmitters, manifested as a DC component in the baseband model. The baseband model of the transmitted signal under I/Q mismatch and LO leakage can be expressed as [34]

$$s[n] = g_1 x[n] + g_2 x^*[n] + c_{LO}, \tag{2}$$

where $g_1 = 1/2(1 + g\exp(j\theta))$ and $g_2 = 1/2(1 - g\exp(j\theta))$, with g and θ denoting the amplitude and phase imbalances, and c_{LO} is the LO leakage coefficient.

Baseband components in a direct-conversion TX, such as the digital-to-analog converter (DAC) or any baseband amplification stages, produce nonlinear distortion which may limit FD system performance [16]. In the case of second-order nonlinearity, the I and Q branch signals can be modeled as $s_I[n] = x_I[n] + \alpha_2 x_I[n]^2$ and $s_Q[n] = x_Q[n] + \alpha_2 x_Q[n]^2$, where $x[n] = x_I[n] + jx_Q[n]$ denotes the ideal baseband signal. The complex-valued signal model can then be shown to be of the form [38]

$$\begin{aligned} s[n] &= s_I[n] + js_Q[n] \\ &= x[n] + \frac{1}{2}(1+j)\alpha_2|x[n]|^2 \\ &\quad + \frac{1}{4}(1-j)\alpha_2(x^2[n] + x^{*2}[n]). \end{aligned} \tag{3}$$

Third-order baseband nonlinearity can be modelled as $s_I[n] = x_I[n] + \alpha_3 x_I[n]^3$ and $s_Q[n] = x_Q[n] + \alpha_3 x_Q[n]^3$, yielding the complex-valued model [38]

$$\begin{aligned} s[n] &= s_I[n] + js_Q[n] \\ &= x[n] + \frac{3}{4}\alpha_3|x[n]|^2 x[n] \\ &\quad + \frac{1}{4}\alpha_3 x^{*3}[n]. \end{aligned} \tag{4}$$

Notice that the distortion term $|x[n]|^2 x[n]$ is produced also by the PA model in (1), while the term $x^{*3}[n]$ is unique. When $x[n]$ is a baseband signal, all the nonlinear distortion products in (3) and (4) also appear at baseband, on top of $x[n]$.

Cascaded nonlinearities are also introduced in the TX, but such secondary effects are typically much lower in magnitude compared to the primary ones. However, the two strongest impairments, I/Q mismatch and PA nonlinearity, can in some cases produce cascaded nonlinearities that are significant [23]. The additional basis functions stemming from this, are of the form $|x[n]|^{(p-1)}x^*[n], p = 3, 5, ...$, with the third order term being the strongest.

B. TX Impairment Analysis With Measured Data

We carry out an analysis of the relative magnitudes of the different impairments, using measured data from a USRP based prototype platform. The transmitter is operated in zero-IF mode, whereas the receiver is operated in low-IF mode to circumvent the RX I/Q imbalance problem. The transmit power is set to 16 dBm. The platform is the same as that used in Section IV, except here the RF output of the USRP is connected directly to the RF input of the device through a 40 dB attenuator (to avoid receiver saturation). These settings allow to analyze the transmitter impairments in isolation, without the effects of receiver impairments or the SI coupling channel. This analysis will give information about the relevant impairments that need to be taken into account in the digital canceller development.

The following model combinations, with their respective sets of instantaneous basis functions also shown, were analyzed:

1) Linear model
   $\Lambda = \{x\}$
2) PA model with polynomial orders $p = 3, 5, ..., 11$
   $\Lambda = \{x,\ x|x|^{p-1}\}$
3) PA + I/Q mismatch + LO leakage models
   $\Lambda = \{x,\ x|x|^{p-1},\ x^*,\ 1\}$
4) PA + I/Q + LO + 2nd order baseband nonlinearity
   $\Lambda = \{x,\ x|x|^{p-1},\ x^*,\ 1,\ |x|^2,\ x^2,\ x^{*2}\}$
5) PA + I/Q + LO + 3rd order baseband nonlinearity
   $\Lambda = \{x,\ x|x|^{p-1},\ x^*,\ 1,\ x^{*3}\}$
6) PA + I/Q + LO + cascaded I/Q-PA nonlinearity
   $\Lambda = \{x,\ x|x|^{p-1},\ x^*,\ 1,\ x^*|x|^2\}$

These models were arranged in a parallel Hammerstein type of overall model, as

$$y[n] = \sum_{k=1}^{|\Lambda|} \beta_k[n] \star \lambda_k[n], \tag{5}$$

with $\beta_k[n]$ denoting the unknown filters, $\lambda_k[n]$ the basis functions, $\star$ the convolution operator, and $|\Lambda|$ the cardinality

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TWC.2020.3040226, IEEE Transactions on Wireless Communications

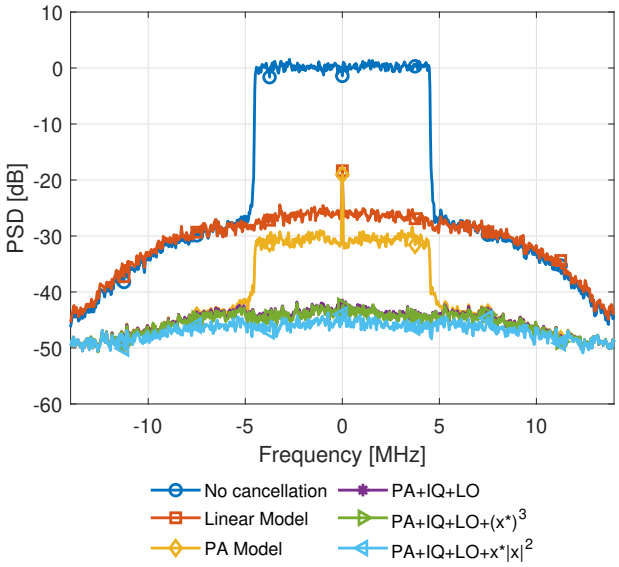


Fig. 2. SI cancellation performance of the considered models.

of the considered set of basis functions. The coefficients were then estimated with the recursive least-squares algorithm [39], with $\lambda = 0.9999$. The error signal of the algorithm, once converged, was extracted for each model combination, and their power spectral densities (PSDs) are shown in Fig. 2. The PSDs are evaluated from 60k instantaneous samples, using the Welch periodogram, with 2048-point Kaiser window with $\beta = 7$, and 50% overlap.

The inclusion of I/Q mismatch and LO leakage to the model clearly brings the most advantage to the cancellation, compared to using PA model only. The baseband distortion models (only the 3rd order case is shown) do not provide any improvement over this model. However, the cascaded I/Q mismatch and PA distortion term $x^*|x|^2$ can be seen to slightly improve the cancellation. Therefore, for the canceller development, we will in this paper consider the additional basis functions $\{x^*, 1, x^*|x|^2\}$, in addition to the linear and PA models. However, the algorithm formulation in the next section is quite general, and allows the inclusion of other basis functions as well, if deemed important in a particular platform.

Finally, we note that the parallel Hammerstein model in (5) could, in principle, be used directly for realizing the canceller, as was indeed done in [40], but with only PA modelling included. However, the computational complexity of this model is prohibitive, as the lengths of the filters $\beta_k[n]$ need to be in the order of the SI channel impulse response, which can be tens of taps. In [40], part of the processing was in fact offloaded to another FPGA, since all the processing could not be fitted on a single FPGA. To simplify the processing, we instead propose a cascaded Hammerstein type model, as described in the next section.

III. Digital Canceller Algorithm

In a Hammerstein system, a nonlinear function is first applied to the input signal $x[n]$, followed by a linear element that generates an output signal $y[n]$. In the context of full-duplex SI cancellation, this model is perfectly suited to model the cascade of a nonlinear transmitter and the linear SI channel. In [26], the theory of spline adaptive filters [41], [42] was utilized to devise the Hammerstein canceller, where a spline-interpolated look-up-table was used to model the PA nonlinearity and a cascaded FIR filter to model the linear SI channel. The novelty in [26] was to generalize the spline adaptive Hammerstein filter theory to complex signals, and to apply the model to SI cancellation. Altogether, the combination of the Hammerstein structure and the simple gradient-based adaptive learning rules results in a cancellation solution that has low complexity in both the signal path (canceller) and in adaption. Compared to earlier memory polynomial based cancellers in [2], [8], this model was shown to reduce the complexity, in terms of the number of real multiplications, by up to 80% [26].

While the Hammerstein canceller in [26] showed favorable SI suppression performance in the presence of PA nonlinear distortion, the model did not consider the additional impairments inherent in direct-conversion transmitter systems, as described in the previous section. To this end, in this article we propose an extended Hammerstein SI model which takes into account these effects, while retaining low processing complexity. For the sake of brevity, we will refer to the basic Hammerstein based digital SI canceller model as DSIC and our proposed extended model as eDSIC.

In the proposed eDSIC model in Fig. 3, the additional impairment models are placed in parallel with the spline-based PA model, the outputs of which will then be summed to produce the input of the linear filter $s[n]$. This model structure has the benefit of using the exact same formulation for the splines and linear filter as presented in [26], while simultaneously retaining relatively simple expressions for the models, which in turn translates to computational simplicity.

A. Self-Interference Models

In this section, we formulate the signal models for the SI canceller blocks in Fig. 3.

1) PA nonlinearity model: From (1), setting $\alpha_1^{PA} = 1$ without loss of generality, the PA model output can be written as

$$\begin{aligned} r[n] &= x[n](1 + \alpha_3^{PA}|x[n]|^2 + \cdots + \alpha_P^{PA}|x[n]|^{P-1}) \\ &= x[n](1 + F(|x[n]|)), \end{aligned} \tag{6}$$

where the function $F(\cdot) = F_I(\cdot) + jF_Q(\cdot)$ is a real-to-complex mapping. Thus, the PA model can be written with two real-valued functions F_I and F_Q. In a device, these can be implemented efficiently with, for example, look-up-tables (LUT). In this work, we choose spline-interpolated LUTs, i.e., tables with a small number of entries and spline interpolation to obtain the intermediate values. Using (6) and the spline interpolation equations introduced in Appendix A, the overall nonlinearity output $r[n]$ can be written as

$$r[n] = x[n](1 + \mathbf{\Psi}_n^T \mathbf{q}_n) \tag{7}$$

with the spline basis functions $\mathbf{\Psi}_n$ and the spline control points $\mathbf{q_n}$ defined in Appendix A.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TWC.2020.3040226, IEEE Transactions on Wireless Communications

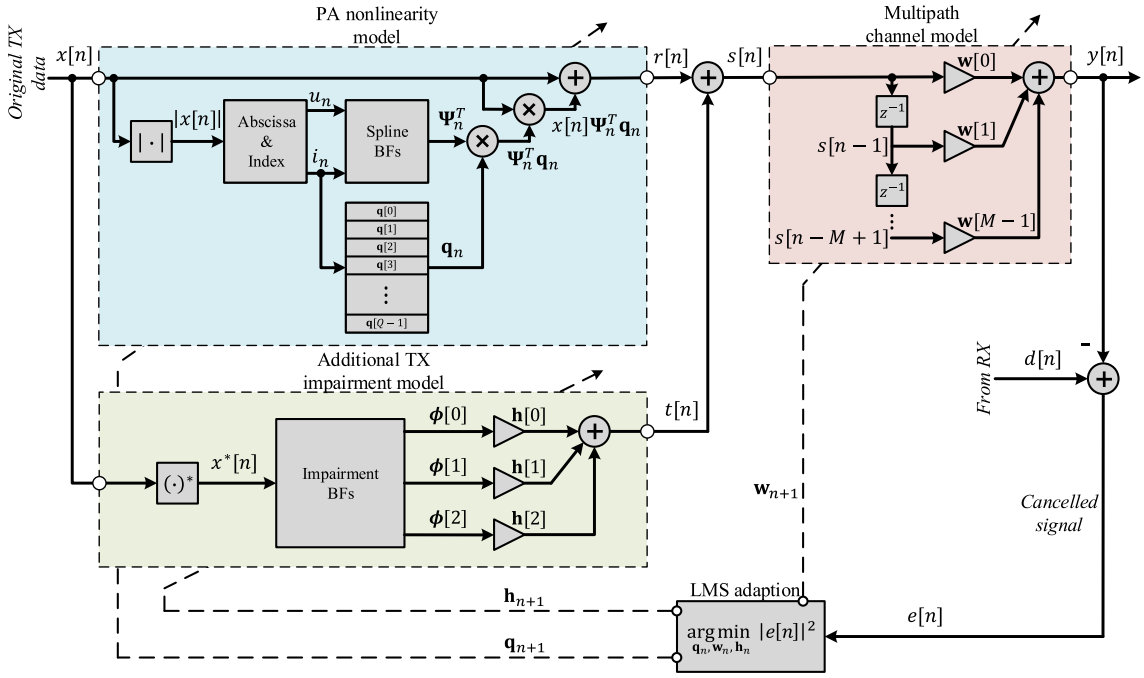


Fig. 3. Block diagram of the proposed extended Hammerstein model for identifying and cancelling the SI signal.

2) Additional TX impairment model: Following the analysis in Section II-B, we define the instantaneous basis function vector as

$$\boldsymbol{\phi}_n = \begin{bmatrix} 1 & x^*[n] & |x[n]|^2 x^*[n] \end{bmatrix}^T, \tag{8}$$

where the elements correspond (from left to right) to LO leakage, I/Q mismatch, and the cascade of I/Q mismatch and PA nonlinearity. Other basis functions, for example corresponding to the TX baseband nonlinearities, could be appended to $\boldsymbol{\phi}_n$ as well, based on needs on the chosen platform.

The output of the model is given as

$$t[n] = \mathbf{h}_n^T \boldsymbol{\phi}_n, \tag{9}$$

where $t[n]$ is the model output and $\mathbf{h}_n \in \mathbb{C}^{3\times 1}$ is the coefficient vector.

3) Multipath channel model: A linear FIR filter accounting for the effects of random reflections in the SI environment, is cascaded with the TX nonlinearity model. The input of the filter is the sum of the outputs of the nonlinear elements, $s[n] = r[n] + t[n]$. The filter output signal, and also the final output signal of the SI canceller model, is

$$y[n] = \mathbf{w}_n^T \mathbf{s}_n, \tag{10}$$

where $\mathbf{s}_n = [s[n + M_{\text{pre}}],\ s[n + M_{\text{pre}} - 1], \cdots, s[n - M_{\text{post}} + 1]]^T$ is the signal regression of $s[n]$ and $\mathbf{w}_n = \begin{bmatrix} w_n[0] & w_n[1] & \cdots & w_n[M-1] \end{bmatrix}^T$ is the coefficient vector, with $M = M_{\text{pre}} + M_{\text{post}} + 1$ being the considered memory in the model, including the pre- and post-cursor taps.

B. Gradient-based Learning Rules

To make the model capable of tracking possible changes in the SI channel or the transmitter impairments, we now derive adaptive learning rules for the coefficient vectors $\mathbf{q}_n$, $\mathbf{w}_n$ and $\mathbf{h}_n$, based on the least mean squares (LMS) gradient descent solution [39]. First, we write the output of the digital SI canceller, or the *error signal*, as

$$e[n] = d[n] - y[n], \tag{11}$$

where $d[n]$ is the received signal in the full-duplex transceiver, containing both the received signal of interest and the SI signal to be removed, and $y[n]$ is the output signal of the adaptive SI model (10). The cost function to be minimized is then defined as

$$J(\mathbf{w}_n, \mathbf{q}_n, \mathbf{h}_n) = e[n]e^*[n]. \tag{12}$$

In the LMS algorithm, the coefficients are adapted towards the negative gradient of the cost function. The updates require no special training signal, as the adaption is based on the transmit signal $x[n]$. The adaption rules for $\mathbf{w}_n$ and $\mathbf{q}_n$ were derived in [26], however they are reformulated with proper complex differentiation rules in Appendix B. The final learning rules are

$$\mathbf{w}_{n+1} = \mathbf{w}_n + \mu_w[n]e[n]\mathbf{s}_n^*, \tag{13}$$

$$\mathbf{q}_{n+1} = \mathbf{q}_n + \mu_q[n]e[n]\boldsymbol{\Sigma}_n^T \mathbf{X}_n^* \mathbf{w}_n^*, \tag{14}$$

where μ_w and μ_q are the respective adaptation step-sizes, $\mathbf{X}_n$ contains the signal regression of $x[n]$ in its main diagonal, and $\boldsymbol{\Sigma}_n = \begin{bmatrix} \boldsymbol{\Psi}_n & \boldsymbol{\Psi}_{n-1} & \cdots & \boldsymbol{\Psi}_{n-M+1} \end{bmatrix}^T$ contains the delayed M samples of $\boldsymbol{\Psi}_n$.

The learning algorithm for $\mathbf{h_n}$ is derived in Appendix B, and is given as

$$\mathbf{h}_{n+1} = \mathbf{h}_n + \mu_h e[n] \boldsymbol{\Phi}_n \mathbf{w}_n^*, \tag{15}$$

where $\boldsymbol{\Phi}_n = \begin{bmatrix} \boldsymbol{\phi}_n^* & \boldsymbol{\phi}_{n-1}^* & \cdots & \boldsymbol{\phi}_{n-M+1}^* \end{bmatrix}^T$ contains M delayed entries of the basis function vector $\boldsymbol{\phi}_n$. The learning

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TWC.2020.3040226, IEEE Transactions on Wireless Communications

TABLE I
COMPLEXITY ANALYSIS OF THE PROPOSED EXTENDED HAMMERSTEIN MODEL IN TERMS OF REAL MULTIPLICATIONS

Operation		Real multiplications
Model identification	$r[n]$	$P^2 + 3P + 7 + 1\text{sqrt}$
	$t[n]$	$4N_h - 2$
	$y[n]$	$3M$
	Total	$P^2 + 3P + 3M + 4N_h + 5 + 1\text{sqrt}$
Coefficient update	$\mathbf{w}_{n+1}$	$3M + 2$
	$\mathbf{q}_{n+1}$	$3Q + 2P\tau + 5\tau + 2$
	$\mathbf{h}_{n+1}$	$3N_h\tau + 3N_h + 2$
	Total	$3Q + 2P\tau + 3N_h\tau + 5\tau + 3N_h + 3M + 6$
Total iteration (model id. + coeff. update)		$P^2 + 3P + 2P\tau + 3Q + 7N_h + 3N_h\tau + 5\tau + 6M + 11 + 1\text{sqrt}$

TABLE II
COMPLEXITY COMPARISON WITH SIMILAR ALGORITHMS FOUND IN LITERATURE

Model	Complexity
This work	$\mathcal{O}(M) + \mathcal{O}((N_h + P)\tau) + \mathcal{O}(Q)$
Spline-based Hammerstein [26]	$\mathcal{O}(M) + \mathcal{O}(P\tau) + \mathcal{O}(Q)$
Cascade Kalman filter [43]	$\mathcal{O}(N_{BF}\frac{(R+M)\log_2(R+M)}{R})$
Parallel Hammerstein, no orthogonalization [44]	$\mathcal{O}(N_{BF}M)$
Parallel Hammerstein, w/ orthogonalization [44]	$\mathcal{O}(N_{BF}^2M^2)$
Parallel Hammerstein [45]	$\mathcal{O}(N_{BF}M) + \mathcal{O}(N_{BF}^2)$

rules of $\mathbf{q}_n$ and $\mathbf{h}_n$ assume that the rate of change is small, that is, they are assumed approximately constant over a period spanning M samples.

The updates of $\mathbf{q}_n$ and $\mathbf{h}_n$ in (14) and (15) require a multiplication with the filter coefficient vector, which spans M samples. The amount of required multiplications can be limited, if only τ most significant taps around the $M_{\text{pre}} + 1$ tap are considered. This does not significantly hinder the cancellation performance [26], while it greatly reduces the amount of required multiplications, and also keeps the amount fixed and independent of the number of filter taps.

C. Computational Complexity

Here, we present a complexity analysis of the proposed algorithm and compare it to other relevant solutions found in literature. Using the aforementioned simplification in updates of $\mathbf{q}_n$ and $\mathbf{h}_n$, and by marking the amount of basis functions in the additional TX impairment modeling as N_h, the computational complexity in terms of real multiplications is presented in Table I. The analysis assumes one complex multiplication takes three real ones. The complexity of the square root operation is marked as sqrt, as it can be implemented in a variety of ways with varying complexities. Assuming viable values of $M = 60$, $P = 2$, $Q = 10$, $N_h = 3$ $\tau = 5$ and $\text{sqrt} = 2$ for the coefficients, the total complexity of the algorithm can be calculated to be 524 real multiplications. Without the simplification from τ, the amount of multiplications would be 1514, which is considerably larger to the point of being unfeasible in a real-time implementation.

Table II collects the approximate complexities of this work and similar ones found in literature for reference. The spline-based Hammerstein model of [26] does not consider additional TX impairments beyond the PA, and thus the algorithm is slightly lighter in computations compared to this work. The numeric examples are given with the coefficient values presented earlier. In [43], a frequency domain Kalman filter solution is proposed, which is applied to the signal in blocks. The complexity presented in Table II is given per processed sample, where N_{BF} is the amount of basis functions considered, and R the frame shift of the system. The Parallel Hammerstein-type systems of [44] and [45] offer a traditional approach to the SI problem, with [44] omitting orthogonalization being relatively low complexity in terms of Hammerstein systems. Adding the full orthogonalization greatly increases the complexity. While [45] also considers orthogonalization, the effect is not as dire, as the orthogonalization is only carried out to the instantaneous basis functions.

IV. TESTBED AND CANCELLER FPGA IMPLEMENTATION DETAILS

This section focuses on the real-time implementation details of the eDSIC solution introduced in the previous section. The implemented testbed has two main parts: the transceiver code, consisting of code executed on a host PC and the FPGA, and the eDSIC canceller, which is running entirely real-time on the target FPGA.

A. Transceiver Testbed

The eDSIC is implemented as an extension to a transceiver testbed coded in LabVIEW Communications System Design Suite 2.0. The testbed contains two main parts, the first of which is the host side program, run entirely on a host PC. This part of the testbed is responsible for uploading the bitfile, which determines the behaviour of the FPGA, to the target platform, controlling the FPGA program by tuning parameters and collecting data that is transferred to the host from the FPGA. Additionally, some arithmetic that is not required at real-time, such as delay estimation, is performed on the host side. The second part, the real-time code, is run in its entirety on the target FPGA. In order to take full

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TWC.2020.3040226, IEEE Transactions on Wireless Communications

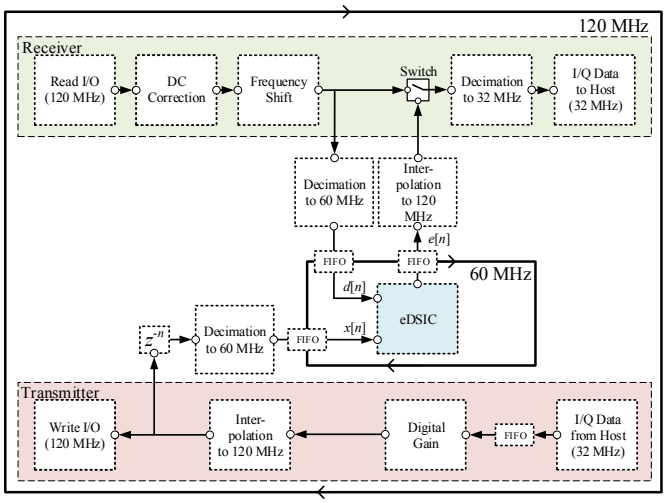


Fig. 4. Block diagram of the baseband transceiver code on the FPGA, complete with the eDSIC and additional necessary functionality.

advantage of LabVIEW's FPGA tools and to achieve real-time operation, the developed code is implemented on an FPGA of a National Instruments' (NI) USRP device. The FPGA of the USRP device is a Xilinx Kintex-7 family model XC7K410T, whose utilizable resources are shown in Table III. The digital baseband signal processing takes place on the FPGA, utilizing complex I/Q data. In addition to the FPGA, the USRP platform contains two full-duplex capable direct-conversion transceiver front-ends. The employed USRP has a frequency range from 400 MHz to 4.4 GHz and maximum instantaneous bandwidth of 120 MHz.

In order to demonstrate the effectiveness of the proposed eDSIC algorithm, a direct-conversion (zero-IF) transmitter architecture is adopted for the transmitter. The receiver utilizes a low-IF architecture, where I/Q downconversion from RF is first done to an IF of 7.5 MHz, and a digital frequency shift block handles the conversion to baseband. Consequently, the I/Q image stemming from the receiver I/Q mismatch is out of band and does not affect the operation of the eDSIC, thus making the transmitter chain the only significant source of I/Q mismatch induced imperfections.

Fig. 4 illustrates an overview of the transceiver code, complete with the eDSIC and required additional functionality, implemented in LabVIEW Communications System Design Suite 2.0. The transmitter chain reads a block of 16-bit I/Q samples from the host, which are generated at a sample rate of 32 MHz. To ensure continuous transmission, the data is read from the host only once, and the same block of data is looped continuously. The data is stored within an internal first-in-first-out (FIFO) buffer, containing 130k samples. First, the samples are digitally amplified, after which they are interpolated to the analog-to-digital converter (ADC) clock rate of 120 MHz. These samples are sent to the digital SI canceller and transmitted by writing them to the I/O of the device. In the receiver chain, data is read from the I/O provided by the 14-bit ADC with effective number of bits (ENOB) of 11.4. These values affect the quantization noise, which has been determined not to limit the achievable digital cancellation levels. The received I/Q samples are sent to the canceller after DC-offset removal and frequency shift from IF to baseband. The DC-offset biases the canceller under limited numerical accuracy, which deteriorates the performance and it is therefore removed. The receiver chain then decimates the received signal back to the original sampling rate of 32 MHz, before sending the samples back to the host via a direct memory access (DMA) FIFO.

B. eDSIC FPGA Implementation

Since the eDSIC runs in its own loop, the data needs to be sent between it and the transceiver loop by internal FIFO buffers to ensure lossless data transfer. Additionally, the input $x[n]$ has to be delayed in accordance to the delay introduced by the ADC and DAC and SI signal propagation, so that the samples $x[n]$ and $d[n]$ correspond with each other. The delay is estimated on the host PC by cross-correlation between the transmitted and received signals. For this purpose, data containing the signals $x[n]$ and $d[n]$ is transferred to the host using DMA FIFOs.

The eDSIC is executed at 60 MHz in order to minimize the need of pipeline stages, thus retaining near real-time operation. The 60 MHz realization of the canceller utilizes five pipeline stages, i.e., it takes an input five cycles to produce the corresponding output. This corresponds to a latency of around 83 ns. Combined with the added delays of 6 cycles from both the interpolation and decimation tasks in the 120 MHz loop, the overall introduced latency to the system from the eDSIC related functionality is approximately 183 ns. Lowering the sample rate is not necessary for the algorithm, but it eases the FPGA programming effort by allowing more operations per iteration, thus requiring less rigorous pipeline delay placement. 60 MHz was chosen due to the relative ease of the implementation of the decimation and interpolation tasks required by the lowered sample rate.

In addition to the pipeline registers, the developed eDSIC code introduces some minor changes to the presented structure to make it FPGA compliant. The code utilizes fixed-point arithmetic, and the bit widths and radix points of the internal values are chosen based on simulations. The 16-bit input values of $x[n]$ and $d[n]$ are interpreted as having 4 integer bits (including the sign bit) and 12 fractional bits, mapping the values to range from -8 to +8. This range fully supports the arbitrary amplitude range chosen for the input signal, which is from 0 to +8. For simplicity, we consider unit spline knot spacing, $\Delta_A = 1$, thus, following the spline interpolation basics from Appendix A, the signal range is divided into 8 regions. To accommodate second order interpolation, the spline control-point LUT has 2 additional entries, making the LUT 10 elements deep.

Important limiting factors for the fixed-point arithmetic are the DSP48 units, responsible for the multiplication tasks, which are restricted to 18×25 bits. Multiplications between higher bit width values force the use of unnecessarily many DSP48s, therefore all multiplications within the system adhere to the given limit. Furthermore, the LabVIEW program only supports bit widths of up to 64 bits. With these restrictions,

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TWC.2020.3040226, IEEE Transactions on Wireless Communications

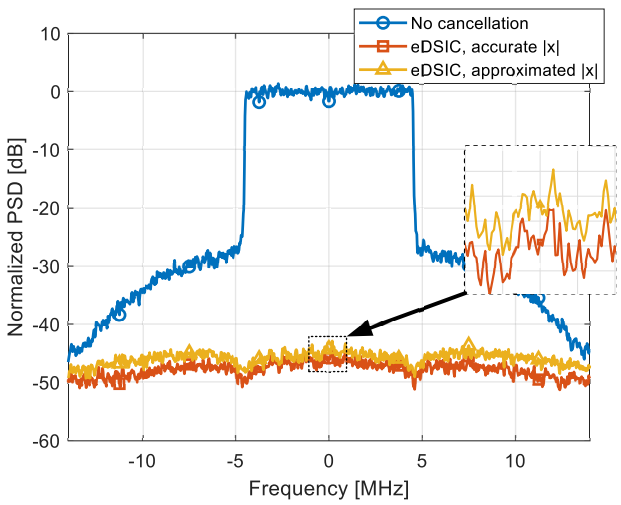


Fig. 5. Comparison of the performance of the eDSIC with double precision accuracy and approximate values using Equation (16) for absolute value of $x[n]$, simulated with data captured from the target SDR system.

the intermediate values are truncated and rounded to prevent overflows, but also use largest available bit widths.

The simplification to matrix multiplications introduced in Section III-B of considering only the most significant taps is employed in the implementation. Additionally, considering the second order spline interpolation and the choice of knot spacing ($\Delta_A = 1$), the computation of $\mathbf{u}_n^T\mathbf{C}$ in (24) saves two real multiplications. The additional required multiplication in $\mathbf{u}_n^T\mathbf{C}$ can be further carried out by bit shift, saving an additional multiplication.

The algorithm requires determining the magnitude of a complex number (see (20) and (21) in Appendix A), which in turn requires the computation of a square root. In a digital environment, this computation is traditionally carried out by iterative methods, such as the Coordinate Rotation Digital Computer (CORDIC) algorithm, which require multiple clock cycles to reach the result. While iterative methods provide more accurate approximations, in order to achieve real-time operation, and to save resources, we utilize simple approximating formulas in this work. To this end, the magnitude of $x[n]$ is approximated by [26], [46]

$$|x[n]| \approx \alpha \max(|\mathrm{Re}\{x[n]\}|, |\mathrm{Im}\{x[n]\}|) + \beta \min(|\mathrm{Re}\{x[n]\}|, |\mathrm{Im}\{x[n]\}|). \quad (16)$$

Choosing static values $\alpha = 0.96043387$ and $\beta = 0.397824735$ yields a maximum absolute error of 3.95 % and standard deviation of 2.70 % for the magnitude error [46]. Simulations made with measured data from the target system indicate that the performance of the eDSIC does not significantly decline with the use of the introduced approximation. Fig. 5 shows a simulation case comparing the performances using a double precision and approximated values for the magnitude, utilizing measured data from the platform. The difference is inconsequential, being only in the order of 1 dB in the inband portion and less than 3 dB in the out-of-band portion of the signal, considering the computational lightness of the approximation. However, if much greater cancellation fidelity is sought, some other method for calculating the absolute value should be used.

TABLE III
RESOURCE USAGE OF THE DIGITAL SI CANCELLER ON THE XILINX KINTEX-7 FPGA WITH $M = 60$

	DSP48s	LUTs	Registers	Total Slices
Available	1 540	254 200	508 440	63 550
Used	502	85 663	38 718	26 589
Percentage (%)	32.6	33.7	7.6	43.1

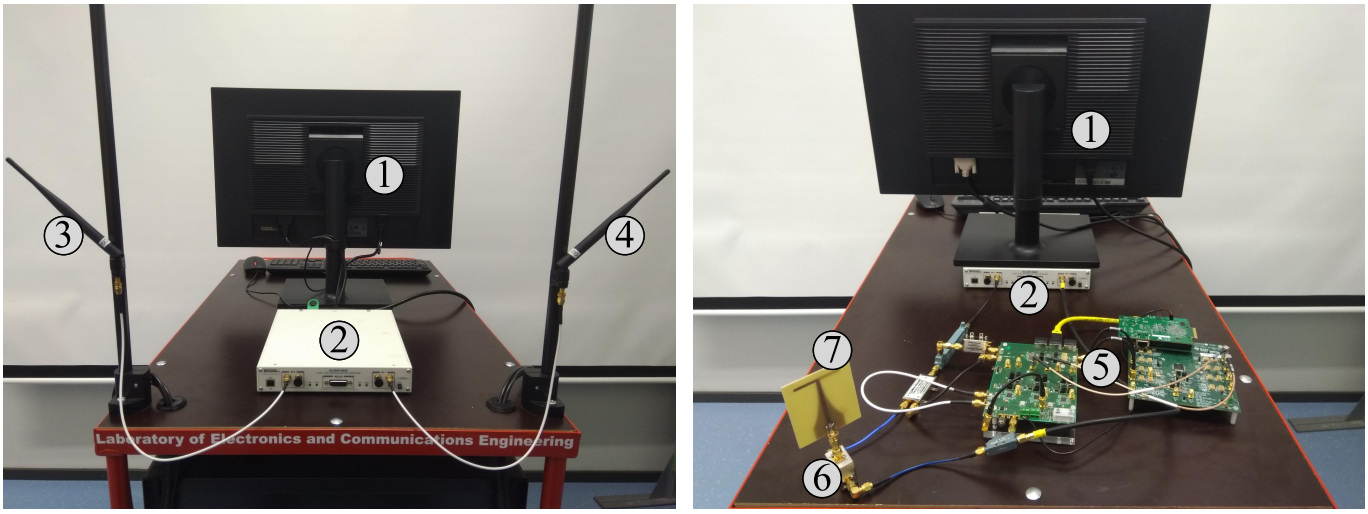
The final resource usage of the eDSIC is shown in Table III, considering 60 taps of memory. With the introduced simplifications, the implemented algorithm employs around 33 % of the available DSP48 units, which includes both the main path processing and the update of the model coefficients. Combined with the low 34 % utilization of LUTs and only 7.6 % of registers, the algorithm leaves plenty of space on the FPGA for other functionalities, such as orthogonal frequency-division multiplexing (OFDM) processing, and underlines the low complexity of the described eDSIC algorithm.

V. REAL-TIME EXPERIMENTS

The functionality and performance of the described eDSIC algorithm implementation is validated with real-time measurements in this section. First, the achieved level of SI suppression is studied in various scenarios. Here, two nodes with different methods of analog SI suppression are employed, and are referred to as Node 1 and Node 2 hereafter, shown in Fig. 6. Node 1 utilizes two separate off-the-shelf antennas to obtain a constant passive propagation domain isolation of around 42 dB between the TX and RX chains. Node 2 is a single-antenna node, where analog suppression is achieved with a circulator combined with an active RF canceller connected between the TX and RX chains. Combined with the circulator, in ideal circumstances, the utilized RF canceller is capable of providing SI cancellation of up to 70 dB with the signal bandwidths used in the measurements, even in the presence of highly nonlinear PAs [47]. In order to show the benefit of the proposed eDSIC algorithm, the SI suppression measurements are additionally carried out with and compared to an implementation of the DSIC algorithm from [26]. Moreover, the combined cancellation performance of the eDSIC and the RF canceller is tested with an external PA. The level of inband SI cancellation is measured as the signal-to-interference-and-noise ratio improvement, as is common in the field. In all of the experiments, the canceller coefficients are initialized as zeros before adaption.

In addition to the pure cancellation performance, the implemented eDSIC is tested in a bidirectional full-duplex scenario, to validate the effectiveness of the proposed algorithm in a communications link. In these measurements, both nodes are utilized in full-duplex operation. For comparison, the same setups are operated in half-duplex mode. In this work, the figures of merit for the bidirectional system operation are the signal-to-interference-plus-noise ratio (SINR), the symbol error rate (SER) and the sum-rate of the system, determined

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TWC.2020.3040226, IEEE Transactions on Wireless Communications



(a) Node 1. (b) Node 2.

Fig. 6. Experiment node setups. Both nodes include a host PC (1) and a USRP SDR device (2). Node 1 employs separate antennas for the TX (3) and RX (4) chains. In Node 2, the analog suppression is achieved with an RF canceller (5) and a circulator (6), allowing the use of a single custom-made antenna (7).

using the capacity of the channel between nodes. SINR in decibels can be estimated as

$$\mathrm{SINR_{dB}} = 10\log_{10}\left(\frac{\frac{1}{N}\sum_{k=1}^{N}|s_{\mathrm{i},k}\hat{h}_k|^2}{\frac{1}{N}\sum_{k=1}^{N}|s_{\mathrm{r},k}-s_{\mathrm{i},k}\hat{h}_k|^2}\right), \quad (17)$$

where N is the total number of symbols transmitted and received, $s_{\mathrm{i},k}$ the ideal received symbol at index k, $\hat{h}_k$ the channel estimate between the transmitter and receiver and $s_{\mathrm{r},k}$ the received symbol at index k. SER is determined by

$$\mathrm{SER} = \frac{N_e}{N}, \quad (18)$$

where N_e is the amount of misinterpreted received symbols, utilizing maximum likelihood detection. Finally, the normalized channel capacity C for a single node can be determined according to Shannon's well-known capacity theorem as

$$C = \log_2(1+\mathrm{SINR})(\mathrm{bits/s/Hz}), \quad (19)$$

where SINR is given as a linear value for the node. In a system with two nodes with capacities C_1 and C_2 measured in half-duplex operation, the total sum-rate can be defined as $\frac{1}{2}(C_1+C_2)$, assuming a single node transmits exactly half of the time. In full-duplex context, the sum-rate can be defined simply as the sum of the two capacities, C_1+C_2, here measured in full-duplex operation, assuming both nodes are constantly transmitting.

A. Functional Validation of the Canceller

First, as a proof-of-concept, the eDSIC solution is tested with a 10 MHz Long-Term Evolution (LTE)-like OFDM signal with peak-to-average power ratio (PAPR) of about 7 dB, at 7 MHz low-IF, transmitted at 16 dBm and with the TX and RX chains connected through a 40 dB attenuator. The transmitted power, as all others mentioned in the paper, were measured from the USRP TX output. This setup reveals the severity

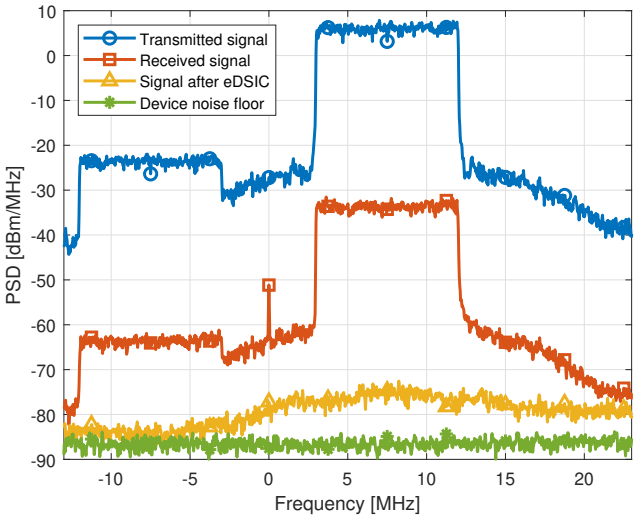


Fig. 7. Proof-of-concept measurement case with the eDSIC, the signal at low-IF of 7 MHz and the TX power at 16 dBm.

of the I/Q imbalance of the transmitter, which would be hidden beneath the received signal if zero-IF transmitter was utilized. Additionally, the I/Q image suppression capability of the eDSIC algorithm becomes evident with this setup. Illustrated in Fig. 7 are the spectra of the transmitted and received signals, signal after eDSIC and the noise floor in this measurement case. The I/Q image appears around 32 dB lower than the transmitted signal. With the eDSIC, the I/Q image is suppressed to around 1 dB of the noise floor, and the in-band SI is suppressed by ∼43 dB.

The proper functional validation measurement setup consists of either of Node 1 or 2. The node in question is placed in the center of a room, in order to avoid excessive reflections from surrounding objects. The transmission is turned on, after which the digital canceller is activated. In the case of Node 2, the RF canceller is tuned before the digital canceller is turned on. This sequence is performed for 10 different TX powers for both

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TWC.2020.3040226, IEEE Transactions on Wireless Communications

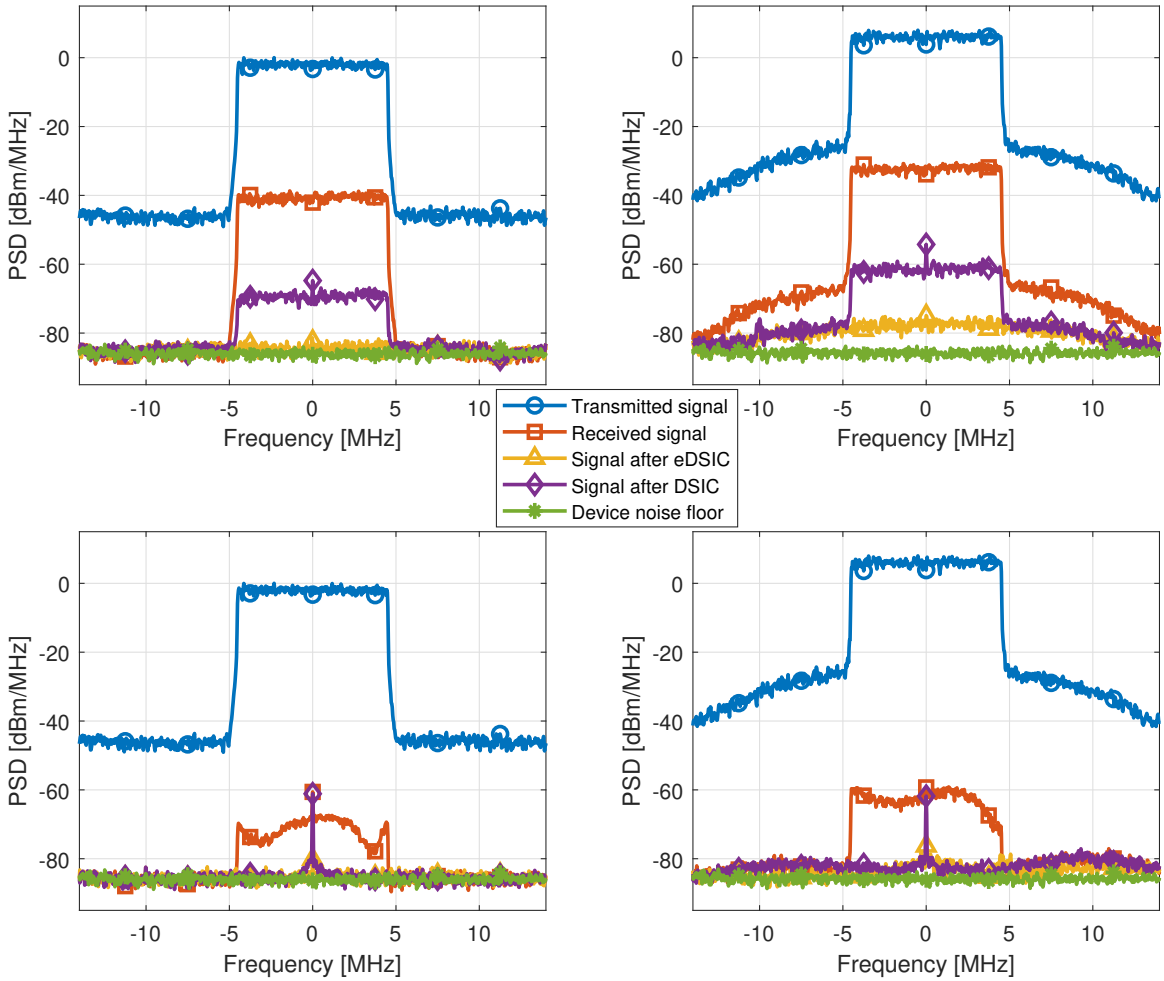


Fig. 8. PSD of selected measurement cases, with the transmitted signal, received SI signal, digitally suppressed SI signal and noise floor shown. Clock-wise from top left: Node 1 with 8 dBm TX power, Node 1 with 16 dBm TX power, Node 2 with 16 dBm TX power and Node 2 with 8 dBm TX power.

nodes, using both eDSIC and DSIC for digital cancellation. The TX powers range from 0 to 18 dBm, with intervals of 2 dBm. The measurements utilize LTE-like OFDM signals with normal cyclic prefix length, a PAPR of 7 dB, bandwidth of 10 MHz, and the transmitter carrier frequency at 2.45 GHz. The receiver operates at 2.435 GHz, meaning an IF of 15 MHz, which is handled by a digital frequency shift.

Fig. 8 illustrates PSDs of selected measurement cases, namely cases with 8 and 16 dBm TX power for both nodes plotted as in Section II-B. Fig. 8 shows that the SI canceller is able to further suppress the SI signal even with notable nonlinear distortion. Furthermore, the advantage of employing the eDSIC algorithm instead of the DSIC becomes evident in the cases with Node 1, as the residual inband power is around 15 dB higher when the eDSIC is not employed. Cases with Node 1 demonstrate around 43 dB and 45 dB of inband cancellation. While these figures represent excellent cancellation, the residual power of the SI signal is still visibly above the noise floor, considerably so with the 16 dBm TX power case. This is due to the relatively low analog SI suppression of 42 dB of the antennas. Hence, the total cancellation of the SI is in the order of 80 dB in Node 1. With Node 2, the RF isolation is at a much higher level, about 67 dB in both of the shown measurement cases. Thus in this case, the residual powers after digital cancellation, with both the DSIC and eDSIC, are close to noise floor, with less than 1 dB gap in the 8 dBm TX power case. The combined cancellation is, at best, up to 90 dB with Node 2.

The inband digital cancellation numbers in all the measurement cases are shown in Fig. 9. In Node 1, the I/Q image, which is around 32 dB below the transmitted signal power, is left untouched by the DSIC, thus limiting the achievable inband SI cancellation. With the eDSIC solution, this limit does not exist and the implemented canceller is capable of achieving a cancellation level of up to 46 dB. Again, the RF canceller is capable of suppressing the SI considerably more than what antenna isolation can provide. Therefore the digital cancellation in Node 2 is notably lower, and the difference between eDSIC and DSIC is not as apparent as in Node 1. Still, it is evident from Fig. 9 that the eDSIC can provide improved full-duplex performance in various circumstances.

Finally, the combined SI suppression capability of the RF canceller and the eDSIC is tested with an external PA. The utilized PA is a Mini-Circuits ZHL-16W-43+ high power

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TWC.2020.3040226, IEEE Transactions on Wireless Communications

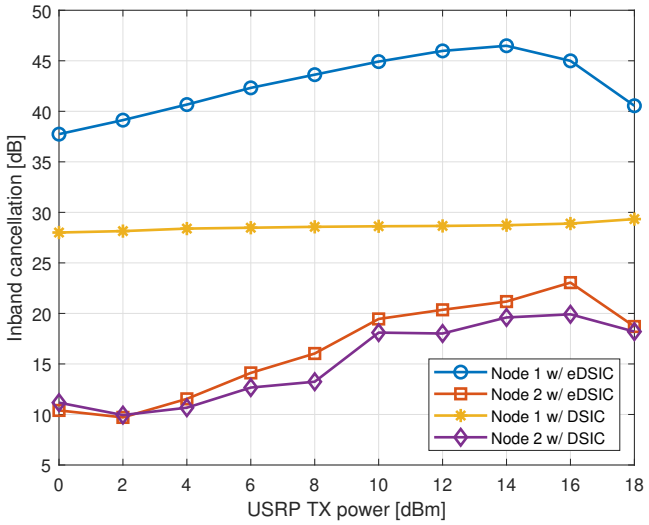


Fig. 9. Achieved inband cancellations of eDSIC and DSIC in Nodes 1 and 2 with various TX powers of the USRP.

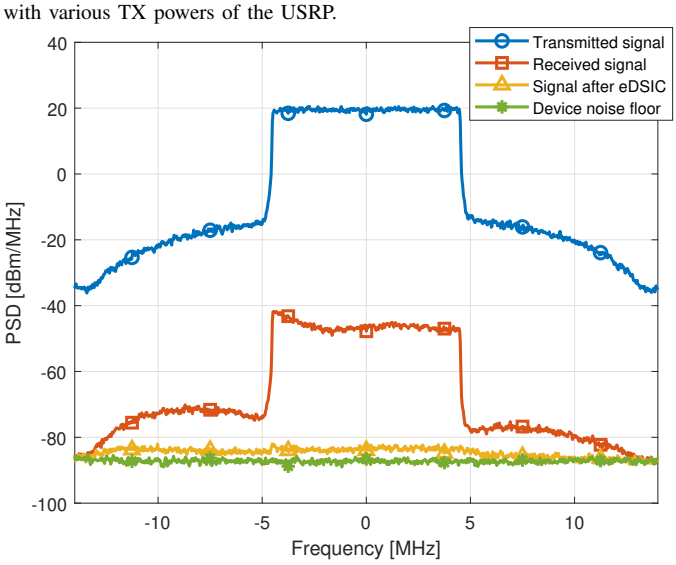


Fig. 10. PSDs of signals using Mini-Circuits ZHL-16W-43+ PA, demonstrating total inband SI cancellation of 103 dB.

amplifier. The output power of the PA is set to 30 dBm. In order to avoid damage to the devices, the analog isolation now employs separate antennas for TX and RX chains, having an isolation of around 40 dB, while the RF canceller brings an extra 26 dB of isolation. The cancellation performance is depicted in Fig. 10, showing a total SI suppression of 103 dB. The residual, which consists of residual SI and noise power, lies around 3.5 dB above the device noise floor. This example, together with the ones presented earlier, demonstrate excellent cancellation performance of the eDSIC algorithm in a direct-conversion transmitter context.

We compare the achieved performance to relevant implementations found in literature, where completely real-time operation is evident. There are only a handful of such publications [3], [33], collected in Table IV for convenience. Early work by Jain *et al.* [30] features the first known real-time full-duplex system. Here, a custom platform featuring an FPGA is utilized to run a linear filter solution in real-time, achieving 30 dB of digital cancellation. Combined with a balun, they are

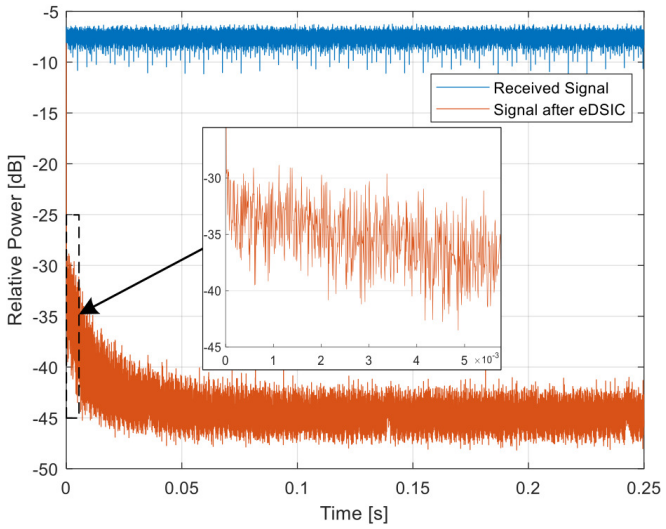


Fig. 11. Convergence of the implemented eDSIC algorithm in Node 1, with 16 dBm TX power.

able to demonstrate 73 dB of total isolation. Later, in 2015 Chung *et al.* [48] demonstrated a real-time digital cancellation of 43 dB using linear filtering on a NI PXIe-7965R platform. In conjunction with their analog suppression, they are able to obtain total isolation of up to 103 dB for a 10 MHz signal. 2016 saw an implementations of nonlinear parallel Hammerstein based model implemented on an FPGA of a NI PXIe-7972R module [31]. This implementation relies on pre-computed basis functions stored on a random-access memory (RAM) to reduce implementation complexity, demonstrating nonlinear digital cancellations of up to 35 dB, taking into account the nonlinear behaviour of the PA. On top of that, a total SI isolation of 94.9 dB is reported, utilizing an active RF canceller. More recently, in 2018 Li *et al.* [33] demonstrated another linear digital canceller implementation, capable of 30.6 dB of digital cancellation and total isolation of 72.5 dB with a respectable 123 MHz bandwidth. This is made possible by an FPGA implementation of a blind linear equalizer and a custom made linearly polarized antenna. Finally, in [32] Soriano-Irigaray *et al.* showcased the best linear cancellation to date, achieving up to 48 dB of digital cancellation and 104 dB of total isolation, with the linear filter solution implemented on on FPGA and the proper cancellation of the SI signal taking place in the analog domain. Compared to the works in these publications, our prototype is capable of producing more nonlinear digital cancellation in real-time than any other reported system, while also having the benefit of compensating for the I/Q imbalance and LO leakage, not just the PA nonlinearity. Moreover, our solution is on par with the state-of-the-art linear implementations that can, however, only perform well in linear environments, which is not the case in many practical, especially low-cost, systems.

B. Example Convergence

Fig. 11 plots the residual power of the signal after the eDSIC against time. The measurement was carried out with Node 1, transmitting the LTE-like OFDM signal at 16 dBm. The

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TWC.2020.3040226, IEEE Transactions on Wireless Communications

TABLE IV
COMPARISON OF THE PERFORMANCE METRICS OF THIS WORK AND RELEVANT REAL-TIME SI CANCELLER IMPLEMENTATIONS FOUND IN LITERATURE

Prototype	Year	Frequency [GHz]	Bandwidth [MHz]	Output Power [dBm]	Model	Digital Cancellation [dB]	Total Isolation [dB]
This work	2020	2.45	10	14	Augmented Spline-based Hammerstein	46	103
[32]	2018	2.4	18	8	Linear FIR Filter	48	104
[33]	2018	3.5	123	0	Linear FIR Filter	30.6	72.5
[31]	2016	2.45	20	10	Parallel Hammerstein	35	94.9
[29]	2015	2.52	10	N/A	Linear FIR Filter	43	103
[30]	2011	2.4	10	N/A	Linear FIR Filter	30	73

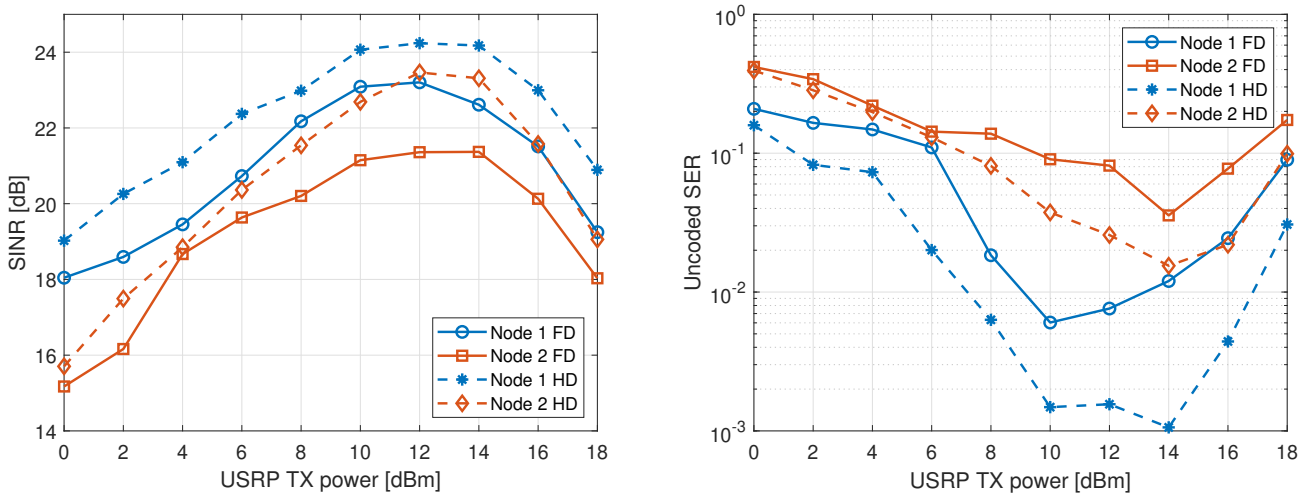


Fig. 12. Average SINR and SER for Nodes 1 and 2 in FD and HD operations, with various TX powers of the USRP, OFDM signal with 20 MHz bandwidth and 64-QAM subcarrier modulation.

powers of the signals are averaged in blocks of 500 samples. Fig. 11 shows that the algorithm converges in approximately 100 milliseconds, which corresponds to 6×10^6 iterations of the algorithm. However, the initial convergence to around -32 dB happens in less than 0.1 ms. The relatively slow adaptation to finally reach maximum SI cancellation can be explained by the utilization of the LMS coefficient update rules, which have been shown to be considerably slower to adapt than for example least-squares based solutions. The slow adaption is one of the few drawbacks of the LMS update scheme. However, the convergence speed can be considered sufficient for most systems, since the SI channel and transmitter impairments are typically slowly varying.

C. Bidirectional Full-Duplex with OFDM Signals

The operation of the eDSIC is further studied in a bidirectional full-duplex communication scenario. For this purpose, Nodes 1 and 2 are again employed, this time utilized simultaneously and placed 4 m apart. In the measurements, both nodes operate in full-duplex mode taking advantage of the eDSIC and node specific RF isolation methods. Measured here are the received signals after the digital cancellation in the full-duplex node. For the sake of comprehensiveness, the system is benchmarked by measuring the same scenario, but in half-duplex operation, where the nodes take turns in acting as transmitter and receiver. By comparing the half-duplex link to the full-duplex one, the improvement in the channel capacity can be evaluated. The links are measured with 10 TX powers, again from 0 dBm to 18 dBm as was the case in the functional validation. The transmitted signals are 20 MHz LTE-like OFDM signals, carrying 64-QAM symbols as the payload, with the TX frequency set to 2.45 GHz. RX chain operates at 2.345 GHz and the samples are digitally frequency shifted by 15 MHz, as was the case in the functional validation. The postprocessing, including synchronization and demodulation of the signals is done offline using MATLAB. The presented results are averages from 9-10 measurements, each one containing 28 OFDM symbols. A single measurement may suffer from external interference, such as Wi-Fi signals. Such cases were discarded from the results.

The SINR and SER results for different TX powers, averaged over all subcarriers and OFDM symbols, are shown in Fig. 12 for both nodes, both in full-duplex and half-duplex operation. It is worth noting, that since Node 1 employs two antennas, and the immediate environment around the nodes are not consistent, the conditions are not symmetrical for the two nodes. Therefore it is more reasonable to compare the full-duplex and half-duplex operations within a single node as opposed to comparing the performances of the nodes with each other. It is obvious from Fig. 12 that the full-duplex operation deteriorates the link, as is expected since the full-duplex operation adds interference to the received signals. In terms of SINR, the performance is around 2-4 dB worse in full-duplex

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TWC.2020.3040226, IEEE Transactions on Wireless Communications

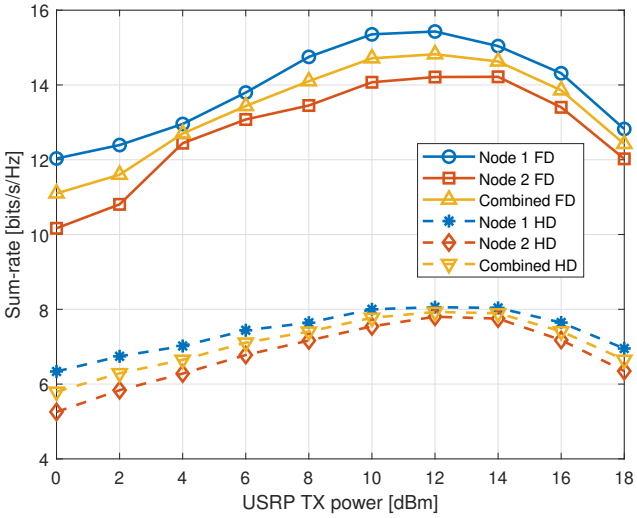


Fig. 13. Sum-rates of the system with various TX powers, in full-duplex (FD) and half-duplex (HD) contexts, measured using the SINR values from Fig. 12.

operation. This result translates to the obtained SER figures, as SER results are visibly worse in full-duplex operation as well. However, the maintained levels are still acceptable, and the benefit from constantly being able to utilize the available channel outweighs the minor performance deterioration.

Lastly, Fig. 13 illustrates the improvement in channel capacity as sum-rates calculated using the SINR values from Fig. 12. Here, it is assumed that the the system either consists of two identical nodes (either Node 1 or 2) with identical capacities, or the system contains both Nodes 1 and 2, which is presented as the combined case in Fig. 13. Generally, all possible systems exhibit sum-rate improvements of up to 1.9 times when comparing the full-duplex and half-duplex cases. This increase in throughput is just shy of the doubling full-duplex could theoretically provide. In practice, this limit cannot be reached, however, so the demonstrated improvement is near the physical maximum capacity increase the full-duplex technology can provide.

VI. Conclusions

In this paper, we have introduced a novel, low complexity SI canceller algorithm for direct-conversion transmitters and verified its functionality with a real-time FPGA implementation and extensive experimentation. The presented algorithm is based on a Hammerstein model utilizing spline adaptive filters, which has previously been shown to be an attractive approach due to its low computational complexity compared to traditionally used memory-polynomial-based models. However, the basic Hammerstein model can only model PA nonlinearity and the linear SI channel, and thus cannot handle the other impairments intrinsic to direct-conversion transmitters such as I/Q mismatch, LO leakage, and baseband nonlinearities. To this end, we propose an extended Hammerstein model, which contains the most significant additional transmitter impairments, while retaining low complexity. This is emphasized by the FPGA resource utilization of the developed real-time solution: only 502 DSP48 units are needed for the entire algorithm, including the coefficient updates. Performance-wise, the real-time SI cancellation of up to 46 dB is among the highest in literature, while also having the benefit of performing in the presence of nonlinear PAs and severe I/Q mismatch, unlike earlier real-time solutions. In real-time bidirectional communications experiments, the canceller solution provides performance very close to the physical limits that full-duplex technology can provide, by increasing the throughput of the system by 90 % compared to half-duplex in a symmetric communication scenario. Overall, the results presented in this work demonstrate the feasibility of full-duplex technology in future communication systems. Works such as this help bring the technology closer to commercial reality.

Appendix A
Spline Interpolation Formulas

We present the basic equations for using a spline-interpolated LUT with uniform knots with a spacing of Δ_A, assuming a real-valued unipolar input signal $A[n]$ with maximum amplitude of $A_{\max}$. In this work, $A[n]$ is the instantaneous magnitude of a complex signal $x[n]$, defined as $A[n] = \sqrt{\mathrm{Re}\{x[n]\}^2 + \mathrm{Im}\{x[n]\}^2}$. In a P-th order uniform spline interpolation scheme [41], [49], the input signal range is divided into $K = A_{\max}/\Delta_A$ regions, accessed and used according to the index, abscissa value, and abscissa vector, defined respectively as

$$i_n = \left\lfloor \frac{A[n]}{\Delta_A} \right\rfloor + 1, \tag{20}$$

$$u_n = \frac{A[n]}{\Delta_A} - (i_n - 1), \tag{21}$$

$$\mathbf{u}_n = \begin{bmatrix} u_n^P & u_n^{P-1} & \cdots & 1 \end{bmatrix}^T. \tag{22}$$

The interpolated output can then be written as

$$f[n] = \mathbf{\Psi}_n^T \mathbf{q}, \tag{23}$$

where $\mathbf{q} = \begin{bmatrix} q_0 & q_1 & \cdots & q_{Q-1} \end{bmatrix}^T$ is the vector of control points with $Q = K + P$ elements and

$$\mathbf{\Psi}_n = \begin{bmatrix} 0 & \cdots & 0 & \mathbf{u}_n^T\mathbf{C} & 0 & \cdots & 0 \end{bmatrix}^T, \tag{24}$$

with the vector $\mathbf{u}_n^T\mathbf{C}$ being indexed such that the starting position is i_n, in order to multiply the corresponding control points in $\mathbf{q}$. The matrix $\mathbf{C}$ contains the coefficients of the P-th order spline basis functions. In the case of 2nd order B-spline interpolation, which we assume in this work, $\mathbf{C}$ takes the form

$$\mathbf{C} = \frac{1}{2} \begin{bmatrix} \frac{1}{\Delta_A^2} & \frac{-2}{\Delta_A^2} & \frac{1}{\Delta_A^2} \\ \frac{-2}{\Delta_A} & \frac{2}{\Delta_A} & 0 \\ 1 & 1 & 0 \end{bmatrix}. \tag{25}$$

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TWC.2020.3040226, IEEE Transactions on Wireless Communications

APPENDIX B
LMS LEARNING RULES OF THE MODEL COEFFICIENTS

The LMS update is generally expressed as [39]:

$$\mathbf{c}_{n+1} = \mathbf{c}_n - \mu \frac{\partial J}{\partial \mathbf{c}_n^*}, \tag{26}$$

where $\mathbf{c}_n$ is a generic coefficient vector to update, μ the step-size and $J = e[n]e^*[n]$ the cost function defined using the instantaneous error $e[n]$. To derive the LMS learning rules, the derivative of the cost function with respect to the corresponding coefficient vector needs to be defined, while assuming that the other coefficient vectors are constant.

The derivative of the cost function with respect to the FIR filter coefficients $\mathbf{w}_n$ is written as

$$\frac{\partial J(\mathbf{w}_n, \mathbf{q}_n, \mathbf{h}_n)}{\partial \mathbf{w}_n^*} = \frac{\partial e[n]e^*[n]}{\partial \mathbf{w}_n^*} \tag{27}$$

$$= e^*[n]\frac{\partial e[n]}{\partial \mathbf{w}_n^*} + e[n]\frac{\partial e^*[n]}{\partial \mathbf{w}_n^*} \tag{28}$$

$$= 0 - e[n]\frac{\partial \mathbf{w}_n^H \mathbf{s}_n^*}{\partial \mathbf{w}_n^*} \tag{29}$$

$$= -e[n]\mathbf{s}_n^*, \tag{30}$$

where it follows that the LMS update for the filter coefficients reads:

$$\mathbf{w}_{n+1} = \mathbf{w}_n + \mu_{\mathrm{w}} e[n]\mathbf{s}_n^*. \tag{31}$$

Similarly, we differentiate the cost function with respect to the spline control points $\mathbf{q}_n$, yielding

$$\frac{\partial J(\mathbf{w}_n, \mathbf{q}_n, \mathbf{h}_n)}{\partial \mathbf{q}_n^*} = \frac{\partial e[n]e^*[n]}{\partial \mathbf{q}_n^*} \tag{32}$$

$$= e^*[n]\frac{\partial e[n]}{\partial \mathbf{q}_n^*} + e[n]\frac{\partial e^*[n]}{\partial \mathbf{q}_n^*} \tag{33}$$

$$= 0 - e[n]\frac{\partial \mathbf{w}_n^H \mathbf{s}_n^*}{\partial \mathbf{q}_n^*} \tag{34}$$

$$= -e[n]\frac{\partial \mathbf{s}_n^H}{\partial \mathbf{q}_n^*}\mathbf{w}_n^* \tag{35}$$

$$= -e[n]\frac{\partial \mathbf{r}_n^H}{\partial \mathbf{q}_n^*}\mathbf{w}_n^*. \tag{36}$$

Assuming a low rate of change for $\mathbf{q}_n$, that is $\mathbf{q}_{n+\sigma} \approx \mathbf{q}_n$ for values of σ in the order of the filter length M, we can write

$$\frac{\partial \mathbf{r}_n^H}{\partial \mathbf{q}_n^*} = \frac{\partial}{\partial \mathbf{q}_n^*}\begin{bmatrix} r_n^* & \cdots & r_{n-M+1}^* \end{bmatrix}^T \tag{37}$$

$$= \begin{bmatrix} x^*[n]\boldsymbol{\Psi}_n^* & \cdots & x^*[n-M+1]\boldsymbol{\Psi}_{n-M+1}^* \end{bmatrix}^T \tag{38}$$

$$= \boldsymbol{\Sigma}_n^T \mathbf{X}_n^*. \tag{39}$$

Thus, the LMS update for the spline control points is

$$\mathbf{q}_{n+1} = \mathbf{q}_n + \mu_{\mathrm{q}} e[n]\boldsymbol{\Sigma}_n^T \mathbf{X}_n^* \mathbf{w}_n^*. \tag{40}$$

The derivation of the learning rule of the additional TX impairment modeling coefficient vector $\mathbf{h}_n$ follows similar logic as the spline control points. The same reasoning may be used to show that

$$\frac{\partial J(\mathbf{w}_n, \mathbf{q}_n, \mathbf{h}_n)}{\partial \mathbf{h}_n^*} = -e[n]\frac{\partial \mathbf{t}_n^H}{\partial \mathbf{h}_n^*}\mathbf{w}_n^*. \tag{41}$$

Assuming slow adaption for $\mathbf{h}_n$ as well ($\mathbf{h}_{n+\sigma} \approx \mathbf{h}_n$), we can write

$$\frac{\partial \mathbf{t}_n^H}{\partial \mathbf{h}_n^*} = \frac{\partial}{\partial \mathbf{h}_n^*}\begin{bmatrix} t_n^* & \cdots & t_{n-M+1}^* \end{bmatrix}^T \tag{42}$$

$$= \begin{bmatrix} \boldsymbol{\phi}_n^* & \cdots & \boldsymbol{\phi}_{n-M+1}^* \end{bmatrix}^T \tag{43}$$

$$= \boldsymbol{\Phi}_n \tag{44}$$

Finally, we arrive at the LMS update for the coefficients of the additional TX impairments:

$$\mathbf{h}_{n+1} = \mathbf{h}_n + \mu_{\mathrm{h}} e[n]\boldsymbol{\Phi}_n \mathbf{w}_n^*. \tag{45}$$

REFERENCES

[1] A. Sabharwal, P. Schniter, D. Guo, D. W. Bliss, S. Rangarajan, and R. Wichman, "In-band full-duplex wireless: Challenges and opportunities," *IEEE J. Sel. Areas Commun.*, vol. 32, no. 9, pp. 1637–1652, Sep. 2014.

[2] D. Korpi, "Full-duplex wireless: Self-interference modeling, digital cancellation, and system studies," Ph.D. dissertation, Tampere University of Technology, Dec. 2017.

[3] K. E. Kolodziej, B. T. Perry, and J. S. Herd, "In-band full-duplex technology: Techniques and systems survey," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 7, pp. 3025–3041, July 2019.

[4] B. Paul, A. R. Chiriyath, and D. W. Bliss, "Survey of RF communications and sensing convergence research," *IEEE Access*, vol. 5, pp. 252–270, 2017.

[5] C. Baquero Barneto, T. Riihonen, M. Turunen, L. Anttila, M. Fleischer, K. Stadius, J. Ryynänen, and M. Valkama, "Full-duplex OFDM radar with LTE and 5G NR waveforms: Challenges, solutions, and measurements," *IEEE Transactions on Microwave Theory and Techniques*, vol. 67, no. 10, 2019.

[6] S. A. Hassani, V. Lampu, K. Parashar, L. Anttila, A. Bourdoux, B. v. Liempd, M. Valkama, F. Horlin, and S. Pollin, "In-band full-duplex radar-communication system," *IEEE Systems Journal*, pp. 1–12, 2020.

[7] B. Kaufman, J. Lilleberg, and B. Aazhang, "An analog baseband approach for designing full-duplex radios," in *Proc. 47th Asilomar Conference on Signals, Systems and Computers*, Nov. 2013, pp. 987–991.

[8] D. Bharadia, E. McMilin, and S. Katti, "Full duplex radios," in *Proc. SIGCOMM'13*, Aug. 2013, pp. 375–386.

[9] T. Huusari, Y.-S. Choi, P. Liikkanen, D. Korpi, S. Talwar, and M. Valkama, "Wideband self-adaptive RF cancellation circuit for full-duplex radio: Operating principle and measurements," in *Proc. 81st IEEE Vehicular Technology Conference (VTC Spring)*, May 2015.

[10] K. E. Kolodziej, J. G. McMichael, and B. T. Perry, "Multitap RF canceller for in-band full-duplex wireless communications," *IEEE Transactions on Wireless Communications*, vol. 15, no. 6, pp. 4321–4334, Jun. 2016.

[11] M. Duarte, C. Dick, and A. Sabharwal, "Experiment-driven characterization of full-duplex wireless systems," *IEEE Trans. Wireless Commun.*, vol. 11, no. 12, pp. 4296–4307, Dec. 2012.

[12] A. Kiayani, M. Waheed, L. Anttila, M. Abdelaziz, D. Korpi, V. Syrjälä, M. Kosunen, K. Stadius, J. Ryynänen, and M. Valkama, "Adaptive nonlinear RF cancellation for improved isolation in simultaneous transmit-receive systems," *IEEE Transactions on Microwave Theory and Techniques*, vol. 66, no. 5, pp. 2299–2312, May 2018.

[13] S. Li and R. D. Murch, "An investigation into baseband techniques for single-channel full-duplex wireless communication systems," *IEEE Transactions on Wireless Communications*, vol. 13, no. 9, pp. 4794–4806, Sep. 2014.

[14] D. Korpi, T. Riihonen, V. Syrjälä, L. Anttila, M. Valkama, and R. Wichman, "Full-duplex transceiver system calculations: Analysis of ADC and linearity challenges," *IEEE Transactions on Wireless Communications*, vol. 13, no. 7, pp. 3821–3836, Jul. 2014.

[15] D. Korpi, L. Anttila, V. Syrjälä, and M. Valkama, "Widely linear digital self-interference cancellation in direct-conversion full-duplex transceiver," *IEEE Journal on Selected Areas in Communications*, vol. 32, no. 9, pp. 1674–1687, Sep. 2014.

[16] A. Balatsoukas-Stimming, A. Austin, P. Belanovic, and A. Burg, "Baseband and RF hardware impairments in full-duplex wireless systems: Experimental characterisation and suppression," *EURASIP Journal on Wireless Communications and Networking*, vol. 2015, no. 142, May 2015.

[17] L. Anttila, D. Korpi, V. Syrjälä, and M. Valkama, "Cancellation of power amplifier induced nonlinear self-interference in full-duplex transceivers," in *Proc. 47th Asilomar Conference on Signals, Systems and Computers (ASILOMAR)*, Nov. 2013, pp. 1193–1198.

[18] D. Korpi, S. Venkatasubramanian, T. Riihonen, L. Anttila, S. Otewa, C. Icheln, K. Haneda, S. Tretyakov, M. Valkama, and R. Wichman, "Advanced self-interference cancellation and multiantenna techniques for full-duplex radios," in *Proc. 47th Asilomar Conference on Signals, Systems and Computers (ASILOMAR)*, Nov. 2013, pp. 3–8.

[19] E. Ahmed, A. M. Eltawil, and A. Sabharwal, "Self-interference cancellation with nonlinear distortion suppression for full-duplex systems," in *Proc. 47th Asilomar Conference on Signals, Systems and Computers (ASILOMAR)*, Nov. 2013, pp. 1199–1203.

[20] A. C. M. Austin, A. Balatsoukas-Stimming, and A. Burg, "Digital predistortion of power amplifier non-linearities for full-duplex transceivers," in *Proc. 17th IEEE International Workshop on Signal Processing Advances in Wireless Communications (SPAWC)*, Jul. 2016.

[21] M. S. Sim, M. Chung, D. K. Kim, and C. B. Chae, "Low-complexity nonlinear self-interference cancellation for full-duplex radios," in *Proc. IEEE Globecom Workshops*, Dec. 2016.

[22] F. H. Gregorio, G. J. González, J. Cousseau, T. Riihonen, and R. Wichman, "Predistortion for power amplifier ainearization in full-duplex transceivers without extra RF chain," in *IEEE International Conference on Acoustics, Speech and Signal Processing (ICASSP)*, Mar. 2017, pp. 6563–6567.

[23] D. Korpi, L. Anttila, and M. Valkama, "Nonlinear self-interference cancellation in MIMO full-duplex transceivers under crosstalk," *EURASIP Journal on Wireless Communications and Networking*, vol. 2017, no. 1, p. 24, Feb. 2017.

[24] D. W. Bliss and Y. Rong, "Full-duplex self-interference mitigation performance in nonlinear channels," in *Proc. 48th Asilomar Conference on Signals, Systems and Computers (ASILOMAR)*, Nov. 2014, pp. 1696–1700.

[25] Y. Kurzo, A. Burg, and A. Balatsoukas-Stimming, "Design and implementation of a neural network aided self-interference cancellation scheme for full-duplex radios," in *2018 52nd Asilomar Conference on Signals, Systems, and Computers*, Oct 2018, pp. 589–593.

[26] P. Pascual Campo, D. Korpi, L. Anttila, and M. Valkama, "Nonlinear digital cancellation in full-duplex devices using spline-based Hammerstein model," in *Proc. IEEE Globecom Workshops*, Dec. 2018.

[27] M. Sakai, H. Lin, and K. Yamashita, "Adaptive cancellation of self-interference in full-duplex wireless with transmitter IQ imbalance," in *Proc. IEEE Global Communications Conference (GLOBECOM)*, Dec. 2014, pp. 3220–3224.

[28] D. Korpi, J. Tamminen, M. Turunen, T. Huusari, Y.-S. Choi, L. Anttila, S. Talwar, and M. Valkama, "Full-duplex mobile device: Pushing the limits," *IEEE Commun. Mag.*, vol. 54, no. 9, pp. 80–87, Sep. 2016.

[29] M. Chung, M. S. Sim, J. Kim, D. K. Kim, and C. b. Chae, "Prototyping real-time full duplex radios," *IEEE Commun. Mag.*, vol. 53, no. 9, pp. 56–63, Sep. 2015.

[30] M. Jain, J. I. Choi, T. Kim, D. Bharadia, S. Seth, K. Srinivasan, P. Levis, S. Katti, and P. Sinha, "Practical, real-time, full duplex wireless," in *Proc. 17th Annual International Conference on Mobile computing and Networking (MobiCom)*, Sep. 2011, pp. 301–312.

[31] D. Korpi, M. AghababaeeTafreshi, M. Piililä, L. Anttila, and M. Valkama, "Advanced architectures for self-interference cancellation in full-duplex radios: Algorithms and measurements," in *Proc. 50th Asilomar Conference on Signals, Systems and Computers (ASILOMAR)*, Nov. 2016, pp. 1553–1557.

[32] F. J. Soriano-Irigaray, J. S. Fernandez-Prat, F. J. Lopez-Martinez, E. Martos-Naya, O. Cobos-Morales, and J. T. Entrambasaguas, "Adaptive self-interference cancellation for full duplex radio: Analytical model and experimental validation," *IEEE Access*, vol. 6, pp. 65 018–65 026, 2018.

[33] H. Li, J. Van Kerrebrouck, O. Caytan, H. Rogier, J. Bauwelinck, P. Demeester, and G. Torfs, "Self-interference cancellation enabling high-throughput short-reach wireless full-duplex communication," *IEEE Transactions on Wireless Communications*, vol. 17, no. 10, pp. 6475–6486, Oct 2018.

[34] L. Anttila, M. Valkama, and M. Renfors, "Circularity-based I/Q imbalance compensation in wideband direct-conversion receivers," *IEEE Transactions on Vehicular Technology*, vol. 57, no. 4, pp. 2099–2113, Jul. 2008.

[35] F. M. Ghannouchi and O. Hammi, "Behavioral modeling and predistortion," *IEEE Microwave Magazine*, vol. 10, no. 7, pp. 52–64, Dec. 2009.

[36] S. Mirabbasi and K. Martin, "Classical and modern receiver architectures," *IEEE Communications Magazine*, vol. 38, no. 11, pp. 132–139, Nov. 2000.

[37] B. Razavi, "Design considerations for direct-conversion receivers," *IEEE Transactions on Circuits and Systems II: Analog and Digital Signal Processing*, vol. 44, no. 6, pp. 428–435, Jun. 1997.

[38] M. Valkama, A. Shahed hagh ghadam, L. Anttila, and M. Renfors, "Advanced digital signal processing techniques for compensation of nonlinear distortion in wideband multicarrier radio receivers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 6, pp. 2356–2366, June 2006.

[39] S. Haykin, *Adaptive Filter Theory*, 3rd ed. Prentice Hall, 1996.

[40] M. AghababaeeTafreshi, M. Koskela, D. Korpi, P. Jääskeläinen, M. Valkama, and J. Takala, "Software defined radio implementation of adaptive nonlinear digital self-interference cancellation for mobile inband full-duplex radio," in *Proc. IEEE Global Conference on Signal and Information Processing (GlobalSIP)*, Dec. 2016, pp. 733–737.

[41] M. Scarpiniti, D. Comminiello, R. Parisi, and A. Uncini, "Nonlinear spline adaptive filtering," *Signal Processing*, vol. 93, no. 4, pp. 772–783, 2013.

[42] ——, "Hammerstein uniform cubic spline adaptive filters: Learning and convergence properties," *Signal Processing*, vol. 100, pp. 112–123, 2014.

[43] H. Vogt, G. Enzner, and A. Sezgin, "State-space adaptive nonlinear self-interference cancellation for full-duplex communication," *IEEE Transactions on Signal Processing*, vol. 67, no. 11, pp. 2810–2825, 2019.

[44] Z. Li, Y. Xia, W. Pei, K. Wang, and D. P. Mandic, "An augmented nonlinear LMS for digital self-interference cancellation in full-duplex direct-conversion transceivers," *IEEE Transactions on Signal Processing*, vol. 66, no. 15, pp. 4065–4078, 2018.

[45] D. Korpi, Y.-S. Choi, T. Huusari, S. Anttila, L. Talwar, and M. Valkama, "Adaptive nonlinear digital self-interference cancellation for mobile inband full-duplex radio: Algorithms and RF measurements," in *Proc. IEEE Global Communications Conference (GLOBECOM)*, Dec. 2015.

[46] A. Filip, "Linear approximations to $\sqrt{\mathrm{x}^2 + \mathrm{y}^2}$ having equiripple error characteristics," *IEEE Transactions on Audio and Electroacoustics*, vol. 21, no. 6, pp. 554–556, December 1973.

[47] J. Tamminen, M. Turunen, D. Korpi, T. Huusari, Y.-S. Choi, S. Talwar, and M. Valkama, "Digitally-controlled RF self-interference canceller for full-duplex radios," in *Proc. 24th European Signal Processing Conference (EUSIPCO)*, Aug. 2016, pp. 783–787.

[48] W. Chung, D. Hong, R. Wichman, and T. Riihonen, "Interference cancellation architecture for full-duplex system with GFDM signaling," in *Proc. 24th European Signal Processing Conference (EUSIPCO)*, Aug. 2016, pp. 788–792.

[49] C. De Boor, *A Practical Guide to Splines*. Springer-Verlag New York, 1978.

This article has been accepted for publication in a future issue of this journal, but has not been fully edited. Content may change prior to final publication. Citation information: DOI 10.1109/TWC.2020.3040226, IEEE Transactions on Wireless Communications

Lauri Anttila received the D.Sc. (Tech.) degree (with distinction) in 2011 from Tampere University of Technology (TUT), Finland. Since 2016, he has been a University Researcher at the Department of Electrical Engineering, Tampere University (formerly TUT). In 2016-2017, he was a Visiting Research Fellow at Aalto University, Finland. His research interests are in radio communications and signal processing, with a focus on the radio implementation challenges in systems such as 5G, full-duplex radio, and large-scale antenna systems.

Vesa Lampu received his B.Sc. degree in 2017 and M.Sc. degree in 2019 in electrical engineering from Tampere University, Finland. He has been working at the Department of Electrical Engineering of Tampere University (formerly TUT) since 2018, where he is currently pursuing a D.Sc. degree. His research focuses on energy efficient MIMO systems. He has also been involved in research on nonlinear system identification, with applications in full-duplex and digital predistortion techniques.

Seyed Ali Hassani obtained his B.Sc. degree in electrical engineering from Arak Azad University, Arak, Iran in 2008. He then worked as an R&D engineer in the industry to gain his professional experience. In 2014, he started M.Sc. in Information Technology - Signal Processing in Finland where he graduated with distinction from Tampere University of Technology, in 2016. Currently, he is a Ph.D. researcher at KU Leuven, focusing on Context-aware Ultra-reliable Networking. His main research interests are low-latency networks, radar signal processing and wireless in-band full-duplex communication.

Pablo Pascual Campo received his B.Sc. and M.Sc. degrees in Telecommunications and Electrical Engineering in 2016 and 2018, respectively, from Universidad Po-litécnica de Madrid, Madrid, Spain. He is currently pursuing his D.Sc. degree at Tampere University's Department of Electrical Engineering, Tampere, Finland. His research interests include digital predistortion, full-duplex systems and applications, and signal processing for wireless communications in the mmWave spectrum.

Dani Korpi received D.Sc. degree (Hons.) in electrical engineering from Tampere University of Technology (TUT), Finland, in 2017. Currently, he is a Senior Specialist with Nokia Bell Labs in Espoo, Finland. He received the best dissertation award of the year in TUT, as well as the Finnish Technical Sector's Award for the best doctoral dissertation of 2017. His research interests include inband full-duplex radios, machine learning for wireless communications, and beyond 5G radio systems.

Matias Turunen is currently pursuing the M.Sc. degree in electrical engineering at Tampere University (TAU), Tampere, Finland, while also working as a Research Assistant with the Department of Electrical Engineering at TAU. His current research interests include in-band full-duplex radios with an emphasis on analog RF cancellation, OFDM radar, and 5G New Radio systems.

Sofie Pollin obtained her PhD degree at KU Leuven with honors in 2006. From 2006-2008 she continued her research on wireless communication, energy-efficient networks, cross-layer design, coexistence and cognitive radio at UC Berkeley. In November 2008 she returned to imec to become a principal scientist in the green radio team. Currently, she is associate professor at the electrical engineering department at KU Leuven. Her research centers around Networked Systems that require networks that are ever more dense, heterogeneous, battery powered and spectrum constrained. Prof. Pollin is BAEF and Marie Curie fellow, and IEEE senior member.

Mikko Valkama received the D.Sc. (Tech.) degree (with honors) from Tampere University of Technology (TUT), Finland, in 2001. In 2003, he was a visiting post-doc research fellow with SDSU, San Diego, CA. Currently, he is a Full Professor and Department Head of Electrical Engineering at the newly formed Tampere University (TAU), Finland. His research interests include radio communications, radio localization, and radio-based sensing, with emphasis on 5G and beyond mobile radio networks.