A 2–5.5 GHz Beamsteering Receiver IC with 4-Element Vivaldi Antenna Array

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***Abstract*—In this paper we present a 4-element Vivaldi antenna array and beamsteering receiver IC for fifth-generation mobile network (5G) New Radio (NR). The implemented receiver utilizes a delay-based local-oscillator (LO) phase-shift technique for accurate beamsteering, and it exhibits 1 to 2.4 degree phase tuning capability for 2–5 GHz bandwidth accordingly. On-chip delay measurement is performed with pilot signal generation and delay estimation capable of 2 ps accuracy. The IC is fabricated on 28 nm CMOS technology, it occupies an area of 1.4 × 1.4 mm^2 including bonding pads and consumes 22.8 mW at 2 GHz for single receiver path operation. The receiver demonstrates wideband over-the-air reception with the prototype antennas.**

***Index Terms*—Beamsteering, calibration, delay estimator, delay line, local oscillator (LO) phase-shifting, phased arrays, RF front ends, self-test, sub-6 GHz, Vivaldi antenna, wideband receiver.**

I. Introduction

THE FIFTH-GENERATION mobile technology (5G) targets for higher data rates and lower latency through improved spectral usage of sub-6 GHz and millimeter-wave frequency ranges. 5G New Radio (NR) aims to enhance capacity of existing LTE networks by exploring unused sub-6 GHz bands through LTE-NR dual-connectivity [1]. Extensive use of phased arrays and beamsteering elevate signal-to-noise ratio and filter interference signals through spatial power combining. Beamsteering receiver architectures incorporate phased array antennas and receiver front-ends with phase-shifting capability to electronically steer the beam towards the desired direction. These beamsteering and array radio techniques for multiple-input multiple-output [2], [3], millimeter-wave transceivers [4]–[6] and W-band car radar [7] offer potential solutions for 5G networks.

Phase-shifting needed for beamsteering can be realized at radio frequency (RF), local oscillator (LO), baseband (BB) or in the digital domain. RF phase-shifting features low power consumption, compact design and relaxed linearity requirements for signal blocks following the summation node. However, RF phase-shifters introduce phase-dependent gain variation, it complicates gain calibration especially of large phased arrays that suffer from amplitude tapering. Baseband and digital phase-shifting offer highly flexible architecture leveraging advanced signal processing techniques. Despite their adaptability, wideband baseband and digital phase-shifters require high dynamic range for analog signal blocks and the digital interface preceding the summation node. In this work we focus on LO phase-shifting, shown in Fig. 1, because of its moderate area and power consumption, RF-signal path linearity, reduction of phase-shift dependent gain variation and relaxed dynamic range requirements for the digital interface.

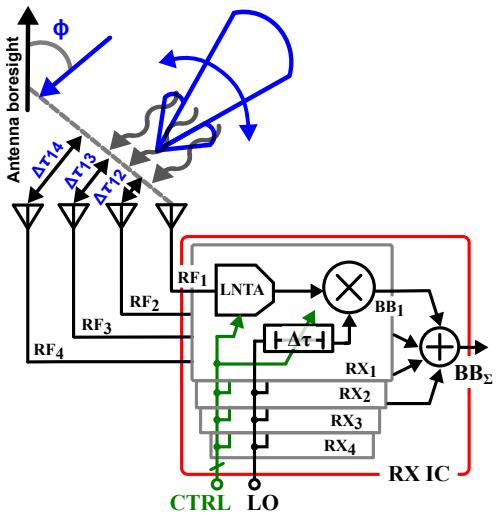

Fig. 1. Beamsteering receiver with LO phase-shifting and calibration.

This paper demonstrates beamsteering receiver with a 2×2 Vivaldi antenna array combined with receiver IC for 2–5.5 GHz frequency range. As 5G NR frequency range 1 (FR1) spans over several GHz, it requires an easily stackable wideband antenna element to realize a wideband array. Antenna array design is a trade-off between multiple factors including beamshape, bandwidth, size, and efficiency. Vivaldi antenna array is chosen because it provides wide operating frequency band and wide beamsteering range, is efficient, and can be conveniently realized on a PCB. We propose a delay-based LO phase shift technique to realize beam steering. The design is based on digitally-controlled delay lines, it inherently exhibits

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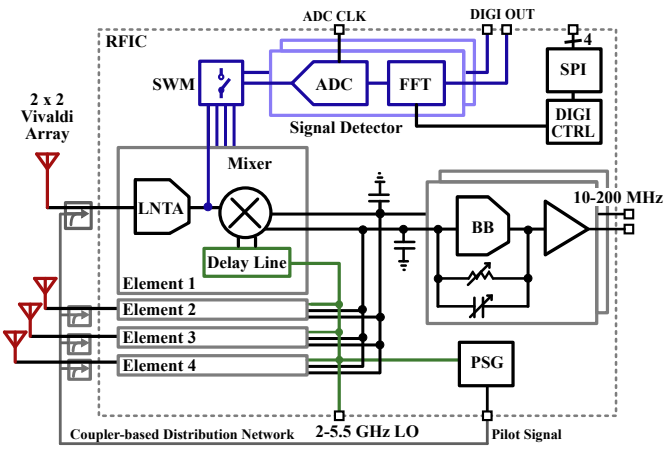

Fig. 2. 4-element beamsteering receiver architecture.

wide frequency operation as compared to RF phase-shift based approaches. The proposed LO phase shifting is power efficient, compact and passive-less, and therefore scalable.

In practical beamsteering implementations, concurrent signal paths are subject to gain and phase mismatches due to PVT variations in the receiver, which in turn skew the incident angle of the beam away from the desired direction. It is common practice to have gain and phase tuning capability in beamsteering receivers [8]–[13]. On-chip calibration methods typically incorporate a self-test apparatus based, for example, on coherent signal summation in the baseband [14], [15] and a tuning scheme for controlling individual channel gains or delays, or both. In this work, we present a delay estimation technique that utilizes an undersampling blocker detector hardware for measuring relative path delays in digital domain. It consists of Successive-Approximation-Register (SAR) ADC, and FFT computation blocks usually present in baseband signal processing in systems utilizing OFDM modulation. By moving the delay measurement into digital domain, the proposed estimator achieves time resolution of 2 picoseconds.

The rest of the paper is organized as follows. Section II discusses the implementation details of the antenna array and the receiver IC. Section III presents the experimental results for a single receiver path, delay estimator and the signal detector. Furthermore, the overall operation of the system is verified with over-the-air measurements. Finally, conclusions are drawn in section IV.

II. Receiver Implementation

Beamsteering operation can be demonstrated with different types of antennas, such as patch, dipole, spiral, or Vivaldi antennas. Patch and dipole-antennas are too narrowband, whereas spiral antennas can be difficult to implement on the same PCB as the IC. The chosen Vivaldi elements provide very wide usable frequency range and are suitable for picocell applications. A 2×2 antenna array configuration was chosen here instead of 1×4 configuration to enable beam steering in two orthogonal planes.

Fig. 2 presents the implemented prototype that includes direct down-conversion receiver paths and 4-element wideband Vivaldi antenna array. A single receiver path is composed of

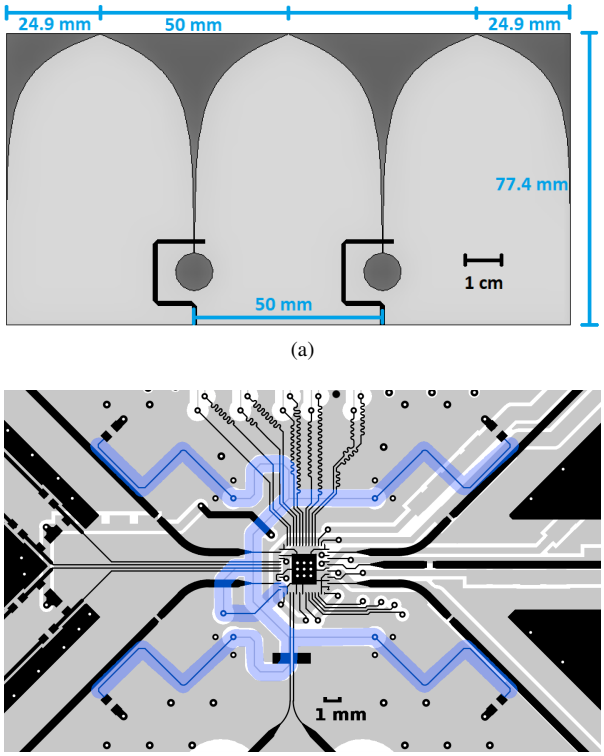

Fig. 3. (a) Layout of the antenna PCB, showing pair of Vivaldi antennas (middle) and extension parts for impedance matching (outer edges). (b) Layout of the test PCB, showing IC footprint (middle), pilot distribution network (in blue) and directional couplers at each receiver path (corners). Bottom layer copper shown in gray.

low-noise transconductance amplifier (LNTA), 4-phase passive mixers, and LO phase tuning elements to circumvent blocker-induced nonlinear distortion and receiver desensitization. The receiver front-end features a coil-less compact design with 3 dB gain tuning capability for gain mismatches. Furthermore, delay characterization between the antenna paths is implemented with sensing ADCs combined with FFT computations. Any of the four antennas can be connected to either of the sensing ADCs through a switch matrix amplifier. Delay characterization with the FFT units provides delay information for digitally-controlled beamsteering implemented with digitally-controlled delay lines [16], [17]. The proposed tuning structure provides wide frequency band for LO phase-shifting architecture. To realize the beamsteering, the received and phase-shifted signals are summed at the base-band filter input, supporting 200 MHz instantaneous signal bandwidth. The IC contains pilot signal generator for measuring gain and phase mismatches, distributed via coupler-based distribution network on the PCB.

A. Vivaldi Antenna Array

Fig. 3a shows one of two Vivaldi antenna PCBs [18]. The Vivaldi antenna element spacing is set to $\frac{\lambda}{2}$ at 3 GHz, corresponding to 5 cm. The outermost extended parts of the antenna array guarantee good matching below 3 GHz, where the opening of the Vivaldi antenna is small compared to the half-wavelength. On the other hand, the spacing of elements is small enough to enable operation at the highest frequency.

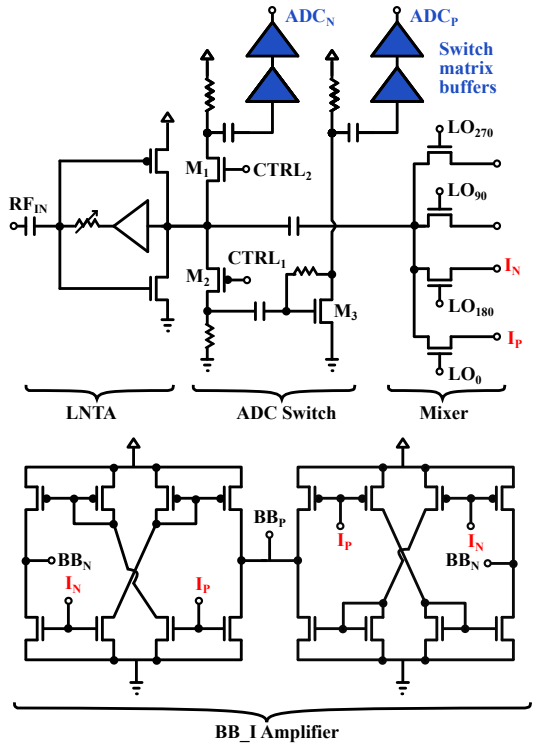

Fig. 4. Receiver front-end: LNTA, ADC switch, switch matrix buffers, mixer and baseband amplifier for I branch.

The presented prototype includes 2×2 antenna array with a coupler-based via $100\,\Omega$ tree type distribution network shown in Fig. 3b. The directional couplers, that are used to couple the pilot signal to the RF path, exhibit 25 dB coupling. The coupling is low enough not to attenuate the RF signal while being strong enough to enable amplitude and phase calibration with the pilot signal.

B. Front-End

The direct-conversion receiver, shown in Fig. 2, comprises of low-noise transconductance amplifier (LNTA) and in-phase and quadrature passive mixers that are driven by 25% duty-cycle LO clock signals, tunable baseband transconductance amplifier and common-source output buffer. The receiver front-end targets to provide $50\,\Omega$ matching for 2–5.5 GHz, compact design, moderate 5 dB amplification before signal summation and instantaneous bandwidth of 200 MHz. Current-mode architecture is adopted to circumvent voltage amplification before spatial filtering of blockers at the summation node [19] as strong blockers in nonlinear signal chain lead to receiver desensitization.

LNTA, presented in Fig. 4, is a complementary common-source amplifier with a tunable resistive feedback. The feedback voltage buffer is a complementary source follower added to improve the large-signal linearity of the amplifier [20]. The designed LNTA achieves wideband input matching, 5 dB noise figure, and 3 dB gain tuning capability with 1 dB step. ADC switches (M1, M2/M3) that interface the RF signal to delay estimator cause minimal deterioration to main LNTA amplifier performance.

The baseband amplifier (Fig. 4) is composed of two parallel operational transconductance amplifiers with common-mode feed-forward as in [21]. The resistor-capacitor feedback network, shown in (Fig. 2), exhibits 3–8 dB gain-bandwidth tuning capability.

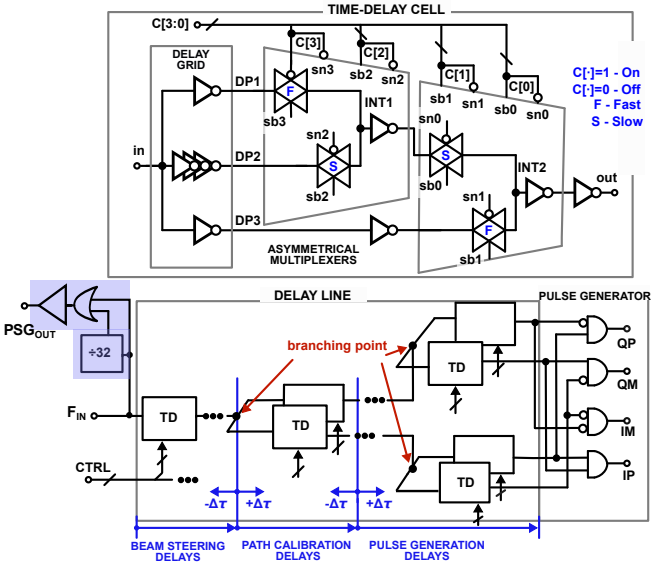

Fig. 5. Proposed time-delay cell, digitally controlled delay line and pilot signal generation (PSG).

C. LO Phase Tuning

The developed LO phase tuning block was designed to achieve phase-shifts down to 1 - 2.4° for 2–5 GHz along with 25% duty cycle 4-phase generation required for the mixer. Digitally-controlled delay lines can provide both tunable phase-shifts and 25% duty-cycle IQ signal generation without dividers or passive components, which facilitates the integration of a large number of beamsteering array elements. External LO reference is input buffered and distributed by a clock tree to all delay lines for multi-phase signal generation. Fig. 5 shows the block diagram of the proposed LO phase-shifter based on delay lines, capable of generating full LO cycle relative phase-shift, and 4-phase generation capability by means of a branched structure and control logic.

Branch points break the delay line into three functional domains: beamsteering, path calibration and pulse generation. Beamsteering section tunes the relative delay differences $\Delta\tau$ between receiver front-ends for beam rotation. Path calibration section can reduce the relative phase variation between different elements thanks to the wide delay-tuning capability of individual time-delay cells in the delay line. The combination of delay tuning paths provide 1–500 ps tuning range. Pulse generation section is responsible for 4-phase generation capability. The last section delay line is branched into four independent delay paths. The four distinct delays are combined using AND gates to generate four 25% duty cycle non-overlapping LO waveforms. The branched structure reduces the power consumption in comparison to architectures with frequency divider that require four fully independent signal paths, and imbalances between IQ signals [16].

Presented in Fig. 5, the designed time-delay (TD) cell generates coarse and fine delays between 1-45 ps respectively to cover the full range of the frequency band and realize fine-

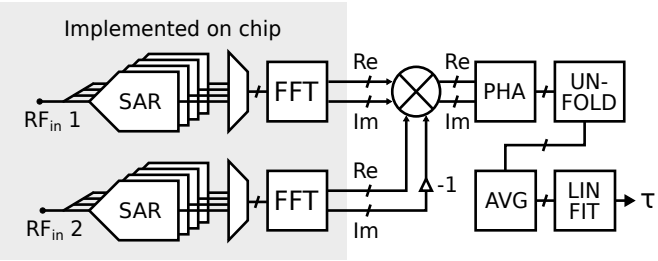

Fig. 6. Structure of implemented signal detector (grey box) showing the post-processing chain for Cross-PSD based delay estimation.

resolution beamsteering. The inverter-based delay grid provides three concurrent paths for coarse delays (15–45 ps). Fine delays (1-4 ps) are produced through current blending regime (nodes INT1 and INT2 in 5) in the asymmetrical multiplexers with slow and fast transmission gates [22]. The designed time-delay cell independently controls each transmission gate in the multiplexers to enable a particular delay using 4-bit control code, this design offers modular extensible architecture.

The reference LO signal (Fig. 5) generates a pilot signal for phase calibration of parallel receiver paths. The reference LO is multiplied, through an XOR operation, with its down-converted version (flip-flop based divide-by-32 circuit) to produce a frequency-shifted pilot signal for delay estimation or coherent detection with ∼100 MHz baseband signal. The pilot signal is amplified and delivered to receiver input via a 25 dB coupler on the PCB.

D. Delay Estimation

The delay estimator presented in Fig. 6 complements the functionality of the beamsteering front-end with delay detection capabilities. The designed apparatus utilizes two parallel sets of ADC and FFT units, where one set serves as a primary calibration channel and other as a zero-delay reference, enabling digitally-assisted self-test for estimation of relative delays between receiver paths. The on-chip section of delay estimator is an extension of our prior work [16] about the RF blocker detector, both of these functions can be performed with this hardware. The RF signal can be passed to the undersampling ADC output of any LNTA via specialized switch matrix amplifier, which consists of source followers and tri-state buffers (Fig. 4).

Each ADC block consists of four successive approximation registers (SAR) utilizing 7-bit split-capacitor array digital-to-analog converters.

Within one block, four SAR units are time-interleaved by a factor of four to allow wider undersampling bandwidth.

Radix-2^2 single delay feedback (SDF) architecture [23] was chosen for the on-chip FFT implementation. The exceptional property of this pipelined structure is the combination of radix-4 and radix-2 FFT architectures which gives best utilization of multipliers and adders while preserving the small memory footprint. The output of both pipelined FFT units is serialized and sent off-chip via LVDS drivers for consequent post-processing. Differing from self-test apparatus based on analog coherent signal summation [14], [15], we implement self-test by signal summation in the digital baseband. The implemented receiver system performs the delay estimation fully in the digital domain via cross-correlation of undersampled reference RF signals. This approach provides a 2 ps delay resolution through averaging of the spectral energy observed at the RF front-end.

For two deterministic discrete-time signals x and y, their cross-correlation product over a window of N samples is defined as

$$R_{xy}[m] = \sum_{n=0}^{N-1} x[n]y^*[n-m]. \tag{1}$$

The discrete Fourier transform of the cross-correlation is called the cross-power spectral density (cross-PSD), denoted as $C_{xy}(k) \triangleq \mathcal{F}(R_{xy}[m])$. If both signals x and y are N-periodic, the cross-PSD can be written as

$$C_{xy}(k) = X(k)Y^*(k), \tag{2}$$

where $X(k) = \mathcal{F}(x[n])$ and $Y(k) = \mathcal{F}(y[n])$. Assuming that y is a version of the signal x delayed by τ and attenuated by factor γ, i.e., $y[n] = \gamma x[n-\tau] \Leftrightarrow Y(k) = \gamma X(k)e^{-\frac{j2\pi k\tau}{N}}$, we obtain

$$C_{xy}(k) = |\gamma|\,|X(k)|^2\, e^{j\alpha(k)} \tag{3}$$

where $\alpha(k) = \frac{2\pi k\tau}{N} - \angle\gamma$.

From (3), a first-order polynomial can be fitted to the phase $\alpha(k)$ in order to estimate the delay τ between x and its delayed replica y. The corresponding post-processing chain is illustrated in Fig. 6. After undersampling by on-chip signal detector, complex multiplication of two signal spectra is performed in software, yielding the delay information embedded in the phase of the complex product. To reconstruct the undersampled RF signal, the corresponding frequency bins of the reference tone and its harmonics are selected and unfolded, producing a clean spectrum from which the Cross-PSD phase is extracted and averaged. The slope of the Cross-PSD phase is obtained from a linear model of the averaged data, yielding a coefficient directly proportional to the time delay between received signals.

III. Measurements

The Vivaldi antennas were implemented on FR4 PCB and the chip was fabricated in 28 nm FDSOI-CMOS process. Chip micrograph is depicted in Fig. 7. It occupies an area of 1.4x1.4 mm^2 including the bonding pads. Following experimental results, we verified the Vivaldi antenna array receiver with over-the-air measurements and further details of the functionality of the IC prototype.

A. Single Receiver Chain

Figure 8 shows the measured gain, noise figure (NF) and third-order input intercept point (IIP3) of one receiver path from 2 to 5.5 GHz. Other signal paths were disabled at the BB input by switching off LO distribution to passive mixers. The gain of the receiver path is 8 to 13 dB over the frequency range. Due to low voltage gain LNTA amplifier, the receiver achieves a high -7 dBm inband IIP3 with 47 and 67 MHz offset tones. The noise figure (NF) varies from 9 to 13 dB in the RF frequency range of interest with baseband bandwidth of 200 MHz.

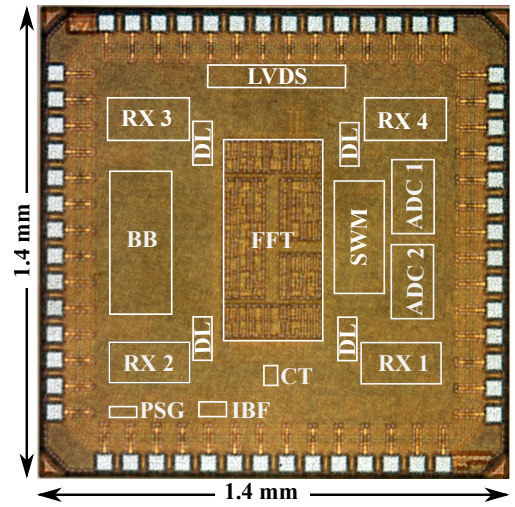

Fig. 7. Chip photograph of the 4-element beamsteering receiver.

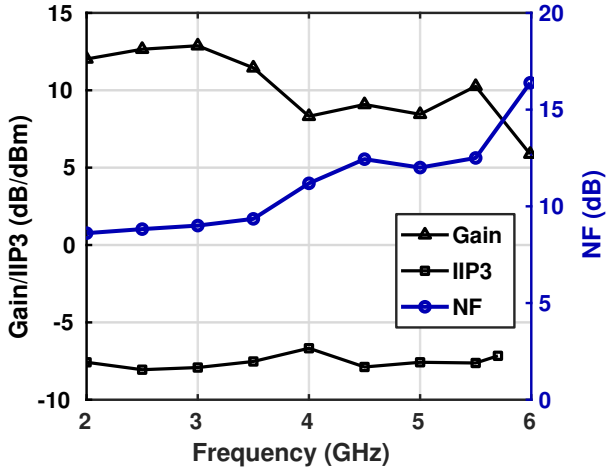

Fig. 8. Measured gain, NF and in-band IIP3 or one receiver path over the reception band.

B. Delay Estimator

The performance of complete delay estimator was then evaluated by feeding two antenna ports with identical RF signals of equal frequency and power while sweeping the phase offset of one signal. Vector signal generator is used to produce the test RF signals and the LVDS output is captured with a logic analyzer. The post-processing of FFT data was implemented in software and interfaced to the chip hardware as shown Fig. 6. Resulting Cross-PSD is averaged by a factor of 4096 in order to further suppress the measurement noise. The frequency of the reference signal is selected to be 2002.4060 MHz and the time-interleaving ADC sampling clock is set to 19.9936 MHz, providing coherent undersampling under constraint

$$f_{sig} = nF_s + \frac{kF_s}{N_{FFT}}, \tag{4}$$

where f_{sig} is the signal frequency and F_s is the sampling frequency, and integer parameters are chosen to be $n = 100$ and $k = 39$. $N_{FFT} = 256$ is defined by implementation. Thus, a particular FFT bin is allocated for each RF harmonic. A single measurement sequence provides a 256-point FFT

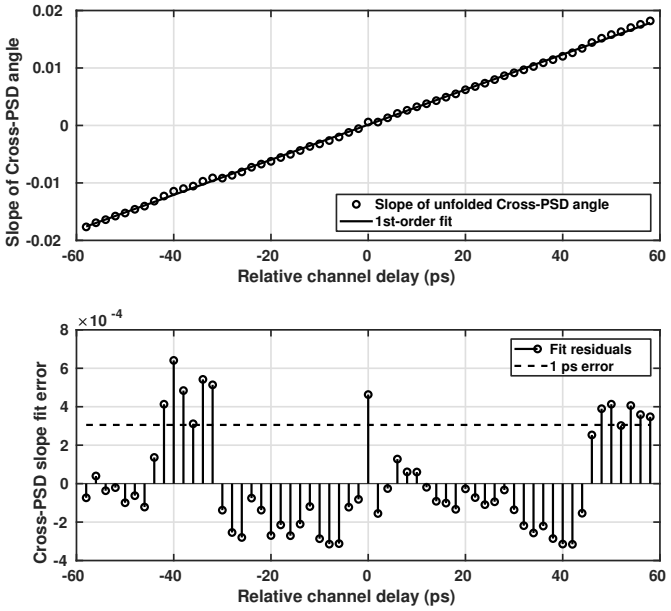

Fig. 9. Relative delay between RF paths extracted from Cross-PSD.

after averaging of 4096 consequent FFT windows, and takes approximately 5.24 ms to complete.

The delay estimator outputs for a linear delay sweep are shown in Fig. 9. The results show a linear dependency between the relative delay of test RF signals and the angle of Cross-PSD extracted by the undersampling delay estimator. The fit residual indicates an absolute error up to 2 ps, in relation to the fit slope per picosecond. Time delay of 2 ps corresponds to phase step of 1.44 degrees and 3.96 degrees for 2 GHz signal and 5.5 GHz signals accordingly.

The results demonstrate that the proposed undersampling estimator enables self-test capabilities for in-system characterization of RF front-end delays due to temperature, aging or process variations. The system is capable of high-precision measurements, enabling estimation of relative path delays from antenna to mixer input, which are typically within tens-of-picoseconds range for wide-band LNA implementations [13], [24]. Together with the proposed LO phase-tuning block described in Section II-C and external post-processing chain described in Section II-D, the proposed estimator can be incorporated into a closed-loop system for compensation of phase mismatches due to PVT variations and aging. The application of phase compensation is beyond the scope of this paper and will be considered in our future work.

C. Over-the-Air Measurements

The far-field beam patterns for the Vivaldi antenna array and the receiver prototype were measured in anechoic chamber. RF and LO signals for the measurements were produced with dual channel vector signal generator and the receiver baseband signal was measured with vector network analyzer.

The width of the main beam is determined by the angle between points where the power is reduced by 3 dB and known as half-power beamwidth (HPBW). Fig. 11 presents over-the-air measurement results for 2 GHz and 5 GHz in both E- and H-plane. Due to the wide frequency band, the far-field patterns

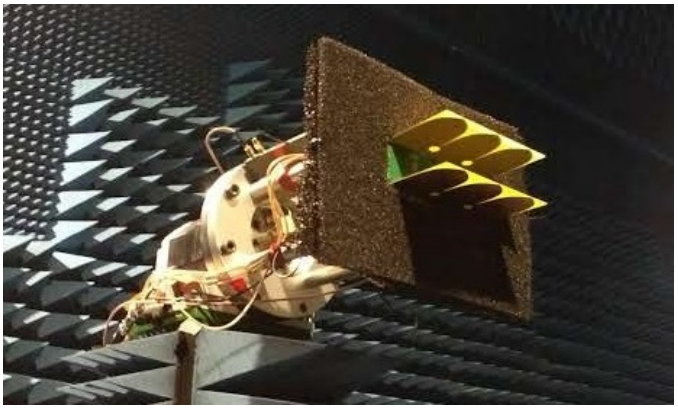

Fig. 10. Vivaldi antenna array with RF-IC attached to the rotator in the measurement chamber.

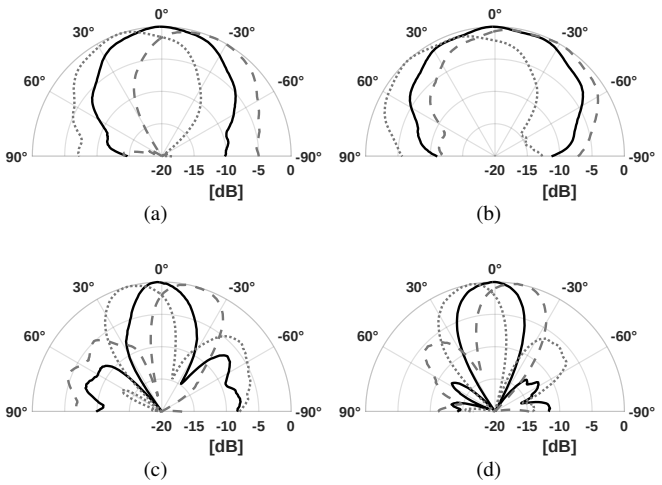

Fig. 11. Measured normalized far-field pattern at 2 GHz in E- (a) and H-plane (b) and at 5 GHz in E- (c) and H-plane (d). Forward beam in **solid black** and steered beams in **dotted** and **dashed gray**.

are not identical at all frequencies. The far-field pattern at 2 GHz have wide HPBW and beamsteering is demonstrated for approximately -30°, 0°, and 30°. HPBW becomes more narrow at 5 GHz and grating lobes appear. The beamsteering is demonstrated for approximately -13°, 0°, and 13°.

The over-the-air measurements demonstrate the logical beamsteering capability of the receiver prototype over a wide frequency range providing extensive coverage and suggesting improved capacity.

Table I compares the presented beamsteering receivers with its counterparts, the proposed design produces higher phase resolution with moderate power consumption. Moreover, this work demonstrates wide beamsteering capability with Vivaldi antenna array.

IV. Conclusion

We have presented a 2–5.5 GHz beamsteering receiver prototype including 4-element receiver IC and 2×2 array of Vivaldi antennas. Implemented in 28 nm CMOS, the prototype is capable of beamsteering with 1° – 2.4° phase tuning through the proposed delay-based LO phase shifter. The IC has pilot signal generator and signal detector for phase calibration. Implemented signal detector has been demonstrated to achieve picosecond accuracy for delay estimation. PCB assembly integrates the Vivaldi antenna array and coupler-based distribution network for calibration.

Our beamsteering receiver achieves a high -7 dBm IIP3, 8–13 dB gain and 9–13 dB NF with instantaneous baseband bandwidth of 200 MHz. A single receiver path consumes 22.8 mW at 2 GHz from 1V supply. The proposed delay-based LO generator is capable of wide frequency operation with 1° – 2.4° phase tuning capability, and the signal detector can estimate delays with 2 ps accuracy (1.44° at 2 GHz). Beamsteering has been demonstrated through over-the-air measurements in E- and H-plane for 2 and 5 GHz. Overall, this work demonstrated integrated antenna-IC wideband operation in sub-6 GHz range, accurate beamsteering, on-chip calibration and compact architecture to facilitate integration of large arrays for 5G FR1.

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TABLE I
COMPARISON WITH WIDEBAND BEAMSTEERING RECEIVERS OPERATING IN SUB-6 GHZ.

	This work	[25]	[26]	[27]
Frequency (GHz)	2-5.5	1-2.5	0.1 - 1.7	2-16
Antenna Type	**Vivaldi**	N/A	2×2	N/A
Number of Element	4	4	4	8
Phase-shifting	LO	Analog	Digital	Analog
min. Phase Step	**1°** - **2.4°**(1)	44 steps	6 bits	5 bits
Technology	28 nm CMOS	65 nm CMOS	65 nm CMOS	130 nm SiGe BiCMOS
1-Element Gain (dB)	8 - 13	12	41	N/A
1-Element Instant. BW (MHz)	200	30 - 300	N/A	N/A
1-Element CP (in-band)(dBm)	-19 – -15	-9	N/A	-14 – -17
1-Element IIP3(out-of-band)(dBm)	-4.5 – -1	5	11	N/A
1-Element Noise Figure (dB)	9 - 13	6	1.7 - 4.6	N/A
Power/Element (mW)	22.8 (2)	6.5 - 9	83(analog), 65(digital)(3)	250
Nominal Supply (V)	1-1.2	1	1.2	2.5

(1) @ 2 - 5 GHz (2) @ 2 GHz (3) @ 500 MHz

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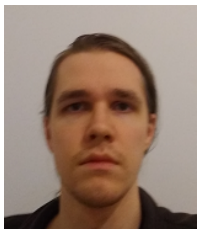

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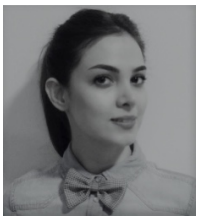

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