A Class-D Tri-Phasing CMOS Power Amplifier With an Extended Marchand-Balun Power Combiner

Mikko Martelius, *Member, IEEE*, Kari Stadius, *Member, IEEE*, Jerry Lemberg, Enrico Roverato, Tero Nieminen, Yury Antonov, *Member, IEEE*, Lauri Anttila, *Member, IEEE*, Mikko Valkama, *Senior Member, IEEE*, Marko Kosunen, *Member, IEEE*, and Jussi Ryynänen, *Senior Member, IEEE*

Abstract—This paper presents a power amplifier (PA) design, which consists of eight class-D PA units on a single 28-nm CMOS die and a coupled-line power combiner on printed circuit board (PCB). The PA utilizes tri-phasing modulation, which combines polar and outphasing components in a way that eliminates linearity-degrading effects of multilevel outphasing while maintaining the back-off efficiency. Each PA unit contains a cascoded output stage with a 3.6-V supply voltage, and multilevel operation is enabled by on/off logic circuitry. Our analysis shows that the choice of power-combiner type is vital for reducing PA supply and ground ripple and thus ensuring reliable operation. Accordingly, the power combiner is implemented with extended Marchand baluns, which consist of input transmission lines and coupled-line sections. Unlike the original Marchand balun, our new topology is feasible for implementation under the layout restrictions caused by the multiple-unit PA on a single die. Measurement results show the PA achieving a peak output power of 29.7 dBm with a 34.7% efficiency, and operation with aggregated LTE signals at 1.7-GHz carrier frequency is verified with bandwidths up to 100 MHz.

Index Terms—CMOS integrated circuits, Marchand balun, outphasing, power amplifiers, power combiners, radio transmitters, tri-phasing

I. INTRODUCTION

ONE of the long-standing challenges in designing radio transmitters and particularly their power amplifiers (PA) is achieving high power efficiency while fulfilling the increasingly demanding standards of linearity and spectral purity. Meanwhile, the development towards higher integration levels and system-on-chip (SoC) implementations, along with the decreasing supply voltages in the latest CMOS processes, leads to digital-intensive and time-based solutions being increasingly favored over analog circuit structures. As a result, there is growing interest in discarding the conventional Cartesian transmitter architecture in favor of alternative structures that employ constant-envelope PA input signals, which enables using highly efficient but nonlinear switch-mode PA classes. One technique for producing a phase and amplitude-modulated signal with such PAs is outphasing [1], [2], in which the output amplitude is modulated by altering the phase offset between two constant-envelope signal components. While outphasing transmitters can achieve a high peak efficiency, they tend to suffer from declining efficiency in power back-off.

A previously proposed solution for improving the back-off efficiency is multilevel outphasing, in which the output amplitude is modulated by discrete amplitude levels in addition to a phase offset [3], [4]. In our earlier work, we have developed new circuit solutions for phase modulators [5] and PAs [6] intended for highly integrated wideband multilevel outphasing transmitters [7]. However, while analyzing the characteristics of multilevel outphasing, we have found that amplitude-level transitions inherently cause discontinuities in the harmonic content of the combined output signal [8]. This appears in the spectrum as additional noise at a wide range of frequencies, including the signal band, where it can limit the achievable adjacent-channel leakage ratio (ACLR). As a solution to this trade-off between efficiency and linearity, we proposed a new transmitter architecture called tri-phasing [8]. This technique combines coarse-amplitude polar modulation with outphasing, resulting in smooth amplitude-level transitions and thus improved spectral performance, while simultaneously achieving a back-off efficiency equal to multilevel outphasing.

In this paper, we present a tri-phasing PA consisting of eight PA units on a single 28-nm CMOS die and a coupled-line power combiner on the printed circuit board (PCB). We place particular emphasis on the analysis and design of the power combiner, which has only been superficially described by our previous papers focusing on the integrated-circuit (IC) design details of the PA [9] and the complete transmitter included on the same die [10]. The combiner is an essential part of the system, largely defining the available carrier-frequency range and many characteristics of the wide spectrum. Furthermore, we present analysis demonstrating that the choice of power-combiner type is critical for PA reliability

M. Martelius (e-mail: mikko.martelius@corehw.com) and Y. Antonov were with the Department of Electronics and Nanoengineering, Aalto University. They are now with CoreHW, 00100 Helsinki, Finland.

K. Stadius, M. Kosunen, and J. Ryynänen are with the Department of Electronics and Nanoengineering, School of Electrical Engineering, Aalto University, 02150 Espoo, Finland

J. Lemberg was with the Department of Electronics and Nanoengineering, Aalto University. He is now with LG Electronics, 20520 Turku, Finland.

E. Roverato and T. Nieminen were with the Department of Electronics and Nanoengineering, Aalto University. They are now with CoreHW, 33720 Tampere, Finland.

L. Anttila and M. Valkama are with the Department of Electrical Engineering, Tampere University, 33720 Tampere, Finland.
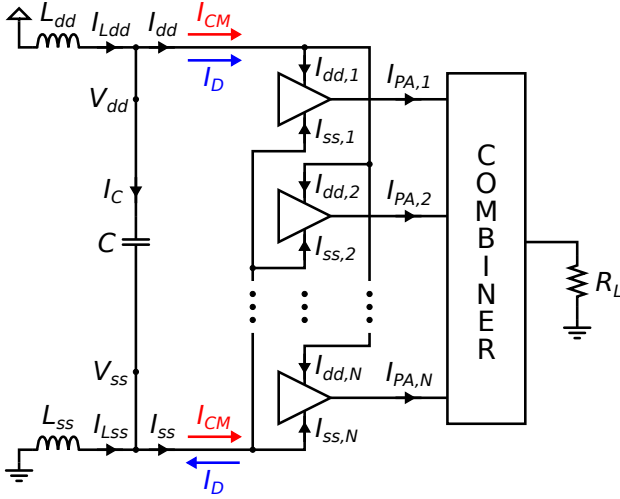
Fig. 1. Schematic of a generic wire-bonded multiple-unit PA system.

due to its effects on voltage ripple at the PA supply and ground. This consequential finding justifies our decision to discard the simple transmission-line combiner structure in favor of a notably more complex voltage-subtracting type.

The task of designing a coupled-line combiner is further complicated by the layout restrictions caused by all eight PA units being on a single die, rendering the Marchand balun [11] unfeasible in its original form. As a solution, we developed a new topology, the extended Marchand balun, which is extensively analyzed in this paper and forms the basis of the presented combiner design. In addition to the coupled lines, this structure features input lines of an arbitrary length, making it suitable for a wider range of applications.

This paper is organized as follows: Section II examines voltage ripple at the PA supply and ground, motivating our decision on the power-combiner type. Section III summarizes the structure and design of the integrated tri-phasing PA. In Section IV, we analyze the extended Marchand balun and present the power-combiner design. Measurement results are reported in Section V, and Section VI concludes the paper.

II. ANALYSIS OF PA SUPPLY AND GROUND RIPPLE

In order to explain why the power-combiner type is critically important for reliable PA operation, this section analyzes how the combiner affects voltage ripple at wire-bonded PA supply and ground nodes. The first part of this analysis examines the effects of common-mode and differential current at the supply and ground, and the second part establishes the dependency between these currents and the power-combiner type. While we apply the results to an outphasing-based PA, the analysis is equally valid for any fully integrated multiple-unit PA.

Fig. 1 depicts the schematic of a generic wire-bonded N-unit PA system, drawn to highlight the supply and ground currents. The bonding wires at the supply and ground nodes are modeled as inductors L_{dd} and L_{ss}, respectively, and the on-chip bypass capacitor C is included in order to stabilize the voltage difference between the internal supply and ground nodes ($V_{dd} - V_{ss}$). However, the capacitor cannot suppress common-mode ripple at V_{dd} and V_{ss}. Despite not affecting the

internal operation of the PA, such ripple can nonetheless cause problems in a larger context. First, in a SoC with multiple supply domains and separated ground nodes, the PA needs to operate with input signals that are not yet affected by the ripple. Consequently, the signals would be distorted by the PA input stages due to the relative fluctuation between the two ground levels. This could lead to suboptimal performance or even failure to produce a recognizable output. Second, the ripple would appear as an unwanted component in each PA-unit output voltage, and unless canceled by the combiner, this component would also degrade the combined output signal.

We begin the analysis by examining the currents shown in Fig. 1. Only the AC components of all voltages and currents are included in all following equations. At this point, each PA unit can be modeled as two current sources drawing $I_{dd,i}$ from the internal supply node (V_{dd}) and $I_{ss,i}$ from the internal ground (V_{ss}), while making no assumptions about the characteristics of these currents. Furthermore, to obtain more illustrative equations, we will use common-mode–differential notation for the total internal supply and ground currents

$$I_{dd} = \sum_{i=1}^{N} I_{dd,i} = I_{CM} + I_D \qquad (1)$$

$$I_{ss} = \sum_{i=1}^{N} I_{ss,i} = I_{CM} - I_D, \qquad (2)$$

as illustrated in Fig. 1. Similarly, we separate the effects of the difference between the bonding-wire inductances by expressing them as

$$L_{dd} = L + \Delta L \qquad (3)$$

$$L_{ss} = L - \Delta L. \qquad (4)$$

First, we can observe that the output current of the ith PA unit is

$$I_{PA,i} = I_{dd,i} + I_{ss,i}, \qquad (5)$$

assuming that its input current is negligible. Thus, the sum of all PA-unit output currents is

$$\sum_{i=1}^{N} I_{PA,i} = I_{dd} + I_{ss} = 2I_{CM}. \qquad (6)$$

This helps to describe some of the factors that affect the common-mode and differential current components. As (6) shows, I_{CM} is directly defined by the sum of PA-unit output currents. Those currents depend partly on the characteristics of the power combiner, as will be shown in a later part of this analysis. On the other hand, I_D represents the current that flows through the PA units from supply to ground or vice versa. This current does not interact with the combiner and is thus primarily determined by the PA units themselves.

With straightforward circuit analysis, the capacitor and bonding-wire currents can be solved as

$$I_C = \frac{2\omega^2 C}{1 - 2\omega^2 LC}(\Delta L I_{CM} + L I_D) \qquad (7)$$

$$I_{Ldd} = I_{CM}\left(1 + \frac{2\omega^2 \Delta LC}{1 - 2\omega^2 LC}\right) + \frac{I_D}{1 - 2\omega^2 LC} \qquad (8)$$

$$I_{Lss} = I_{CM}\left(1 - \frac{2\omega^2 \Delta LC}{1 - 2\omega^2 LC}\right) - \frac{I_D}{1 - 2\omega^2 LC} \quad (9)$$

From these results, we can derive the supply and ground voltage ripple. By using the common-mode–differential notation

$$V_{dd} = V_{CM} + V_D \quad (10)$$

$$V_{ss} = V_{CM} - V_D, \quad (11)$$

the voltage components are expressed as

$$V_{CM} = -j\omega\left[I_{CM}\left(L + \Delta L\frac{2\omega^2 \Delta LC}{1 - 2\omega^2 LC}\right) + \frac{\Delta LI_D}{1 - 2\omega^2 LC}\right] \quad (12)$$

$$V_D = -j\omega\frac{\Delta LI_{CM} + LI_D}{1 - 2\omega^2 LC}. \quad (13)$$

In the general case shown in (12) and (13), both V_{CM} and V_D include components induced by both I_{CM} and I_D. Increasing C suppresses the entirety of V_D and the part of V_{CM} that is caused by I_D, provided that $C > 1/(2\omega^2 L)$. Thus, the part of V_{CM} induced by I_{CM} is the most difficult component to reduce. This component could theoretically be eliminated at a single frequency by choosing

$$C = \frac{L}{2\omega^2(L^2 - (\Delta L)^2)}, \quad (14)$$

but given that ΔL is typically much smaller than L, this value of C would be severely insufficient for suppressing the other voltage components.

Based on the above analysis, we conclude that in practice, a large value of I_{CM} prevents effective suppression of supply and ground voltage ripple. Given that I_{CM} is defined by the sum of PA-unit output currents, it might seem that reducing this current always leads to a lower output power. However, this is only true if all PA-unit output voltages are equal in both amplitude and phase, which does not need to be the case. For example, with two fully differential voltages, the output power only depends on the difference between the currents, not the sum. Thus, with a well-informed choice of power-combiner type, it may be possible to design a system in which the PA-unit output currents are fully or mostly differential, leading to a small I_{CM} even with a high output power.

In order to further examine the dependency between power-combiner type and I_{CM}, we will next derive the sum of PA-unit output currents with two common types of combiners: a voltage-adding transmission-line combiner [12]–[15] and a voltage-subtracting Marchand balun [11], [16]–[20]. This analysis uses arbitrary combiner input voltages and thus applies to all methods of signal construction.

The generic schematic of a voltage-adding transmission-line power combiner with N inputs is shown in Fig. 2. Assuming lossless transmission lines, the combiner input currents (i.e. PA output currents) are defined by the ABCD parameters of a quarter-wave line:

$$\begin{bmatrix} V_i \\ I_i \end{bmatrix} = \begin{bmatrix} 0 & jZ_0 \\ j\frac{1}{Z_0} & 0 \end{bmatrix}\begin{bmatrix} V_{out} \\ I_{o,i} \end{bmatrix}, \quad i = 1, 2, \ldots, N \quad (15)$$

We can derive from the sum of combiner input currents that

$$I_{CM} = \frac{1}{2}\sum_{i=1}^{N} I_i = j\frac{N}{2Z_0}V_{out}. \quad (16)$$
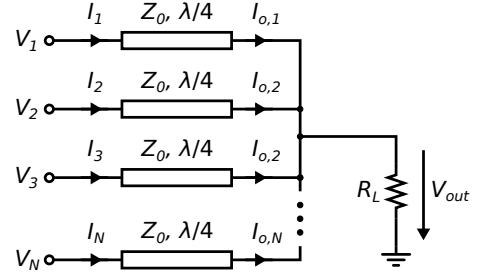

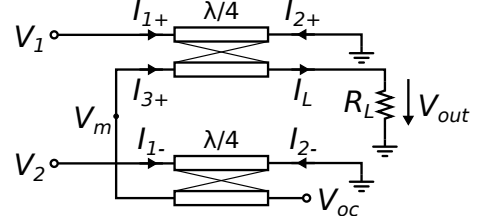Fig. 2. Generic schematic of a voltage-adding transmission-line power combiner.

Fig. 3. Schematic of a Marchand balun.

When applied to (12), this means that the common-mode voltage ripple contains a component that is proportional to the combiner output voltage and cannot be suppressed by a large on-chip capacitance. Thus, when using this type of combiner, the aforementioned ripple component can only be reduced by decreasing the output power.

The Marchand balun, depicted in Fig. 3, is a typical coupled-line structure used in voltage-subtracting power combiners. It consists of two pairs of coupled quarter-wave lines, which are here assumed to be lossless and symmetrical. The Y-parameter equations describing the operation, derived from the general-case equations of coupled lines [21], can be expressed as

$$\begin{bmatrix} I_{1+} \\ I_{2+} \\ I_{3+} \\ -I_L \end{bmatrix} = \begin{bmatrix} 0 & Y_{12} & 0 & Y_{14} \\ Y_{12} & 0 & Y_{14} & 0 \\ 0 & Y_{14} & 0 & Y_{12} \\ Y_{14} & 0 & Y_{12} & 0 \end{bmatrix}\begin{bmatrix} V_1 \\ 0 \\ V_m \\ V_{out} \end{bmatrix} \quad (17)$$

$$\begin{bmatrix} I_{1-} \\ I_{2-} \\ -I_{3+} \\ 0 \end{bmatrix} = \begin{bmatrix} 0 & Y_{12} & 0 & Y_{14} \\ Y_{12} & 0 & Y_{14} & 0 \\ 0 & Y_{14} & 0 & Y_{12} \\ Y_{14} & 0 & Y_{12} & 0 \end{bmatrix}\begin{bmatrix} V_2 \\ 0 \\ V_m \\ V_{oc} \end{bmatrix}. \quad (18)$$

First, we can determine the relation between V_{out} and V_{oc} from the two equations for I_{3+}:

$$V_{oc} = -V_{out}. \quad (19)$$

Based on this, we find that regardless of the input voltages, the balun input currents are

$$I_{1+} = Y_{14}V_{out} \quad (20)$$

$$I_{1-} = -Y_{14}V_{out}. \quad (21)$$

These equations show that the balun input currents are differential and their sum is always zero, even when the input

voltages are not fully differential. Consequently, I_{CM} is inherently zero with such combiners, and all remaining voltage-ripple components in (12) and (13) can be indefinitely reduced by increasing the on-chip capacitance. Finally, from (20) and (21), we can derive the total input power of the balun

$$P_{in} = \frac{1}{2} \operatorname{Re}[V_1(Y_{14}V_{out})^*] + \frac{1}{2} \operatorname{Re}[V_2(-Y_{14}V_{out})^*] \quad (22)$$

$$P_{in} = \frac{1}{2} \operatorname{Re}\left[(V_1 - V_2)(Y_{14}V_{out})^*\right]. \quad (23)$$

This shows that despite the zero sum of input currents, the input power is not zero, provided that $V_{out} \neq 0$ and $(V_1 - V_2) \neq 0$. These results apply to combiners consisting of any number of Marchand baluns whose output currents are summed at a single load.

We summarize the key findings of this section as follows:

- The sum of PA-unit output currents defines the common-mode current at the PA supply and ground, which in turn causes the supply and ground ripple component that is not suppressed by on-chip capacitors. Thus, this sum of currents must be minimized to avoid excessive ripple.
- The PA units can produce a large output power with a small or even zero sum of output currents, if the currents are mostly or fully differential. This indicates that the sum of currents can be minimized by using a voltage-subtracting power combiner that produces the maximum output power with differential voltages and currents.

To support this suggestion, we derived the input currents of two common types of transmission-line-based combiners with arbitrary input voltages, with the following results:

- With a voltage-adding transmission-line combiner, the sum of currents is proportional to the output voltage.
- With a voltage-subtracting Marchand-balun combiner, the currents are always differential, which means that their sum is zero regardless of output power.

Thus, we conclude that by utilizing a Marchand-balun-based power combiner and a sufficiently large on-chip bypass capacitor, we can minimize all components of the PA supply and ground ripple without needing to limit the output power.

III. TRI-PHASING POWER AMPLIFIER

This section presents an overview of the integrated tri-phasing PA. The PA greatly informs the combiner design, and these circuits can be more meaningfully characterized as a single entity, which is why this paper covers the entire PA system. However, instead of repeating all previously published details of the tri-phasing concept [8] or the PA design [9], this section only summarizes the main points to provide context for the combiner work and the measurement results.

The designed tri-phasing PA system, as shown by the block diagram in Fig. 4(a), contains one always-active outphasing PA pair and a polar section of three PA pairs. The phase-modulated input signals are

$$S_0(t) = \cos(\omega t + \phi(t)) \quad (24)$$

$$S_1(t) = \cos(\omega t + \phi(t) + \theta(t)) \quad (25)$$

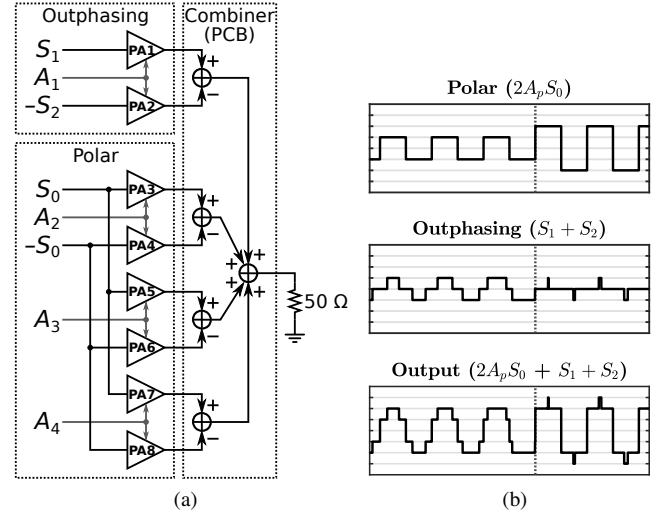$$S_2(t) = \cos(\omega t + \phi(t) - \theta(t)), \quad (26)$$

Fig. 4. (a) Block diagram of the designed tri-phasing PA system. (b) Time-domain example of the tri-phasing signal composition, showing a coarse-level transition (vertical line) with no instantaneous change the combined waveform.
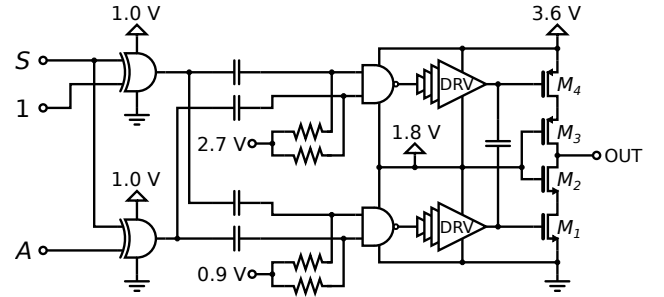

Fig. 5. Simplified schematic of the PA unit.

where $\phi(t)$ is the polar phase and $\theta(t)$ is the outphasing angle. The polar section creates coarse-level amplitude modulation, and the outphasing pair covers the gaps between coarse levels with high resolution. The signal composition is illustrated by example waveforms in Fig. 4(b), where A_p is the number of active polar PA pairs. The waveforms illustrate the main advantage of tri-phasing: the smooth transitions between coarse levels, with no harmonic discontinuities. As demonstrated by analysis and simulations in [8], this can potentially improve the spectral performance compared to multilevel outphasing, while maintaining the back-off efficiency benefit.

Fig. 5 depicts the schematic of a single PA unit featuring a cascoded class-D output stage. In order to switch the output stage on and off according to the signal A, the XOR and NAND gates construct the desired signals in both "on" and "off" states in a manner that allows constant bias voltages [6], [9]. This solution enables multilevel operation with a relatively high 3.6-V supply voltage in an integrated system, where all PA input signals are generated in the 1.0-V domain.

The output-stage transistor sizes were chosen such that their on-resistances do not cause significant output-voltage saturation at the peak output power. Building on our analysis in [6], this means that the vast majority of power loss in the PA units occurs due to the charging and discharging of the relatively large drain–source capacitances of the output
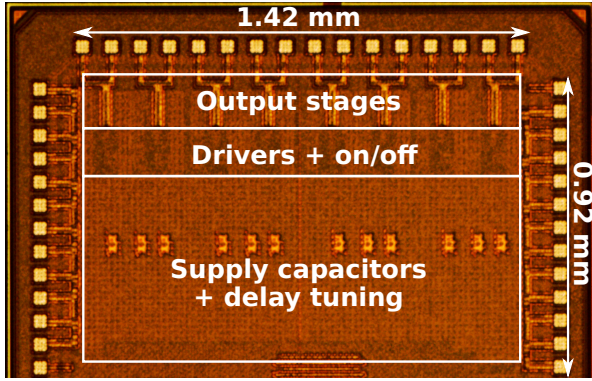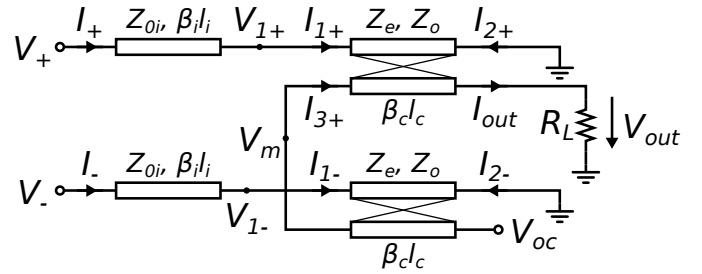
Fig. 6. Die micrograph of the PA.

Fig. 7. Schematic of the extended Marchand balun. The load resistor is shown for illustrative purposes only and can be replaced by any non-open circuit.

transistors. By assuming that other losses are negligible, we can thus derive a simple efficiency model in which the loss in each active PA unit, P_{loss}, is constant and independent of output power. According to this model, the total efficiency is

$$\eta = \frac{P_{out}}{P_{out} + 2(A_p + 1)P_{loss}}, \tag{27}$$

which is equal between tri-phasing and multilevel outphasing at any value of P_{out}.

The PA was implemented in 28-nm CMOS as an integrated part of the tri-phasing transmitter presented in [10]. Fig. 6 shows the die micrograph of the PA. The depicted die area, excluding pads, is 1.31 mm^2, of which the PA units occupy 0.44 mm^2. Each of the eight PA-unit outputs is connected to two bonding pads, which are directly wire-bonded to the power-combiner inputs on the PCB. This configuration causes the main restriction on the combiner layout, requiring its inputs to be located within a relatively small area near the die.

IV. EXTENDED MARCHAND-BALUN POWER COMBINER

This section presents analysis and design of the coupled-line power combiner, implemented as part of the tri-phasing PA. In this system, the combiner sets the limit for the range of carrier frequencies, which is why we chose to realize the combiner on the PCB. This arrangement enables using the same IC in different products by only changing the PCB, saving the expenses of fabricating several variants of the IC.

Isolating combiners, such as the Wilkinson combiner [22], are are beneficial for linearity but inherently lossy at back-off and thus discarded. Among non-isolating combiners, one of the simplest types to realize on PCB is the voltage-adding transmission-line combiner shown in Fig. 2, which is often accompanied by Chireix compensation for improved back-off efficiency [12]–[15]. However, we concluded in Section II that using such a combiner with a relatively high-power wire-bonded PA may cause excessive voltage ripple at supply and ground, which can degrade the PA performance or even inhibit proper operation. Thus, we chose to design a voltage-subtracting coupled-line combiner, which can also improve the output spectrum by canceling undesired common-mode signal components [23]. Voltage-subtracting transformer combiners have rarely been implemented on PCB [24], and due to their

typical shape, designing the layout for eight inputs connected to a single IC would be difficult. In contrast, coupled lines are long but narrow, which enables placing several of them in a relatively narrow area. Therefore, we chose the Marchand balun, a widely used coupled-line structure, as the basis of our combiner development.

As mentioned in Section III, the integrated PA necessitates locating all combiner inputs within a narrow area. More-over, the bonding wires are inevitably part of the combiner, functionally resembling short transmission lines. Under these circumstances, the Marchand balun in its original form (Fig. 3) would be difficult to implement. Therefore, we introduce the extended Marchand balun, shown in Fig. 7, which performs the same basic function while containing arbitrarily long input lines before the coupled-line section. The input lines can thus be utilized to increase line spacing, which reduces unwanted coupling and creates sufficient space for DC-block capacitors. By including the input lines, we introduce a degree of freedom in designing the balun, which will reduce the limitations of layout design and thus expand the range of potential applications. The coupled-line length is reduced in a way that resembles the previously presented method of compensating for a connecting line between the two coupled-line sections [25]–[27]. However, the inclusion of the input lines is a distinct concept that addresses different practical needs, and it has not been thoroughly analyzed in earlier publications.

A. Analysis of the Extended Marchand Balun

In a voltage-subtracting power combiner with multiple pairs of inputs, the purpose of a balun is to produce an output current that is proportional to the difference of its two input voltages and independent of the output voltage. Thus, the output currents can be summed by connecting all balun outputs to a single load resistor. In this section, we analyze the operation of a single extended Marchand balun, and derive the rules by which it needs to be designed.

Fig. 7 shows the schematic of the extended Marchand balun. The original Marchand balun can be considered a special case of this circuit, in which the line lengths in radians are $\beta_i l_i = 0$ and $\beta_c l_c = \pi/2$, where $\beta = 2\pi/\lambda$. In this case, the current in any port of the quarter-wavelength coupled lines is defined by the voltages at the opposite end of the lines. Therefore, the zero current at the open circuit (V_{oc}) consists of components induced by V_- and V_m, which must cancel each other, resulting in a V_m that is proportional to $-V_-$. V_+
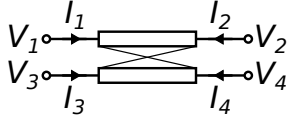
Fig. 8. Coupled transmission lines as a four-port network.

and V_m affect the output current in the same proportion as V_- and V_m affect the zero current, and thus I_{out} is proportional to $V_+ - V_-$.

When input lines with non-zero length are included, quarter-wavelength coupled lines no longer result in the desired operation, and therefore the circuit is analyzed with general line lengths. Now I_{out} depends not only on $V_{1+} - V_{1-}$ but also on $I_{1+} - I_{1-}$, both of which are affected by input voltages and input currents. The goal in designing the balun is to choose line lengths so that the effect of $I_\pm$ on $V_{1\pm}$ and the effect of $I_\pm$ on $I_{1\pm}$ cancel each other in the output current, resulting in I_{out} depending only on $V_+ - V_-$.

The dependencies between the voltages and currents at both ends of a pair of coupled transmission lines, as shown in Fig. 8, are described by the Y-parameter equation

$$\begin{bmatrix} I_1 \\ I_2 \\ I_3 \\ I_4 \end{bmatrix} = \begin{bmatrix} Y_{11,c} & Y_{12,c} & Y_{13,c} & Y_{14,c} \\ Y_{21,c} & Y_{22,c} & Y_{23,c} & Y_{24,c} \\ Y_{31,c} & Y_{32,c} & Y_{33,c} & Y_{34,c} \\ Y_{41,c} & Y_{42,c} & Y_{43,c} & Y_{44,c} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \\ V_3 \\ V_4 \end{bmatrix}. \tag{28}$$

The derivation of the Y-parameters of a generic coupled-line pair has been presented in [21] and will not be repeated here. For simplicity, the following analysis assumes TEM transmission lines, while the implemented lines operate in quasi-TEM mode. In addition, the input lines are assumed to be lossless. As such, the exact results may be slightly different from the realistic case, but the principles still apply.

The operation of the extended balun is described by two Y-parameter equations, both related to one input line and one pair of coupled lines:

$$\begin{bmatrix} I_+ \\ I_{2+} \\ I_{3+} \\ -I_{out} \end{bmatrix} = \begin{bmatrix} Y_{11,e} & Y_{12,e} & Y_{13,e} & Y_{14,e} \\ Y_{21,e} & Y_{22,e} & Y_{23,e} & Y_{24,e} \\ Y_{31,e} & Y_{32,e} & Y_{33,e} & Y_{34,e} \\ Y_{41,e} & Y_{42,e} & Y_{43,e} & Y_{44,e} \end{bmatrix} \begin{bmatrix} V_+ \\ 0 \\ V_m \\ V_{out} \end{bmatrix} \tag{29}$$

$$\begin{bmatrix} I_- \\ I_{2-} \\ -I_{3+} \\ 0 \end{bmatrix} = \begin{bmatrix} Y_{11,e} & Y_{12,e} & Y_{13,e} & Y_{14,e} \\ Y_{21,e} & Y_{22,e} & Y_{23,e} & Y_{24,e} \\ Y_{31,e} & Y_{32,e} & Y_{33,e} & Y_{34,e} \\ Y_{41,e} & Y_{42,e} & Y_{43,e} & Y_{44,e} \end{bmatrix} \begin{bmatrix} V_- \\ 0 \\ V_m \\ V_{oc} \end{bmatrix}. \tag{30}$$

The analysis is kept generally applicable by examining the output current and voltage as two independent variables instead of assuming any specific dependency between them, such as the load resistor (R_L) shown in Fig. 7. In order to derive these Y-parameters, we apply the coupled-line Y-parameters in (28) and the ABCD-parameters of the input line

$$\begin{bmatrix} V_{1\pm} \\ I_{1\pm} \end{bmatrix} = \begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix} \begin{bmatrix} V_\pm \\ I_\pm \end{bmatrix}, \tag{31}$$

$$\begin{bmatrix} A' & B' \\ C' & D' \end{bmatrix} = \begin{bmatrix} \cos(\beta_i l_i) & -jZ_{0i}\sin(\beta_i l_i) \\ -j\frac{1}{Z_{0i}}\sin(\beta_i l_i) & \cos(\beta_i l_i) \end{bmatrix}. \tag{32}$$

By solving the currents, taking into account that $Y_{mn,c} = Y_{nm,c}$, the following equations are obtained:

$$Y_{11,e} = \frac{A'Y_{11,c} - C'}{D' - B'Y_{11,c}} \tag{33}$$

$$Y_{1m,e} = Y_{m1,e} = \frac{Y_{1m,c}}{D' - B'Y_{11,c}}, \quad m = 2,3,4 \tag{34}$$

$$Y_{mn,e} = \frac{B'Y_{1n,c}Y_{m1,c}}{D' - B'Y_{11,c}} + Y_{mn,c}, \quad m,n = 2,3,4 \tag{35}$$

In general, $Y_{m1,c} = Y_{1m,c}$ [21], and thus (34) and (35) show that the Y-parameter matrix is symmetric, i.e. $Y_{mn,e} = Y_{nm,e}$. Hereafter, $Y_{mn,e}$ and $Y_{nm,e}$ are both expressed as $Y_{mn,e}$, where $m < n$.

Next, we derive the condition for the output current depending only on input voltages and not on input currents. From (29) and (30), we obtain the equation for the output current

$$I_{out} = \left(\frac{Y_{11,e}Y_{44,e}}{Y_{14,e}} - Y_{14,e} \right)(V_+ - V_-) - \frac{Y_{44,e}}{Y_{14,e}}(I_+ - I_-). \tag{36}$$

The coefficient of $I_+ - I_-$ has to be zero, which is true if $Y_{44,e} = 0$. By using (35) to express $Y_{44,e}$, this leads to the general condition for the input-line length

$$\tan(\beta_i l_i) = \frac{j}{Z_{0i}} \cdot \frac{Y_{44,c}}{Y_{11,c}Y_{44,c} - Y_{14,c}^2}. \tag{37}$$

Beginning from this point, the analysis is simplified by assuming that the coupled lines are lossless and symmetrical. Thus, the Y-parameters of the coupled lines are

$$Y_{11,c} = Y_{22,c} = Y_{33,c} = Y_{44,c} = -j\frac{(Y_e + Y_o)\cot(\beta_c l_c)}{2} \tag{38}$$

$$Y_{12,c} = Y_{21,c} = Y_{34,c} = Y_{43,c} = j\frac{Y_e + Y_o}{2\sin(\beta_c l_c)} \tag{39}$$

$$Y_{13,c} = Y_{24,c} = Y_{31,c} = Y_{42,c} = j\frac{(Y_o - Y_e)\cot(\beta_c l_c)}{2} \tag{40}$$

$$Y_{14,c} = Y_{23,c} = Y_{32,c} = Y_{41,c} = j\frac{Y_e - Y_o}{2\sin(\beta_c l_c)}, \tag{41}$$

and the condition of (37) can be written as a function of the coupled-line length and admittances with the help of (38) and (41):

$$\tan(\beta_i l_i) = \frac{2}{Z_{0i}} \cdot \frac{(Y_e + Y_o)\sin(\beta_c l_c)\cos(\beta_c l_c)}{(Y_e - Y_o)^2 - (Y_e + Y_o)^2\cos^2(\beta_c l_c)}. \tag{42}$$

Having defined that $Y_{44,e} = 0$, we will finally derive the Y-parameters of the whole balun, describing I_+, I_-, and $-I_{out}$ as functions of V_+, V_-, and V_{out}. This requires solving V_m and V_{oc} first. Two equations for V_m can be obtained, one from the sum of I_{3+} and $-I_{3+}$, and the other from the open-circuit zero current:

$$V_m = -\frac{Y_{13,e}}{2Y_{33,e}}(V_+ + V_-) - \frac{Y_{34,e}}{2Y_{33,e}}(V_{out} + V_{oc}), \tag{43}$$
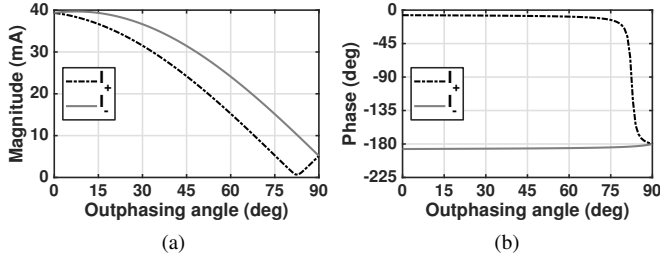
$$V_m = -\frac{Y_{14,e}}{Y_{34,e}}V_-. \tag{44}$$

Fig. 9. (a) Magnitude and (b) phase of the input currents of an ideal extended Marchand balun in outphasing.
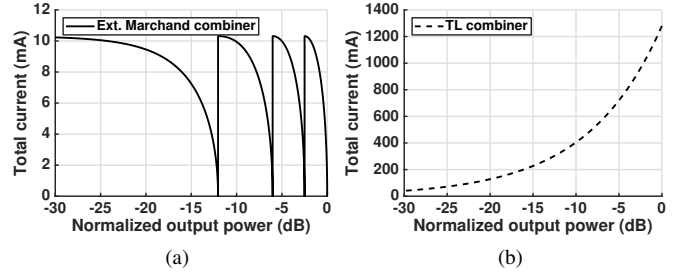

Fig. 10. The sum of combiner input currents in tri-phasing with (a) an extended Marchand-balun combiner; (b) a transmission-line combiner with equal output power.

From these two equations, we can derive

$$V_{oc} = -\frac{Y_{13,e}}{Y_{34,e}}V_+ + \frac{2Y_{14,e}Y_{33,e} - Y_{13,e}Y_{34,e}}{Y_{34,e}^2}V_- - V_{out}. \quad (45)$$

Now we can write the equations for I_+, I_-, and I_{out} in (29) and (30) substituting V_m from (44) and V_{oc} from (45). After deriving from (38), (39), (40), and (41) that $Y_{13,c}Y_{34,c} = Y_{14,c}Y_{33,c}$, the resulting Y-parameter equation simplifies into

$$\begin{bmatrix} I_+ \\ I_- \\ -I_{out} \end{bmatrix} = \begin{bmatrix} Y_{11,e} & -\frac{Y_{13,e}Y_{14,e}}{Y_{34,e}} & Y_{14,e} \\ -\frac{Y_{13,e}Y_{14,e}}{Y_{34,e}} & Y_{11,e} & -Y_{14,e} \\ Y_{14,e} & -Y_{14,e} & 0 \end{bmatrix} \begin{bmatrix} V_+ \\ V_- \\ V_{out} \end{bmatrix}. \quad (46)$$

This leads to the equations for the output current and the sum of the input currents:

$$I_{out} = -Y_{14,e}(V_+ - V_-) \quad (47)$$

$$I_+ + I_- = \left(Y_{11,e} - \frac{Y_{13,e}Y_{14,e}}{Y_{34,e}} \right)(V_+ + V_-). \quad (48)$$

In the special case that the input voltages are fully differential and the output is connected to a load resistance R_L, the impedance seen at each input is

$$Z_{in} = \frac{1}{Y_{11,e} + Y_{13,e}Y_{14,e}/Y_{34,e} - 2R_L Y_{14,e}^2}. \quad (49)$$

The output current is proportional to the difference between the input voltages, as seen in (47). This is the most important result of this analysis, as it demonstrates that the extended Marchand balun performs its intended function regardless of the input-line length as long as the condition of (42) is met. The input-current behavior is more complex and is therefore illustrated graphically in Fig. 9. In this example, $Z_{0i} = 50\ \Omega$, $\beta_i l_i = 28.5°$, $Z_e = 125\ \Omega$, $Z_o = 20\ \Omega$, $\beta_c l_c = 70°$, and $R_L = 50\ \Omega$. The magnitude of both input voltages is $V_{in} = 1$ V, and their phase difference is defined by the outphasing angle θ as

$$V_\pm = \pm V_{in}e^{\pm j\theta}. \quad (50)$$

The results show that the magnitudes of the input currents are not equal and their phase difference is not precisely 180°, unless the input voltages are purely differential, i.e. the outphasing angle is zero. This is the most notable effect caused by the additional input lines, compared to the conventional Marchand balun. The shorter the input lines are, the closer to differential the input currents become at all outphasing angles.
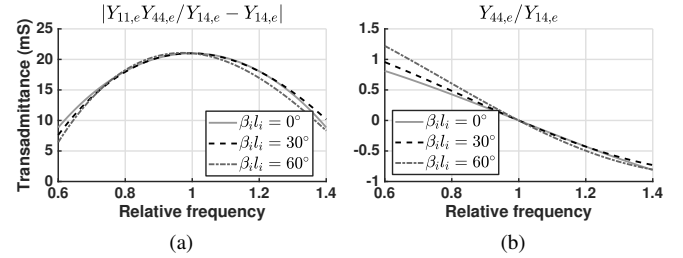

Fig. 11. Calculated balun characteristics as a function of frequency, based on (36): (a) input-voltage-to-output-current transadmittance; (b) input-current-to-output-current multiplier. The design-parameter values are shown in Table I.

The mismatch between currents does not directly affect the combiner output, but in a realistic case it can have an indirect effect by changing the PA-unit output voltages due to non-zero transistor on-resistances. However, the effect on linearity is minor, provided that the PA is designed to tolerate sufficiently large currents without significant effect on output voltage. As a general design guideline, an excessive input-line length should nonetheless be avoided, because the mismatch also leads to a non-zero sum of PA-unit output currents and thus common-mode supply and ground ripple.

Finally, Fig. 10(a) depicts the sum of combiner input currents in tri-phasing operation, using a power combiner consisting of four ideal extended Marchand baluns with previously stated example parameter values and input-voltage magnitudes. While individual input currents up to 157 mA appear, they are fully differential in the polar section and mostly differential in the outphasing pair, such that the sum of all currents is at most 10.3 mA. For comparison, Fig. 10(b) shows the equivalent results with a voltage-adding transmission-line combiner (Fig. 2) that produces equal output voltage. This comparison shows that although the total PA-unit output current is not precisely zero with extended Marchand baluns, its maximum value is only 0.8% of the maximum with an equivalent transmission-line combiner. Thus, with regard to supply and ground voltage ripple, the effect of the input lines is insignificant compared to the advantage over a voltage-adding combiner.

To analyze the frequency-dependent effects of the input lines, Fig. 11 compares the compares key characteristics of the extended Marchand balun, based on the output-current equation (36), in three example cases. Fig. 11(a) shows the

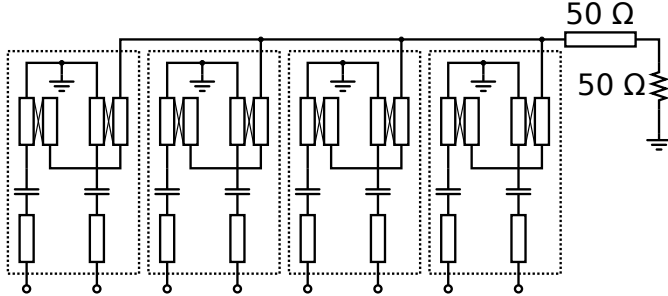| $\beta_i l_i$	$0°$	$30°$	$60°$
Z_{0i}	—	$39.8\ \Omega$	$42.0\ \Omega$
$\beta_c l_c$	$90°$	$72.4°$	$56.4°$

Fig. 12. Schematic of the designed power combiner.

(a)

(b)
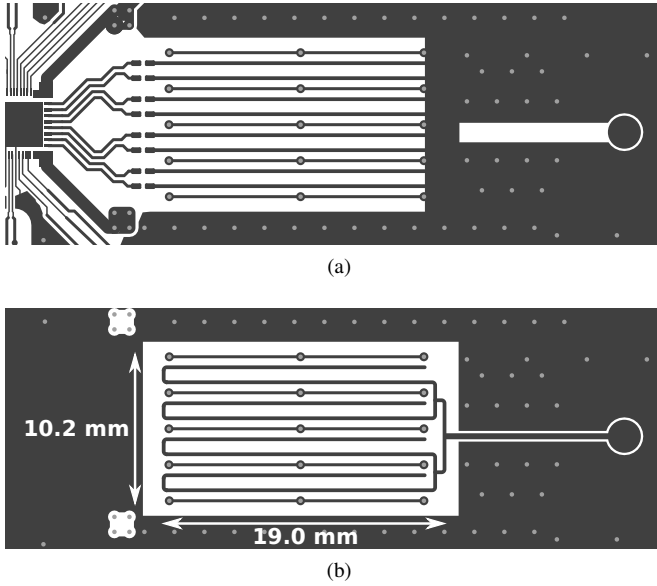
Fig. 13. Layout of the designed power combiner. (a) Top layer. (b) Middle layer.

(a)

(b)

Fig. 14. Photographs of (a) the power combiner on PCB; (b) the bonding wires connecting the PA to the combiner.
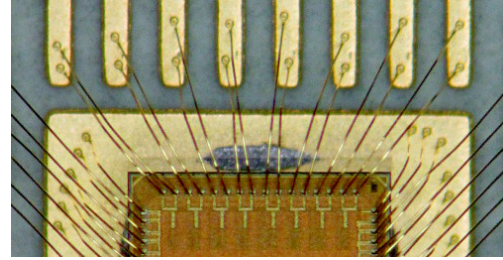
absolute value of the transadmittance of $(V_+ - V_-)$, and 11(b) depicts the multiplier of $(I_+ - I_-)$, both as a function of frequency. In all compared cases, $Z_e = 125\ \Omega$ and $Z_o = 20\ \Omega$. Three different values are chosen for $\beta_i l_i$, including $0°$ which corresponds to a conventional Marchand balun. The remaining variables are shown in Table I, defined such that $Y_{14,e}$ at the center frequency is equal between all cases. Based on the results in Fig. 11, the bandwidth effect of the input lines is minor, especially if the lines are relatively short.

B. Power-Combiner Design

Fig. 12 shows the schematic of the designed power combiner, which consists of four extended Marchand baluns with DC-block capacitors between the input lines and the coupled lines, and an output line with a 50-Ω characteristic impedance connected to the load. As indicated by the analysis of Section IV-A, the output-current behavior of each balun is

independent of its effective load impedance, which is 200 Ω at the peak output power. The layout is presented in Fig. 13, including the top metal layer in Fig. 13(a), the middle layer in Fig. 13(b), and the vias connecting these two layers to the ground plane below them (light-grey circles in both figures). The photograph of the fabricated power combiner on PCB is shown in Fig 14(a). The input lines are implemented as equally long microstrip lines with the middle layer used as the ground plane, and they are followed by surface-mounted 10-pF DC-block capacitors. The coupled-line section is realized with broadside-coupled lines, with coupling between the baluns reduced by ground lines between them on both layers. The balun outputs are connected together on the middle layer, and the combined signal is brought to the SMA connector with a coplanar waveguide.

The layout design was finalized using Momentum for electromagnetic (EM) simulations, and the resulting S-parameters were utilized to simulate the combiner together with the PA. The 16 bonding wires connecting the PA directly to the combiner, as shown in Fig. 14(b), were included in the simulations by using the model included in Keysight ADS [28], which considers the length and approximated shape of the wires and also models mutual coupling between them. The capacitors were modeled by S-parameters provided by the manufacturer. In the designed combiner, the input-line width and length are 0.2 mm and 7.0 mm, respectively, and the coupled-line width and length are 0.25 mm and 17.2 mm, respectively. To examine the effects of undesired coupling, the combiner was also simulated without the grounded lines between baluns, showing a maximum output-power mismatch of 0.38 dB between two baluns when ideal voltage sources are used. When the grounded lines are included, the mismatch is reduced to 0.17 dB.

In order to verify the theoretical design rules, we calculated the characteristic impedance of the input lines (45.1 Ω) with ADS and obtained the Y-parameters of a single coupled-line
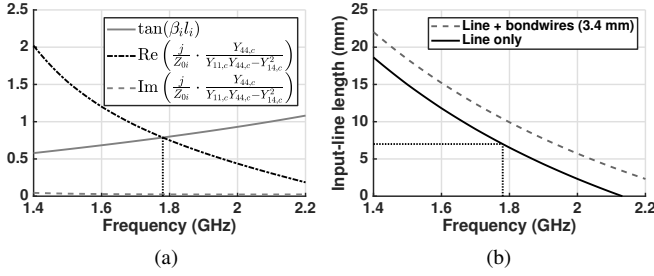
Fig. 15. (a) Verification of the theoretical design rules by comparing the left and right side of (37). (b) Calculated input-line length as a function of desired operation frequency.

Fig. 17. CW measurement results at 1.7 GHz: (a) efficiency as a function of output power; (b) output power as a function of outphasing angle.
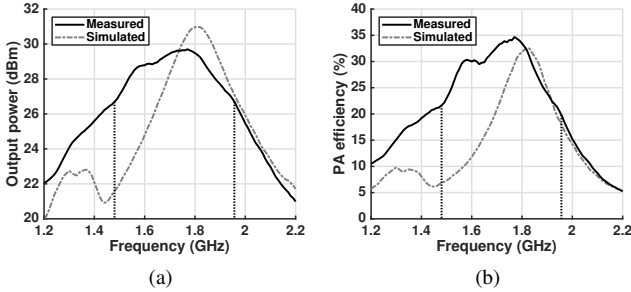

Fig. 16. CW measurements of (a) output power and (b) PA efficiency as a function of frequency.

pair with an EM simulation. With the help of the bonding-wire model, we also determined that the average bonding-wire pair can be approximated as a 3.4-mm extension of the input line. Based on these results and the actual line lengths, Fig. 15(a) compares the left and right sides of (37), which should be equal to ensure the desired operation. The imaginary part of the right side is negligible, and its real part crosses $\tan(\beta_i l_i)$ at 1.78 GHz, which is very close to the desired center frequency of 1.8 GHz. Fig. 15(b) depicts the calculated dependency between the input-line length and the operation frequency based on (37) and the simulated line characteristics. The dashed line shows the direct result of the calculation, and the solid line represents the actual line length without the 3.4-mm extension modeling the bonding wires.

V. Measurement Results

All measurements presented in this section were conducted using the on-chip phase modulators [10] to generate the PA input signals. The 1.0-V supply domain is shared with the modulators, which dominate the power consumption in that domain. Therefore, the power-consumption figures used in PA-efficiency calculations include all circuitry in the 1.8-V and 3.6-V supply domains but not the XOR gates. The presented output-power figures are measured at the combiner output.

A. Continuous-Wave Measurements

Fig. 16 depicts the peak output power and corresponding PA efficiency as a function of frequency in continuous-wave (CW) operation. The dependency between output power and frequency, shown in Fig. 16(a), demonstrates the power-combiner
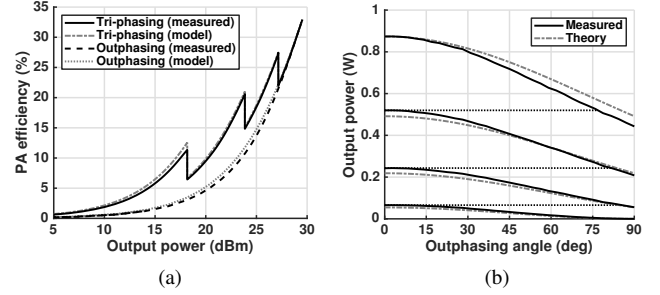
frequency response, which is the primary limiting factor for the operation frequency. The highest output power of 29.7 dBm (0.93 W) is achieved at 1.77 GHz, with an efficiency of 34.7%. This frequency matches well with the value calculated from (37) and illustrated in Fig. 15 (1.78 GHz). The 3-dB bandwidth is 476 MHz, ranging between 1.48–1.96 GHz (fractional bandwidth 28%) as illustrated by the dotted lines. Within this range, the PA efficiency remains above 19.8%, as shown by Fig. 16(b). The bandwidth is considerably wider than what was seen in simulations, while the peak output power is lower. Although this resembles the simulated effects of changing the characteristic impedances, we were not able to confirm such inaccuracies in the PCB manufacturing. On the other hand, the measured efficiency is higher than simulated. This is at least partly explained by power loss on IC, which in simulations is larger than the total measured power loss of the IC and the combiner. The measured insertion loss of the combiner without bonding wires is 1.0 dB at the optimal operation frequency. For subsequent measurements, we selected the center frequency of 1.7 GHz, which is near the middle of the 3-dB band.

Tri-phasing operation is demonstrated with CW signals in Fig. 17. The PA efficiency as a function of output power is depicted in Fig. 17(a), comparing the results in outphasing and tri-phasing modes. This figure shows that the back-off efficiency is significantly improved by tri-phasing, being at most 3.9 times the efficiency with outphasing at the same output power. The measurements are also compared to the results of the constant-loss efficiency model in (27), where the PA-unit power loss of 228 mW is chosen to match with the measured peak output power and efficiency. The model is unrelated to the simulation results shown in Fig. 16. Close agreement between the model and measured efficiency confirms the validity of the model and supports the claim of equal efficiency between tri-phasing and multilevel outphasing.

Fig. 17(b) depicts the output power as a function of the outphasing angle at all four coarse amplitude levels. The theoretical output power

$$P_{out} = \frac{P_{peak}}{16}(A_p + \cos\theta)^2 \qquad (51)$$

is also shown for comparison, with a peak value equal to measurements. The minimum output power of each coarse level is slightly lower than the maximum output power of the previous level, which means that there are no gaps in achievable levels of output power. This result differs from
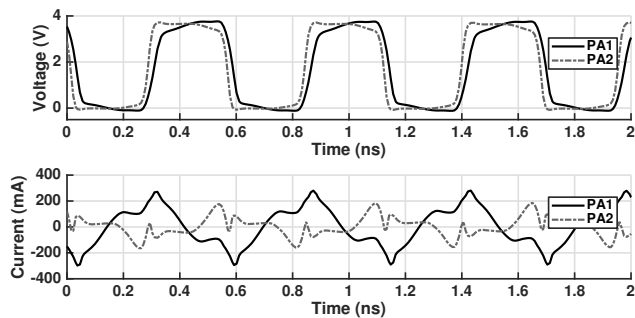
Fig. 18. Simulated output voltages and currents of the outphasing PA pair with $A_p = 3$, $\theta = 90°$, illustrating the cause of output-power discrepancy between theory and measurements.

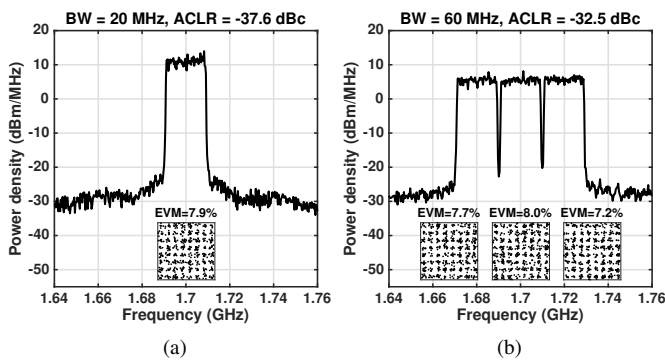Fig. 20. Measured spectrum and constellations of a 100-MHz aggregated LTE signal.

Fig. 19. Measured spectra and constellations of (a) 20-MHz LTE and (b) 60-MHz aggregated LTE signals. The PAPR has been limited to maximize output power and efficiency within the 8% EVM specification.

Fig. 21. Wide-span spectra of 20-MHz LTE and 60-MHz aggregated LTE signals.

(51), in which switching an additional polar PA pair on and changing the outphasing angle from 0 to 90° has no effect on the output power. The cause of this nonideality is illustrated by Fig. 18, which shows simulated waveforms of the outphasing PA pair with a 90° outphasing angle while all polar PA pairs are active. Due to the non-isolating power combiner, rising and falling edges under these circumstances occur when the output current is positive in one PA unit and negative in the other. This causes mismatch in rise and fall times, leading to a non-zero contribution to the combined output voltage and reduced output power. Nevertheless, the overlap between coarse levels is significantly smaller than in multilevel outphasing, where an outphasing angle of 90° always corresponds to a zero output power. Furthermore, this nonideality has been taken into account in the following measurements by performing signal-component separation according to the measured minimum and maximum output powers at each coarse level.

B. Measurements With Modulated Signals

The modulation performance of the PA was evaluated with 64-QAM LTE signals at a carrier frequency of 1.7 GHz. Apart from using measured CW power figures in signal-component separation, no digital predistortion was used in any of the presented measurements. Fig. 19 depicts the output spectra with 20-MHz LTE and 60-MHz aggregated LTE signals. In these measurements, the peak-to-average power ratio (PAPR) is reduced with iterative clipping and filtering, which increases
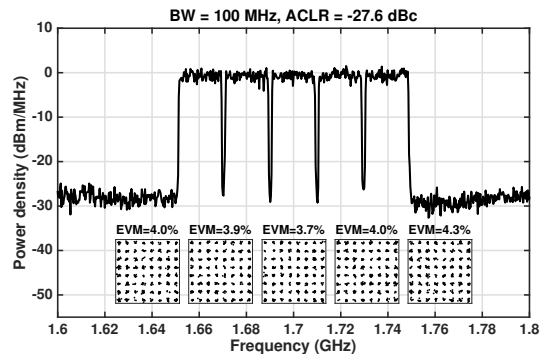
the output power with virtually no effect on the ACLR, while gradually increasing the EVM. To maximize output power and efficiency, we chose the lowest PAPR that maintains an EVM of at most 8% in each carrier, in accordance with LTE specifications. With a 20-MHz bandwidth, the PA achieves an average output power of 23.1 dBm with an efficiency of 15.3% and an ACLR of -37.6 dBc. By increasing the PAPR, an EVM of 2.4% is achieved at an output power of 21.4 dBm and an efficiency of 12.3%. With a 60-MHz bandwidth and an 8% EVM, the average output power is 22.4 dBm, the efficiency is 13.8%, and the ACLR is -32.5 dBc. The PA is also demonstrated to operate with a 100-MHz aggregated LTE signal in Fig. 20, with an output power of 19.0 dBm and an efficiency of 9.0%.

The wide-span spectra of the 20-MHz and 60-MHz signals are shown in Fig. 21. The small bumps on both sides of the signal band can be explained by supply ringing arising from sudden current-consumption changes at coarse amplitude-level transitions, which results in some unwanted amplitude modulation [30]. In future work, this ringing could be suppressed for example with damping legs [36]. Phase-modulator nonidealities are another source of noise near the signal band [10]. In PA simulations of a 20-MHz LTE signal without the aforementioned effects, tri-phasing improves the ACLR by 3.0 dB and reduces the noise at a 40-MHz offset from the signal band (ACLR2) by 9.1 dB compared to multilevel outphasing. Both spectra in Fig. 21 display a peak around 460 MHz, which is a local maximum in noise level caused by the power-combiner frequency response. While the second

TABLE II
COMPARISON OF MEASUREMENT RESULTS.

	JSSC [29]	JSSC [30]	ESSCIRC [31]	JSSC [32]	JSSC [33]	JSSC [34]	RFIC [35]	This work
CMOS tech. (nm)	32	45	45	90	65	55	65	**28**
Architecture	Outphasing	Multil. outph.	Outphasing	Polar	Polar	Polar	IQ cell sharing	**Tri-phasing**
PA class	Class D	Class D	Class E	Switched-cap.	Inv. class D	Inv. class D	Class G	**Class D**
Power combiner	On-chip	On-chip	PCB	—	On-chip	—	On-chip	**PCB**
Combiner loss (dB)	1.3^1	1.4^1	N/A	—	1.5^1	—	N/A	**1.0**
Peak P_{out} (dBm)	25.3	31.5	31.6	25.2	23.3	21.9	30.1	**29.7**
Peak efficiency (%)	35	27	43.7	45	43	41	37.0	**34.7**
Carrier freq. (GHz)	2.4	2.4	2.4	2.25	2.2	2.08	2.2	**1.7**
64-QAM signal	WiFi	WiFi	LTE	IEEE 802.11g	IEEE 802.11g	LTE	IEEE 802.11g	**LTE**
Mod. P_{out} (dBm)^2	19.6	24.8^3	25.6^4	17.7	16.8^5	N/A	19.5^6	**23.1 / 21.4^7**
PAPR (dB)^2	5.7	6.7^3	6.0^4	7.5	6.5^5	N/A	10.6^6	**6.6 / 8.3^7**
Mod. efficiency (%)^2	21.8	16^3	20.1^4	27	21.8^5	N/A	14.7^6	**15.3 / 12.3^7**
ACLR (dBc)^2	N/A	N/A	-53	N/A	N/A	-35.4	N/A	**-37.6**
Min. EVM (%)^2	5.6	3.5	N/A	2.6	2.3	2.5	0.7	**2.4**
Predistortion	Yes	No	Yes	Yes	Yes	Yes	Yes	**No**
Max. BW (MHz)	20	20	40	20	20	40	20	**100**

^{1} Simulated ^{2} Bandwidth = 20 MHz; power and efficiency results at minimum EVM unless noted otherwise
^{3} EVM = 5.6% ^{4} EVM not reported ^{5} EVM = 4% ^{6} EVM = 0.9% ^{7} EVM = 8% / 2.4%

harmonic is clearly visible, the third harmonic has been considerably attenuated, although the combiner does not contain any structures specifically intended for harmonic filtering.

Table II summarizes the presented measurement results and compares them to previously published CMOS PAs that integrate all of their PA units on a single die. While many of them report a higher efficiency than our PA, most of these ones either have a significantly lower output power or use PA classes that are generally more efficient than class D but feature other limitations. Some of them also use flip-chip packaging [29], [31] or probing at the output [32], which reduces losses compared to wire-bonding. The insertion loss of our combiner is lower than the simulated values reported by other compared papers, which is expected due to the off-chip implementation but nonetheless indicates viability for high-efficiency systems. The most outstanding result of our circuit is the widest reported signal bandwidth of 100 MHz, in contrast to other compared PAs only presenting results at bandwidths up to 20 or 40 MHz. The EVM of 2.4% is also among the best figures reported with polar and outphasing-based techniques. Our results were achieved without predistortion, which is used by most of the compared circuits.

VI. CONCLUSION

In this paper, we have presented an eight-unit class-D tri-phasing PA implemented in 28-nm CMOS, with a coupled-line power combiner on the PCB. The PA utilizes tri-phasing modulation, a newly developed technique that eliminates the inherent harmonic discontinuities of multilevel outphasing, thus potentially improving the spectral performance without compromising the back-off efficiency. Each PA unit contains a cascoded output stage supporting a 3.6-V supply voltage, and on/off logic circuitry that enables multilevel operation with low-voltage input signals.

The essential outcome of the analysis presented in this paper is that the choice of power-combiner type is critical

in terms of minimizing voltage ripple at the PA supply and ground. Accordingly, we chose to design a voltage-subtracting coupled-line combiner instead of a simpler voltage-adding one. In order to enable PCB implementation with eight narrowly-spaced inputs, as dictated by the integrated PA, we developed and analyzed the extended Marchand balun, which forms the basis of the combiner. This new coupled-line structure with arbitrarily long input lines introduces an additional degree of freedom to the balun layout, which expands the available applications and thus enables the advantages of a voltage-subtracting combiner in the context of this work.

The measurement results of the complete PA system demonstrate a peak output power of 29.7 dBm at 1.77 GHz, with an efficiency of 34.7%. Operation with modulated signals is also verified at bandwidths up to 100 MHz, which is the widest reported bandwidth among similar PAs and demonstrates the suitability of tri-phasing for wideband operation.

REFERENCES

[1] H. Chireix, "High power outphasing modulation," *Proc. IRE*, vol. 23, no. 11, pp. 1370–1392, Nov. 1935.

[2] D. C. Cox, "Linear amplification with nonlinear components," *IEEE Trans. Commun.*, vol. 22, no. 12, pp. 1942–1945, Dec. 1974.

[3] Y. J. Chen, K. Y. Jheng, A. Y. Wu, H. W. Tsao, and B. Tzeng, "Multilevel LINC system design for wireless transmitters," in *Int. Symp. VLSI Design, Automation and Test (VLSI-DAT)*, Apr. 2007.

[4] K.-Y. Jheng, Y.-C. Chen, and A.-Y. Wu, "Multilevel LINC system designs for power efficiency enhancement of transmitters," *IEEE J. Sel. Topics Signal Process.*, vol. 3, no. 3, pp. 523–532, Jun. 2009.

[5] J. Lemberg *et al.*, "Digital interpolating phase modulator for wideband outphasing transmitters," *IEEE Trans. Circuits Syst. I*, vol. 63, no. 5, pp. 705–715, May 2016.

[6] M. Martelius *et al.*, "Class D CMOS power amplifier with on/off logic for a multilevel outphasing transmitter," in *2016 IEEE Int. Symp. Circuits and Systems (ISCAS)*, May 2016, pp. 710–713.

[7] M. Kosunen *et al.*, "A 0.35-to-2.6GHz multilevel outphasing transmitter with a digital interpolating phase modulator enabling up to 400MHz instantaneous bandwidth," in *2017 IEEE Int. Solid-State Circuits Conf. (ISSCC)*, Feb. 2017, pp. 224–225.

[8] J. Lemberg *et al.*, "Tri-phasing modulation for efficient and wideband radio transmitters," *IEEE Trans. Circuits Syst. I*, vol. 65, no. 9, pp. 3085–3098, Sep. 2018.

[9] M. Martelius *et al.*, "A 30-dBm class-D power amplifier with on/off logic for an integrated tri-phasing transmitter in 28-nm CMOS," in *2018 IEEE Radio Frequency Integrated Circuits Symp. (RFIC)*, Jun. 2018, pp. 136–139.

[10] J. Lemberg *et al.*, "A 1.5–1.9-GHz all-digital tri-phasing transmitter with an integrated multilevel class-D power amplifier achieving 100-MHz RF bandwidth," *IEEE J. Solid-State Circuits*, vol. 54, no. 6, pp. 1517–1527, Jun. 2019.

[11] N. Marchand, "Transmission line conversion transformers," *Electronics*, vol. 17, no. 12, pp. 142–144, Dec. 1944.

[12] J. Hur *et al.*, "A multilevel class-D CMOS power amplifier for an outphasing transmitter with a nonisolated power combiner," *IEEE Trans. Circuits Syst. II*, vol. 63, no. 7, pp. 618–622, Jul. 2016.

[13] T. W. Barton, A. S. Jurkov, P. H. Pednekar, and D. J. Perreault, "Multi-way lossless outphasing system based on an all-transmission-line combiner," *IEEE Trans. Microw. Theory Techn.*, vol. 64, no. 4, pp. 1313–1326, Apr. 2016.

[14] T. Hwang, K. Azadet, R. S. Wilson, and J. Lin, "Nonlinearity modeling of a Chireix outphasing power amplifier," *IEEE Trans. Circuits Syst. I*, vol. 62, no. 12, pp. 2898–2907, Dec. 2015.

[15] T. P. Hung, D. K. Choi, L. E. Larson, and P. M. Asbeck, "CMOS outphasing class-D amplifier with Chireix combiner," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 8, pp. 619–621, Aug. 2007.

[16] H. Jia, B. Chi, L. Kuang, and Z. Wang, "A W-band power amplifier utilizing a miniaturized Marchand balun combiner," *IEEE Trans. Microw. Theory Techn.*, vol. 63, no. 2, pp. 719–725, Feb. 2015.

[17] S. Muralidharan, K. Wu, and M. Hella, "A compact low loss single-ended to two-way differential power divider/combiner," *IEEE Microw. Wireless Compon. Lett.*, vol. 25, no. 2, pp. 103–105, Feb. 2015.

[18] H.-C. Park, S. Daneshgar, Z. Griffith, M. Urteaga, B. S. Kim, and M. Rodwell, "Millimeter-wave series power combining using sub-quarter-wavelength baluns," *IEEE J. Solid-State Circuits*, vol. 49, no. 10, pp. 2089–2102, Oct. 2014.

[19] A. N. Stameroff, H. H. Ta, A. V. Pham, and R. E. Leoni III, "Wide-bandwidth power-combining and inverse class-F GaN power amplifier at X-band," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 3, pp. 1291–1300, Mar. 2013.

[20] M. P. van der Heijden, M. Acar, J. S. Vromans, and D. A. Calvillo-Cortes, "A 19W high-efficiency wide-band CMOS-GaN class-E Chireix RF outphasing power amplifier," in *IEEE MTT-S Int. Microw. Symp.*, Jun. 2011.

[21] R. K. Mongia, I. J. Bahl, and P. Bhartia, *RF and Microwave Coupled-Line Circuits*. Norwood, MA, USA: Artech House, 2007.

[22] E. Wilkinson, "An N-way hybrid power divider," *IRE Trans. Microw. Theory Tech.*, vol. 8, no. 1, pp. 116–118, Jan. 1960.

[23] M. Martelius *et al.*, "Spectral effects of discrete-time amplitude levels in digital-intensive wideband radio transmitters," in *2018 IEEE Int. Symp. Circuits and Systems (ISCAS)*, May 2018.

[24] J. Jang, C. Park, H. Kim, and S. Hong, "A CMOS RF power amplifier using an off-chip transmission line transformer with 62% PAE," *IEEE Microw. Wireless Compon. Lett.*, vol. 17, no. 5, pp. 385–387, May 2007.

[25] C. Lin, C. Wu, G. Zhou, and T. Ma, "General compensation method for a Marchand balun with an arbitrary connecting segment between the balance ports," *IEEE Trans. Microw. Theory Techn.*, vol. 61, no. 8, pp. 2821–2830, Aug 2013.

[26] G. Yang, Z. Wang, Z. Li, Q. Li, and F. Liu, "Balance-compensated asymmetric Marchand baluns on silicon for MMICs," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 6, pp. 391–393, June 2014.

[27] I. Piekarz, J. Sorocki, S. Gruszczynski, and K. Wincza, "Input match and output balance improvement of Marchand balun with connecting line," *IEEE Microw. Wireless Compon. Lett.*, vol. 24, no. 10, pp. 683–685, Oct 2014.

[28] A. L. Nazarian, L. F. Tiemeijer, D. L. John, J. A. van Steenwijk, M. de Langen, and R. M. T. Pijper, "A physics-based causal bond-wire model for RF applications," *IEEE Trans. Microw. Theory Techn.*, vol. 60, no. 12, pp. 3683–3692, Dec 2012.

[29] H. Xu, Y. Palaskas, A. Ravi, M. Sajadieh, M. A. El-Tanani, and K. Soumyanath, "A flip-chip-packaged 25.3 dBm Class-D outphasing power amplifier in 32 nm CMOS for WLAN application," *IEEE J. Solid-State Circuits*, vol. 46, no. 7, pp. 1596–1605, Jul. 2011.

[30] W. Tai *et al.*, "A transformer-combined 31.5 dBm outphasing power amplifier in 45 nm LP CMOS with dynamic power control for back-off power efficiency enhancement," *IEEE J. Solid-State Circuits*, vol. 47, no. 7, pp. 1646–1658, Jul. 2012.

[31] A. Banerjee, L. Ding, and R. Hezar, "High efficiency multi-mode outphasing RF power amplifier in 45nm CMOS," in *41st Eur. Solid-State Circuits Conf. (ESSCIRC)*, Sep. 2015, pp. 168–171.

[32] S. Yoo, J. S. Walling, E. C. Woo, B. Jann, and D. J. Allstot, "A switched-capacitor RF power amplifier," *IEEE J. Solid-State Circuits*, vol. 46, no. 12, pp. 2977–2987, Dec. 2011.

[33] L. Ye, J. Chen, L. Kong, E. Alon, and A. M. Niknejad, "Design considerations for a direct digitally modulated WLAN transmitter with integrated phase path and dynamic impedance modulation," *IEEE J. Solid-State Circuits*, vol. 48, no. 12, pp. 3160–3177, Dec. 2013.

[34] Q. Zhu *et al.*, "A digital polar transmitter with DC-DC converter supporting 256-QAM WLAN and 40-MHz LTE-A carrier aggregation," *IEEE J. Solid-State Circuits*, vol. 52, no. 5, pp. 1196–1209, May 2017.

[35] S. Yoo, S. Hung, and S. Yoo, "A 1W quadrature class-G switched-capacitor power amplifier with merged cell switching and linearization techniques," in *2018 IEEE Radio Frequency Integrated Circuits Symp. (RFIC)*, Jun. 2018, pp. 124–127.

[36] P. Godoy, S. Chung, T. Barton, D. Perreault, and J. Dawson, "A 2.4-GHz, 27-dBm asymmetric multilevel outphasing power amplifier in 65-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 47, no. 10, pp. 2372–2384, Oct. 2012.

Mikko Martelius (S'16–M'19) was born in Laitila, Finland, in 1988. He received the B.Sc., M.Sc. (Hons.), and D.Sc. degrees in electrical engineering from Aalto University, Espoo, Finland, in 2012, 2015, and 2019, respectively. From 2013 to 2019, he was with the Department of Electronics and Nanoengineering, Aalto University, where his research focused on switch-mode power amplifiers, digital-intensive transmitters, and frequency synthesizers. Since 2019, he has been with CoreHW, Helsinki, Finland, where he is currently working on mm-wave 5G transceivers as an RFIC Design Engineer.

Kari Stadius (S'95–M'03) received the M.Sc., Lic.Tech., and D.Sc. degrees in electrical engineering from the Helsinki University of Technology, Espoo, Finland, in 1994, 1997, and 2010, respectively. He is currently a Staff Scientist at the Department of Electronics and Nanoengineering, School of Electrical Engineering, Aalto University. He has authored or coauthored over one hundred refereed journal and conference papers in the areas of analog and RF circuit design. His research interests include the design and analysis of RF transceiver blocks with special emphasis on frequency synthesis.

Jerry Lemberg received his M.Sc. and D.Sc. degrees from Aalto University, Espoo, Finland, in 2013 and 2018, respectively. From 2010 to 2018 he was at the department of Electronics and Nanoengineering, Aalto University, and since 2018 he has been with LG Electronics as a Design Engineer. His research interests include digital-intensive and high-datarate RF transceivers.

Enrico Roverato was born in Padua, Italy, in 1988. He received the B.Sc. degree *cum laude* in information engineering from the University of Padua, Padua, in 2010, and the M.Sc. and D.Sc. degrees (Hons.) in electrical engineering from Aalto University, Espoo, Finland, in 2012 and 2017, respectively. From 2012 to 2018 he was with the Department of Electronics and Nanoengineering, Aalto University, where he carried out research on high-speed DSP algorithms for all-digital RF transmitters. He is currently a Senior Digital IC Designer with CoreHW, Tampere, Finland. He is a Consultant with Huawei Technologies, Helsinki, Finland, where he is working on the next-generation 5G cellular receivers.

Tero Nieminen received the M.Sc. degree in electrical engineering from the Helsinki University of Technology, Espoo, Finland, in 2007, and the Lic.Tech. and D.Sc. degrees in electrical engineering from Aalto University, Espoo, Finland, in 2012 and 2016, respectively. From 2005 to 2016, he was with the Electronic Circuit Design Laboratory, Helsinki University of Technology (later with Aalto University). His research work concentrated on analog/mixed-signal CMOS circuits, including analog-to-digital converters (ADCs), digital-to-time converters, and serial input/output interfaces. Since 2017, he has been with CoreHW, Tampere, Finland, providing analog CMOS design at Huawei Technologies, Helsinki, Finland, where he has been involved with ADCs for receiver circuits.

Yury Antonov (S'15–M'18) received the Engineering degree in computer design and technology from Bauman Moscow State Technical University (BMSTU), Moscow, Russia, in 2007, and the M.Sc. degree (Hons.) in electrical engineering from Aalto University, Espoo, Finland, in 2014. From 2004 to 2010, he was a Circuit Designer with several R&D companies in Moscow, where he was developing CPLD/FPGA-based mixed-signal circuits for the synchronization of scalable radar-phased arrays and designing downconversion front ends for lidar-based measurement solutions. From 2014 to 2019, he was with Aalto University where he has worked on multiple successful tape-outs from 28 to 65 nm. He is now a Senior RFIC Design Engineer with CoreHW, Helsinki, Finland, where he is involved in mm-wave frequency synthesizer design. His research interests are in multi-phase and spur-free frequency synthesis for RF/mm-wave front ends with digital assistance and on-chip calibration loops.

Lauri Anttila (S'06–M'11) received the M.Sc. and the D.Sc. (Hons.) degrees in electrical engineering from Tampere University of Technology (TUT), Tampere, Finland, in 2004 and 2011, respectively. Since 2016, he has been a University Researcher at the Department of Electrical Engineering, Tampere University (formerly TUT). In 2016–2017, he was a Visiting Research Fellow at the Department of Electronics and Nanoengineering, Aalto University, Finland. He has co-authored 100+ refereed articles, as well as three book chapters. His research interests include signal processing for wireless communications, transmitter and receiver linearization, and radio implementation challenges in 5G cellular radio, full-duplex radio, and large-scale antenna systems.

Mikko Valkama (S'99–M'02–SM'15) received the M.Sc. and Ph.D. Degrees (both with honors) in electrical engineering (EE) from Tampere University of Technology (TUT), Finland, in 2000 and 2001, respectively. In 2002, he received the Best Ph.D. Thesis -award by the Finnish Academy of Science and Letters for his dissertation entitled "Advanced I/Q signal processing for wideband receivers: Models and algorithms". In 2003, he was working as a visiting post-doc research fellow with the Communications Systems and Signal Processing Institute at SDSU, San Diego, CA. Currently, he is a Full Professor and Department Head of Electrical Engineering at newly formed Tampere University (TAU), Finland. His general research interests include radio communications, radio localization, and radio-based sensing, with particular emphasis on 5G and beyond mobile radio networks.

Marko Kosunen (S'97–M'07) received the M.Sc., Lic.Sc., and D.Sc. (Hons.) degrees from the Helsinki University of Technology, Espoo, Finland, in 1998, 2001, and 2006, respectively. He is currently a Senior Researcher at the Department of Electronics and Nanoengineering, Aalto University. He is currently involved in implementations of digital-intensive transceiver circuits and medical sensor electronics. His expertise is in implementation of the wireless transceiver DSP algorithms and communication circuits.

Jussi Ryynänen (S'99–M'04–SM'16) was born in Ilmajoki, Finland, in 1973. He received the M.Sc. and D.Sc. degrees in electrical engineering from the Helsinki University of Technology, Espoo, Finland, in 1998 and 2004, respectively. He is a full professor and the Head of the Department of Electronics and Nanoengineering, Aalto University, Espoo. He has authored or co-authored more than 140 refereed journal and conference papers in analog and RF circuit design. He holds seven patents on RF circuits. His research interests are integrated transceiver circuits for wireless applications. Prof. Ryynänen has served as a TPC Member for the European Solid-State Circuits Conference (ESSCIRC) and the IEEE International Solid-State Circuits Conference (ISSCC), and as a Guest Editor for the IEEE Journal of Solid-State Circuits.