

Load-Resistor-Affected Dynamic Models in Control Design of Switched-Mode Converters

Teuvo Suntio

Electrical Energy Engineering, Tampere University of Technology, Tampere, Finland

Korkeakoulunkatu 3, FI-33720 Tampere, Finland

Email: teuvo.suntio@tut.fi

Phone: +358400828431

Load-Resistor-Affected Dynamic Models in Control Design of Switched-Mode Converters

Abstract: The application of a resistor as a load of the pulse-width-modulated DC-DC converters has dominated the dynamic modelling since the development of the modelling methods in early 1970s. In 1990s, the research in the source and load interactions was very active providing valuable information to justify the necessity to develop unterminated dynamic models for characterising the dynamics of the converters. The small-signal modelling can be performed always by using the ideal load, which is determined by the output-terminal variable to be kept constant, regardless of whether the actual converter can operate or not with the ideal load. This paper will review the feasibility of using the load-resistor-affected models in control design of switched mode converters. The best strategy is always to use unterminated models, which can be used to obtain different load-impedance-affected models if needed. A buck converter is used as the source of information.

Keywords: switched-mode converter; load effect; control design

1. Introduction

The small-signal modelling of switched-mode converters is most often performed by using a resistor as a load [1-28] even if the practical load will never be a resistor. Sometimes, the open-loop converter cannot operate with the required ideal load, which is dictated by the output-terminal feedback variable (i.e., the output-voltage feedback requires to use a constant-current sink as an ideal load, and the output-current feedback requires to use a constant-voltage sink as an ideal load, respectively [29,30]), and therefore, a resistor has to be used as a load. The special cases are the current-mode-controlled converters, which cannot be operated with a constant-current sink as a load in open loop due to their current-output nature as discussed in [31], and the converters, where the ideal load shall be the same type as the input source as discussed in [32]. The analytic modelling can be, however, performed always by using the proper ideal load [30]. If the practical frequency responses are load-resistor affected then the unterminated responses have to be solved computationally by utilizing the load-interaction formulations given explicitly, for example, in [33].

The first attempts to justify the necessity to use the unterminated small-signal models were published in [34,35] in early 2000s, and later adopted in use in [29-33,37-39]. The unterminated modelling method has not, however, gained popularity as Refs. [15-22] clearly imply, which may be the consequence of the popular text books promoting the use of resistor-loaded small-signal modelling methods as in [23,24].

The load-resistor effect on the converter dynamic behaviour is reflected via the open-loop output impedance [30]: In the output-voltage feedback-controlled converters, the load resistor starts affecting the converter dynamics when it is close to the magnitude of the open-loop output impedance or higher than it. In the output-current feedback-controlled converters, the load resistor starts affecting when it is lower than the magnitude of the output impedance, respectively. In practice, this means that the control method and controlled output variable as well as the operation mode (i.e., continuous (CCM) or discontinuous (DCM) conduction mode) will determine the severity of the load-resistor interactions in the converter dynamics.

We will review the load-resistor effects in case of a buck converter under direct-duty-ratio (DDR) and peak-current-mode (PCM) control in CCM and DCM with output voltage and current feedback controls. As discussed in [27,28], the load-resistor-affected small-signal models can be used in designing the feedback control loop under the output-voltage feedback control in most of the cases, because the load-resistor effects usually dominate the dynamic behaviour only at the low frequencies or at the frequencies in vicinity of the power-stage resonances. In case of output-current feedback-controlled converters, the load resistor reduces the crossover frequency of the feedback loop significantly, which will lead to instability, when the practical load is connected at the output terminal as discussed and demonstrated in [38,39]. This paper will explicitly clarify the root causes for the load-resistor effects in the converter dynamics so that the

reader can select the proper modelling approach in advance and avoid the severe problems in control design.

The rest of the paper is organized as follows: Section 2 introduces the theoretical basis for the load-affected dynamics as well as the specific formulations for the voltage-fed-voltage-output (VF/VO) and voltage-fed-current-output (VF/CO) buck converter in CCM and DCM under DDR and PCM controls. Section 3 introduces the analytical and experimental validations of the theoretical load-resistor effects. The conclusions are finally presented in Section 4.

2. Load-Affected Dynamics

The set of transfer functions representing the dynamics of a DC-DC converter can be given by (1) and the corresponding general load by (2).

$$\begin{bmatrix} \hat{y}_{\text{in-C}} \\ \hat{y}_{\text{out-C}} \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & -C_{22} & C_{23} \end{bmatrix} \begin{bmatrix} \hat{u}_{\text{in-C}} \\ \hat{u}_{\text{out-C}} \\ \hat{u}_{\text{c-C}} \end{bmatrix} \quad (1)$$

$$\begin{bmatrix} \hat{y}_{\text{in-L}} \\ \hat{y}_{\text{out-L}} \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & -L_{22} \end{bmatrix} \begin{bmatrix} \hat{u}_{\text{in-L}} \\ \hat{u}_{\text{out-L}} \end{bmatrix} \quad (2)$$

where \hat{u} and \hat{y} denote the input and output variables as well as the subscripts ‘in’ and ‘out’ denote the terminal, where the variable physically exists and the subscript ‘c’ the control variable, respectively. The minus sign in front of the elements (2,2) in (1) and (2) denotes that the output current is flowing out of the output terminal, respectively, as shown in Fig. 1.

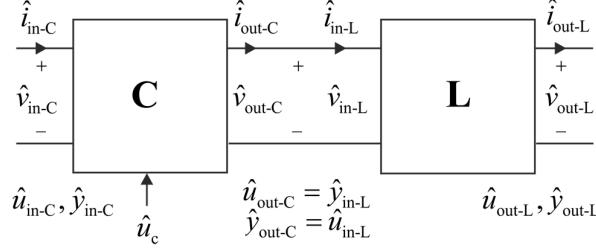


Fig. 1. General representation of the cascaded system composing of the converter (**C**) and the load (**L**).

According to Fig. 1, the output-terminal variables of the converter equal the input-terminal variables of the load. Therefore, the pair of simultaneous equations can be given according to (3). According to it, the mapping from the system input variables to the system output variables can be computed to be as given in (4), respectively. The formulation in (4) follows the extra-element-method-based formulation introduced in [40].

$$\begin{cases} \begin{bmatrix} \hat{y}_{in-C} \\ \hat{u}_{in-L} \end{bmatrix} = \begin{bmatrix} C_{11} & C_{12} & C_{13} \\ C_{21} & -C_{22} & C_{23} \end{bmatrix} \begin{bmatrix} \hat{u}_{in-C} \\ \hat{y}_{in-L} \\ \hat{u}_c \end{bmatrix} \\ \begin{bmatrix} \hat{y}_{in-L} \\ \hat{y}_{out-L} \end{bmatrix} = \begin{bmatrix} L_{11} & L_{12} \\ L_{21} & -L_{22} \end{bmatrix} \begin{bmatrix} \hat{u}_{in-L} \\ \hat{u}_{out-L} \end{bmatrix} \end{cases} \quad (3)$$

$$\begin{bmatrix} \hat{y}_{in-C} \\ \hat{y}_{out-L} \end{bmatrix} = \begin{bmatrix} \frac{1+L_{11}C_{22-xi}}{1+L_{11}C_{22}}C_{11} & \frac{L_{12}}{1+L_{11}C_{22}}C_{12} & \frac{1+L_{11}C_{22-\infty}}{1+L_{11}C_{22}}C_{13} \\ \frac{L_{21}}{1+L_{11}C_{22}}C_{21} & -(L_{22} + \frac{L_{12}L_{21}C_{22}}{1+L_{11}C_{22}}) & \frac{L_{21}}{1+L_{11}C_{22}}C_{23} \end{bmatrix} \begin{bmatrix} \hat{u}_{in-C} \\ \hat{u}_{out-L} \\ \hat{u}_c \end{bmatrix} \quad (4)$$

where the special elements C_{22-xi} and $C_{22-\infty}$ are defined in (5) based on the converter transfer functions in (1).

$$C_{22-xi} = C_{22} + \frac{C_{12}C_{21}}{C_{11}} \quad C_{22-\infty} = C_{22} + \frac{C_{12}C_{23}}{C_{13}} \quad (5)$$

The load system (\mathbf{L}) is usually considered to contain only an ohmic circuit element (L_{11}) with an ideal source. Thus $L_{12} = L_{21} = 1$ and $L_{22} = 0$ in (2). In this specific case, Eq. (4) can be given by (6), which is also utilized in the subsequent analyses in this paper.

$$\begin{bmatrix} \hat{y}_{\text{in-C}} \\ \hat{y}_{\text{out-L}} \end{bmatrix} = \begin{bmatrix} \frac{1+L_{11}C_{22-\text{xi}}}{1+L_{11}C_{22}} C_{11} & \frac{C_{12}}{1+L_{11}C_{22}} & \frac{1+L_{11}C_{22-\infty}}{1+L_{11}C_{22}} C_{13} \\ \frac{C_{21}}{1+L_{11}C_{22}} & -\frac{C_{22}}{1+L_{11}C_{22}} & \frac{C_{23}}{1+L_{11}C_{22}} \end{bmatrix} \begin{bmatrix} \hat{u}_{\text{in-C}} \\ \hat{u}_{\text{out-L}} \\ \hat{u}_c \end{bmatrix} \quad (6)$$

Eq. (6) indicates that all the transfer functions are affected by the impedance-ratio-based (i.e., $L_{11}C_{22}$) sensitivity function $(1+L_{11}C_{22})^{-1}$, where the impedance ratio is known as minor-loop gain in [41,42]. The input-terminal transfer function C_{11} and C_{13} are also affected by the certain impedance ratios $L_{11}C_{22-\text{xi}}$ and $L_{11}C_{22-\infty}$ as visible in (6). The explicit forms of the special elements in (5) can be found from [30] for a number of converters including the buck converter. In the context of this paper, we will treat only the load effects on the control-to-output transfer function (C_{23}) determined by the element (2,3) in (6).

The power stage of the buck converter in the voltage-output mode is given in Fig. 2 and in the current-output mode in Fig. 3, respectively. In voltage-output mode (Fig.2), the analysis and experimental information are given both in CCM and DCM (Note: The value of the inductor is defined in the figure capture). In current-output mode (Fig.3), the analysis and experimental information are given only in CCM. The ideal load of the converter in the voltage-output mode is the constant-current sink (Fig. 2) and in the current-output mode the constant-voltage source (Fig. 3). The load resistor (R_L) is denoted in the figures by dashed-line connection.

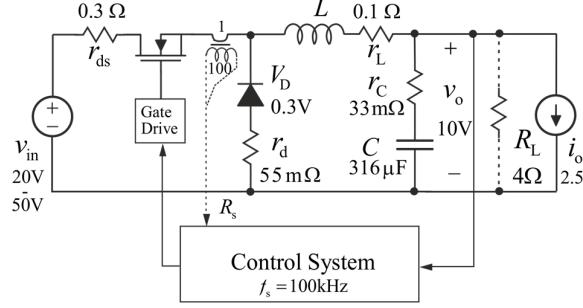


Fig. 2. The power stage of the buck converter in voltage-output mode. In CCM, $L = 105\mu\text{H}$ and in DCM, $L = 5\mu\text{H}$.

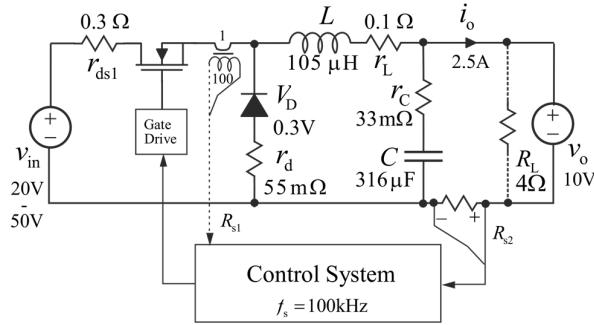


Fig. 3. The power stage of the buck converter in current-output mode.

The simultaneous sets of transfer functions in voltage-output mode can be given in an explicit form applicable to the DDR and PCM-controlled converters as shown in (7) [30]. The simultaneous sets of transfer functions in current-output mode can be given similarly as above according to (8) [30], respectively. Both of the sets correspond to (1) and (2).

$$\begin{cases} \begin{bmatrix} \hat{i}_{in} \\ \hat{v}_o \end{bmatrix} = \begin{bmatrix} Y_{in}^{vo} & T_{oi}^{vo} & G_{ci}^{vo} \\ G_{io}^{vo} & -Z_o^{vo} & G_{co}^{vo} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{i}_o \\ \hat{c} \end{bmatrix} \\ \begin{bmatrix} \hat{i}_{in-L} \\ \hat{v}_{out-L} \end{bmatrix} = \begin{bmatrix} Y_{in-L} & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in-L} \\ \hat{i}_{out-L} \end{bmatrix} \end{cases} \quad (7)$$

$$\begin{cases} \begin{bmatrix} \hat{i}_{in} \\ \hat{i}_o \end{bmatrix} = \begin{bmatrix} Y_{in}^{co} & T_{oi}^{co} & G_{ci}^{co} \\ G_{io}^{co} & -Y_o^{co} & G_{co}^{co} \end{bmatrix} \begin{bmatrix} \hat{v}_{in} \\ \hat{v}_o \\ \hat{c} \end{bmatrix} \\ \begin{bmatrix} \hat{i}_{in-L} \\ \hat{i}_{out-L} \end{bmatrix} = \begin{bmatrix} Z_{in-L} & 1 \\ 1 & 0 \end{bmatrix} \begin{bmatrix} \hat{v}_{in-L} \\ \hat{v}_{out-L} \end{bmatrix} \end{cases} \quad (8)$$

We will treat, in this paper, only the load interactions in the control-to-output-voltage transfer function (i.e., Eq. (7), the element (2,3)) and in the control-to-output-current transfer function (Eq. (8), the element (2,3)). According to (6) (i.e., the element (2,3)), the load-affected $G_{co-o}^{VO-R_L}$ in (7) and $G_{co-o}^{CO-R_L}$ in (8) can be given by

$$G_{co-o}^{VO-R_L} = \frac{G_{co-o}^{VO}}{1 + \frac{Z_{o-o}^{VO}}{R_L}} \quad G_{co-o}^{CO-R_L} = \frac{G_{co-o}^{CO}}{1 + \frac{R_L}{Z_{o-o}^{CO}}} \quad (9)$$

If the power stage is the same in the VO and CO modes then $Z_{o-o}^{CO} = Z_{o-o}^{VO}$ [30]. According to (9), this information can be interpreted as follows: If the power stage in the voltage-output mode is affected by the load resistor in the certain range of frequencies then the power stage in the current-output mode is affected by the load resistor at all the frequencies, which do not belong to the certain range of frequencies, respectively.

2.1: Specific Formulation for VF-VO DDR-Controlled Buck Converter

2.1.1: CCM Operation

The unterminated G_{co-o}^{VO-DDR} and Z_{o-o}^{VO-DDR} of the buck converter in VO mode in CCM can be given according to [30] by

$$\begin{aligned} G_{co-o}^{VO} &= \frac{V_e(1 + sr_c C)}{LC(s^2 + s \frac{r_e}{L} + \frac{1}{LC})} \\ Z_{o-o}^{VO} &= \frac{(r_e - r_c + sL)(1 + sr_c C)}{LC(s^2 + s \frac{r_e}{L} + \frac{1}{LC})} \end{aligned} \quad (10)$$

where

$$\begin{aligned} r_e &= r_L + Dr_{ds1} + D'r_d + r_C \\ V_e &= V_{in} + V_D + (r_d - r_{ds1})I_o \end{aligned} \quad (11)$$

According to (9) and (10), we can compute $G_{co-o}^{VO-DDR-R_L}$ to be

$$G_{co-o}^{VO-DDR-R_L} \approx \frac{V_e(1+sr_C C)}{LC(s^2 + s(\frac{1}{R_L C} + \frac{r_e}{L}) + \frac{1}{LC})} \quad (12)$$

According to (10) and (12), we can conclude that the load resistor affects only the damping of the system as

$$\zeta_{R_L} = \frac{r_e}{2} \sqrt{\frac{C}{L}} + \frac{1}{2R_L} \sqrt{\frac{L}{C}} \quad (13)$$

where the first term corresponds to the original damping and the last term to the damping provided by the load resistor as also stated in [27,28].

2.1.2: DCM Operation

The unterminated $G_{co-o}^{VO-DDR-DCM}$ and $Z_{o-o}^{VO-DDR-DCM}$ of the buck converter in DCM can be

given according to [30] by

$$\begin{aligned} G_{co-o}^{VO-DDR-DCM} &= \frac{2V_{in}(1+sr_C C)}{LC(s^2 + s\frac{R_{eq}}{L}\sqrt{\frac{K}{1-M}} + \frac{1}{LC(1-M)}\sqrt{\frac{K}{1-M}})} \\ &\quad \frac{(sL + R_{eq}\sqrt{\frac{K}{1-M}})(1+sr_C C)}{LC} \quad (14) \\ Z_{o-o}^{VO-DDR-DCM} &= \frac{LC}{LC(s^2 + s\frac{R_{eq}}{L}\sqrt{\frac{K}{1-M}} + \frac{1}{LC(1-M)}\sqrt{\frac{K}{1-M}})} \end{aligned}$$

where $M = V_o / V_{in}$, $K = 2L / T_s R_{eq}$, and $R_{eq} = V_o / I_o$ [30].

The roots of the denominator in (14) are usually well separated [12], and therefore, the system poles can be approximated as (Note: LF stands for low frequency, and HF for high frequency)

$$\begin{aligned} \omega_{p-LF}^{VO-DDR-DCM} &\approx \frac{1}{R_{eq}C(1-M)} \\ \omega_{p-HF}^{VO-DDR-DCM} &\approx \frac{R_{eq}}{L} \sqrt{\frac{K}{1-M}} \end{aligned} \quad (15)$$

According to (9) and (14), the load-resistor-affected $G_{\text{co-o}}^{\text{VO-R}_L}$ in DCM can be given by

$$G_{\text{co-o}}^{\text{VO-DDR-DCM-R}_L} = \frac{2V_{\text{in}}(1+sr_C C)}{LC(s^2 + s(\frac{1}{R_L C} + \frac{R_{\text{eq}}}{L} \sqrt{\frac{K}{1-M}}) + \frac{1}{LC} (\frac{1}{1-M} + \frac{R_{\text{eq}}}{R_L}) \sqrt{\frac{K}{1-M}})} \quad (16)$$

and the system poles as

$$\begin{aligned} \omega_{\text{p-LF}}^{\text{VO-DDR-DCM-R}_L} &\approx \frac{\frac{2-M}{1-M} \sqrt{\frac{K}{1-M}}}{\frac{L}{R_L} + R_{\text{eq}} C \sqrt{\frac{K}{1-M}}} \approx \frac{2-M}{(1-M)R_{\text{eq}} C} \\ \omega_{\text{p-HF}}^{\text{VO-DDR-DCM-R}_L} &\approx \frac{1}{R_{\text{eq}} C} + \frac{R_{\text{eq}}}{L} \sqrt{\frac{K}{1-M}} \approx \frac{R_{\text{eq}}}{L} \sqrt{\frac{K}{1-M}} \end{aligned} \quad (17)$$

According to (15) and (17), we can conclude that the load resistor moves slightly the low-frequency pole into higher frequencies (i.e., twice the unterminated location), and it does not affect the higher-frequency pole in practice. This means that the load-resistor effect is quite insignificant.

2.2: Specific Formulations for VF-VO PCM-Controlled Buck Converter

2.2.1: CCM Operation

The unterminated $G_{\text{co-o}}^{\text{VO-PCM}}$ and $Z_{\text{o-o}}^{\text{VO-PCM}}$ of the buck converter in VO mode in CCM can be given according to [30, 41-43] by

$$\begin{aligned} G_{\text{co-o}}^{\text{VO-PCM}} &= \frac{F_m V_e (1+sr_C C)}{LC(s^2 + s \cdot \frac{r_e + F_m V_e q_L}{L} + \frac{1}{LC})} \\ Z_{\text{o-o}}^{\text{VO-PCM}} &= \frac{(r_e - r_C + F_m V_e q_L + sL)(1+sr_C C)}{LC(s^2 + s \cdot \frac{r_e + F_m V_e q_L}{L} + \frac{1}{LC})} \end{aligned} \quad (18)$$

where V_e and r_e are as given in (11) as well as F_m , q_L , and q_{in} are given in (19).

$$\begin{aligned}
F_m &= \frac{1}{T_s \left(M_c + \frac{(D' - D)V_e}{2L} \right)} \\
q_L &= 1 + \frac{DD'T_s}{2L} (r_d - r_{ds1}) \\
q_{in} &= \frac{DD'T_s}{2L}
\end{aligned} \tag{19}$$

The damping in a PCM-controlled converter is rather high [43], and therefore, the system poles are well separated. Thus they can be approximated as

$$\begin{aligned}
\omega_{p-LF}^{VO-PCM} &\approx \frac{1}{F_m V_e q_L C} \\
\omega_{p-HF}^{VO-PCM} &\approx \frac{F_m V_e q_L}{L}
\end{aligned} \tag{20}$$

The load-resistor-affected $G_{co-o}^{VO-PCM-R_L}$ can be given according to (9) and (18) by

$$G_{co-o}^{VO-PCM-R_L} = \frac{F_m V_e (1 + s r_c C)}{LC \left(s^2 + s \left(\frac{1}{R_L C} + \frac{F_m V_e q_L}{L} \right) + \frac{1}{LC} \left(1 + \frac{F_m V_e q_L}{R_L} \right) \right)} \tag{21}$$

Similarly as in case of (20), the system poles can be given by

$$\begin{aligned}
\omega_{p-LF}^{VO-PCM-R_L} &\approx \frac{1}{R_L C} \\
\omega_{p-HF}^{VO-PCM-R_L} &\approx \frac{F_m V_e q_L}{L}
\end{aligned} \tag{22}$$

According to (20) and (22), we may conclude that the load resistor affects only the low-frequency dynamic behaviour of the converter as discussed and demonstrated in [43].

2.2.2: DCM Operation

The unterminated $G_{co-o}^{VO-PCM-DCM}$ and $Z_{o-o}^{VO-PCM-DCM}$ of the buck converter in VO mode in DCM can be given according to [29,30] by

$$\begin{aligned}
G_{\text{co-o}}^{\text{VO-PCM-DCM}} &= \\
&\frac{2F_m V_{\text{in}} (1 + sr_c C)}{LC \left(s^2 + s \frac{R_{\text{eq}} \sqrt{\frac{K}{1-M}} + 2F_m V_{\text{in}}}{L} + \frac{1}{LC} \left(\frac{1}{1-M} \sqrt{\frac{K}{1-M}} + 2F_m V_{\text{in}} q_c \right) \right)} \\
Z_{\text{o-o}}^{\text{VO-PCM-DCM}} &= \\
&\frac{(sL + 2F_m V_{\text{in}} + R_{\text{eq}} \sqrt{\frac{K}{1-M}})(1 + sr_c C)}{LC \left(s^2 + s \frac{R_{\text{eq}} \sqrt{\frac{K}{1-M}} + 2F_m V_{\text{in}}}{L} + \frac{1}{LC} \left(\frac{1}{1-M} \sqrt{\frac{K}{1-M}} + 2F_m V_{\text{in}} q_c \right) \right)}
\end{aligned} \tag{23}$$

where

$$\begin{aligned}
F_m &= \frac{1}{T_s \left(M_c + \frac{V_{\text{in}} (1-M) (1 - \sqrt{\frac{K}{1-M}})}{L} \right)} \\
q_c &= \frac{1}{R_{\text{eq}} (1-M)} (1 - 2M \sqrt{\frac{1-M}{K}})
\end{aligned} \tag{24}$$

Similarly as above, the system poles (cf. Eq. (23)) can be approximated as

$$\begin{aligned}
\omega_{\text{p-LF}}^{\text{VO-PCM-DCM}} &\approx \frac{1-2M}{1-M} \cdot \frac{1}{R_{\text{eq}} C} \\
\omega_{\text{p-HF}}^{\text{VO-PCM-DCM}} &\approx \frac{D}{M-D} \cdot \frac{R_{\text{eq}}}{L}
\end{aligned} \tag{25}$$

The load-resistor-affected $G_{\text{co-o}}^{\text{VO-PCM-DCM-R}_L}$ can be given according to (9) and (23) by

$$G_{\text{co-o}}^{\text{VO-PCM-DCM-R}_L} = \frac{2F_m V_{\text{in}} (1 + sr_c C)}{LC \left(s^2 + s \left(\frac{1}{R_L C} + \frac{R_{\text{eq}} \sqrt{\frac{K}{1-M}} + 2F_m V_{\text{in}}}{L} \right) + \frac{1}{LC} \left(\frac{R_{\text{eq}}}{R_L} + \frac{1}{1-M} \right) \sqrt{\frac{K}{1-M}} + 2F_m V_{\text{in}} \left(\frac{1}{R_L} + q_c \right) \right)} \tag{26}$$

Similarly as above, the system poles can be given by

$$\begin{aligned}\omega_{\text{p-LF}}^{\text{VO-PCM-DCM-}R_L} &\approx \frac{2-3M}{1-M} \cdot \frac{1}{R_{\text{eq}}C} \\ \omega_{\text{p-HF}}^{\text{VO-PCM-DCM-}R_L} &\approx \frac{D}{M-D} \cdot \frac{R_{\text{eq}}}{L}\end{aligned}\quad (27)$$

Eq. (25) shows that the system becomes unstable when $M>0.5$. The load-resistor-affected poles in (27) predict that the system becomes unstable when $M>2/3$ as discussed also in [13,23]. According to (25) and (27), we may conclude that the load resistor affects only the low-frequency dynamic behaviour of the converter but it hides the real location of the right-half-plane (RHP) pole, which will affect the control design (i.e., the minimum feedback-loop crossover frequency is limited) as discussed in [30].

2.3: Specific Formulations for VF-CO DDR-Controlled Buck Converter

The unterminated $G_{\text{co-o}}^{\text{CO-DDR}}$ and $Z_{\text{o-o}}^{\text{CO-DDR}}$ of the buck converter in CO mode in CCM can be given according to [30,36,37] by

$$\begin{aligned}G_{\text{co-o}}^{\text{CO-DDR}} &= \frac{V_e}{sL + r_e - r_c} \\ Z_{\text{o-o}}^{\text{CO-DDR}} &= \frac{(sL + r_e - r_c)(1 + sr_c C)}{s^2 LC + sr_e C + 1}\end{aligned}\quad (28)$$

where r_e and V_e are defined in (11). As discussed earlier, the output impedance equals the output impedance of VO converter in (10) when the power stage is same as shown in (28). The converter is basically of first order in dynamic sense due to the effect of the ideal voltage source connected at the output terminal (cf. Fig. 3).

The load-resistor-affected $G_{\text{co-o}}^{\text{CO-DDR-}R_L}$ can be given according to (9) and (28) by

$$G_{\text{o-o}}^{\text{CO-DDR-}R_L} \approx \frac{V_e(1 + sr_c C)}{R_L C \left(s^2 + s \left(\frac{1}{R_L C} + \frac{r_e}{L} \right) + \frac{1}{LC} \right)} \quad (29)$$

Eq. (29) shows that the load resistor changes $G_{\text{co-o}}^{\text{CO-DDR-}R_L}$ to resemble the second-order transfer function given in (12) but its DC gain is reduced to V_e / R_L . This reduction

indicates significant reduction of the output-voltage-loop crossover frequency, and thus the practical load (i.e., voltage-type load) will recover the unterminated mode of the feedback loop, which may easily lead to instability due to extremely high crossover frequency [36,37].

2.4: Specific Formulations for VF-CO PCM-Controlled Buck Converter

The unterminated $G_{\text{co-o}}^{\text{CO-PCM}}$ and $Z_{\text{o-o}}^{\text{CO-PCM}}$ of the buck converter in CO mode in CCM can be given according to [30,36,37] by

$$\begin{aligned} G_{\text{co-o}}^{\text{CO-PCM}} &= \frac{F_m V_e}{sL + r_e - r_C + F_m q_L V_e} \\ Z_{\text{o-o}}^{\text{CO-PCM}} &= \frac{(sL + r_e - r_C + F_m q_L V_e)(1 + s r_C C)}{s^2 L C + s(r_e + F_m q_L V_e)C + 1} \end{aligned} \quad (30)$$

where r_e and V_e are given in (11) as well as F_m and q_L in (19). As discussed earlier, the output impedance equals the output impedance of VO converter in (18) when the power stage is same as shown in (30). The converter is basically of first order in dynamic sense due to the effect of the ideal voltage source connected at the output terminal (cf. Fig. 3).

The system pole $\omega_p^{\text{CO-PCM}}$ equals approximately $F_m q_L V_e / L$.

The load-resistor-affected $G_{\text{co-o}}^{\text{CO-R}_L}$ can be given according to (9) and (30) by

$$G_{\text{co-o}}^{\text{CO-PCM-R}_L} \approx \frac{F_m V_e (1 + s r_C C)}{LC R_L \left(s^2 + s \left(\frac{1}{R_L C} + \frac{F_m V_e q_L}{L} \right) + \frac{1}{LC} \left(1 + \frac{F_m V_e q_L}{R_L} \right) \right)} \quad (31)$$

where the system poles equal the poles given in (22).

Eq. (31) shows that the load resistor changes $G_{\text{co-o}}^{\text{CO-PCM-R}_L}$ to resemble the second-order transfer function given in (21) with the same close to unity DC gain. The reduction of the feedback loop crossover frequency will take place due to the significant reduction in the frequency of the low-frequency system pole i.e., $F_m q_L V_e / L \gg 1 / R_L C$. The practical load (i.e., voltage-type load) will recover the unterminated mode of the feedback

loop, which may easily lead to instability due to extremely high crossover frequency [36,37].

2.5: Discussions

As Eq. (9) indicates, the control-to-output transfer functions are affected by the impedance-ratio-based sensitivity functions $S^{VO} = (1 + Z_{o-o}^{VO} / R_L)^{-1}$ and $S^{CO} = (1 + R_L / Z_{o-o}^{CO})^{-1}$, respectively. The load-resistor effect will take place, when the named magnitudes of the impedance ratios are close to one or higher. If the load effects are computed based on the load-resistor-affected transfer functions in (9) then the load-resistor-affected $G_{co-o}^{R_L}$ would be

$$G_{co-o}^{VO-R_L} = \frac{G_{co-o}^{VO}}{1 + 2 \frac{Z_{o-o}^{VO}}{R_L}} \quad G_{co-o}^{CO-R_L} = \frac{G_{co-o}^{CO}}{1 + 2 \frac{R_L}{Z_{o-o}^{CO}}} \quad (32)$$

which indicate that the error in analyses would be approximately 6 dB compared to the correct formulations in (9).

As discussed above, the typical load-resistor effect concentrates at the low frequencies or at the frequencies in vicinity of the resonant frequencies in the voltage-output converters. This makes sense, because the magnitude of the output impedance is highest at the resonant frequency under DDR control in CCM and under PCM control at the low frequencies. Thus the load resistor does not usually affect the converter dynamic behaviour at the typical feedback-loop-crossover frequencies, and therefore, the control design can be performed with the load-resistor-affected small-signal models as well.

The impedance ratio in the current-output converter is the inverse of the corresponding voltage-output-converter impedance ratio. Therefore, it is easy to understand that the typical load-resistor effect concentrates at the high frequencies, and

thus the control design cannot be performed with the load-resistor-affected small-signal models.

As discussed and demonstrated in Section 2.2 (i.e., the location of the RHP pole), the load resistor can also affect the control design in the voltage-output converters even if the effects are concentrated at the low frequencies. The observed phenomenon is actually a very good indication that the best strategy in small-signal modelling is to perform it in unterminated mode to avoiding problems in the converter stability and transient performance.

The unterminated models can be recovered from the load-resistor-affected models by letting $R_L \rightarrow \infty$ in the output-voltage-controlled converters operating in CCM (cf. Eq. (21) vs. Eq. (18)), when the averaged inductor current is left intact. In all the other cases, the same strategy does not work properly. The unterminated models cannot be usually recovered from the load-resistor-affected models in DCM. As an example, the typical control-to-output-voltage transfer function for the DDR-controlled buck converter in DCM ($G_{\text{co-o}}^{\text{VO-DDR-}R_L}$) is given by [12]

$$G_{\text{co-o}}^{\text{VO-DDR-}R_L} = \frac{2V_{\text{in}}(1+sr_C C)}{LC(s^2 + s(\frac{1}{R_L C} + \frac{R_{\text{eq}}}{L} \sqrt{\frac{K}{1-M}}) + \frac{2-M}{LC(1-M)} \sqrt{\frac{K}{1-M}})} \quad (33)$$

If letting $R_L \rightarrow \infty$ then $G_{\text{co-o}}^{\text{VO-DDR-}R_L}$ in (33) will become

$$G_{\text{co-o}}^{\text{VO-DDR}} = \frac{2V_{\text{in}}(1+sr_C C)}{LC(s^2 + s \frac{R_{\text{eq}}}{L} \sqrt{\frac{K}{1-M}} + \frac{2-M}{LC(1-M)} \sqrt{\frac{K}{1-M}})} \quad (34)$$

which does not comply with the real unterminated model given in (14). In addition, R_{eq} is usually denoted by R_L as explicitly visible in [23, p.110]. Therefore, Eq. (34) will not make sense anymore when $R_L \rightarrow \infty$.

3. Theoretical and Experimental Validation

The load-resistor-affected dynamic behaviours of the voltage-fed buck converter in voltage and current-output modes are validated by simulation-based and experimental frequency response measurements. The used pseudorandom binary sequence (PRBS) frequency-response measurement technique is described more in detail in [46]. The used MatlabTM Simulink-based switching models are presented in detail in [47]. The PRBS frequency-response measurement method is implemented as a Matlab m-file, which operates the corresponding Simulink switching model. The validations are performed at the output voltage of 10 V and at the output power of 25 W, respectively.

Fig. 4 shows the experimental frequency response of the output-voltage-feedback loop as unterminated (black line) and load-resistor affected (red line) (i.e., the DDR-controlled buck converter in Fig. 2), which reflects the behaviour of the control-to-output voltage transfer function explicitly, when the buck converter operates in CCM. As discussed in Sections 2.1 and 2.5, the load-resistor effect is visible as an increase in damping in vicinity of the resonant frequency, where the magnitude of the open-loop output impedance is highest (cf. Fig. 6). In this specific case, the damping is increased from 0.28 to 0.35, which is quite an insignificant effect as discussed earlier.

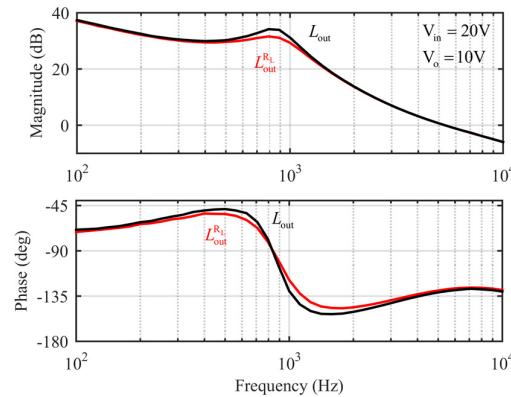


Fig. 4. The experimental unterminated (black line) and load-resistor-affected (red line) control-to-output-voltage transfer function of the DDR-controlled buck converter in CCM.

Fig. 5 shows the experimental frequency response of the control-to-output-voltage transfer function of the DDR-controlled buck converter (cf. Fig. 2) operating in DCM as unterminated (black line) and load-resistor affected (red line). The figure shows that the load-resistor effect dominates at the low frequencies, where the unterminated low-frequency pole (black line) locates approximately at 240 Hz and the corresponding load-resistor-affected pole (red line) at 400 Hz, respectively, which complies with the discussions provided in Section 2.1. The open-loop output impedances of the CCM (red line) and DCM (blue line) buck converter are given in Fig. 6, which explains explicitly the dynamic changes in Figs. 4 and 5 as discussed in Section 2 (i.e., the corresponding minor-loop gains are less than one, which implies small changes to take place in the corresponding transfer functions).

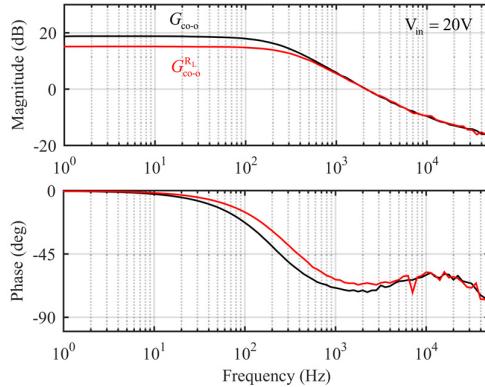


Fig.5. The experimental frequency responses of the unterminated (black line) and load-resistor-affected (red line) control-to-output-voltage transfer function of the DDR-controlled buck converter operating in DCM.

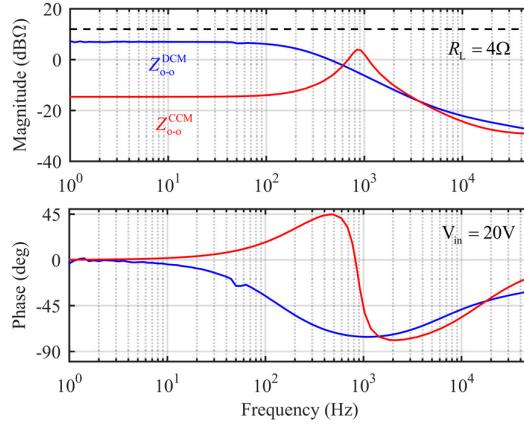


Fig. 6. The experimental unterminated frequency responses of the open-loop output impedances of the buck converter operating in CCM (red line) and in DCM (blue line) with the load resistor of 4Ω at the input voltage of 20 V.

Fig. 7 shows the simulated frequency response of the unterminated (red line) and load-resistor-affected (blue line) control-to-output-voltage transfer function of PCM-controlled buck converter operating in DCM. The frequency responses are extracted from the switching models [47] by using the PRBS method introduced in [46]. The unterminated response is computed from the measured load-resistor-affected responses by applying (9). The operating point complies with the condition $M \approx 0.5$ as discussed in Section 2.2. The existence of the RHP pole in the converter is clearly visible in Fig. 7 (i.e., red line), which is totally hided by the load-resistor effect (blue line) as well. The load-resistor effects in the PCM-controlled buck converter operating in CCM are extensively covered and presented in [45].

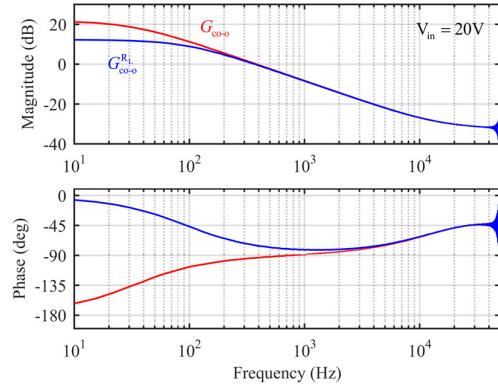


Fig. 7. The simulated frequency responses of the unterminated (red line) and load-resistor-affected (blue line) control-to-output-voltage transfer functions of the buck converter operating in DCM at the input voltage of 20 V.

Fig. 8 shows the experimentally measured output-current-feedback loop gain of the DDR-controlled buck converter (cf. Fig. 3) as unterminated (black line) and load-resistor affected (red line). Approximately one-decade reduction of the loop-gain crossover frequency is clearly visible in the figure due to the resistor loading as discussed in Section 2.3.

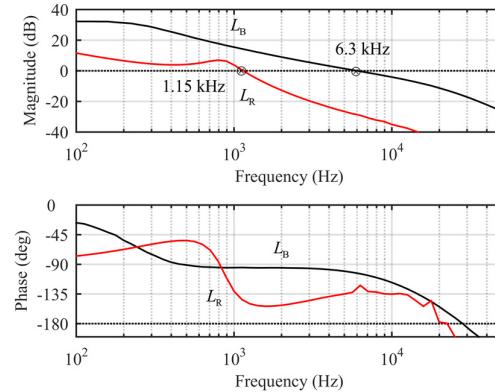


Fig. 8. The experimental frequency responses of the unterminated (black line) and load-resistor-affected (red line) output-current-feedback loop gains of the DDR-controlled buck converter operating in CCM at the input voltage of 20 V.

Fig. 9 shows the same output-current feedback-loop frequency responses as in Fig. 8, when the buck converter operates under PCM control (cf. Fig. 3). In this case, the reduction in the loop-gain crossover frequency is approximately two decades as discussed in Section 2.4.

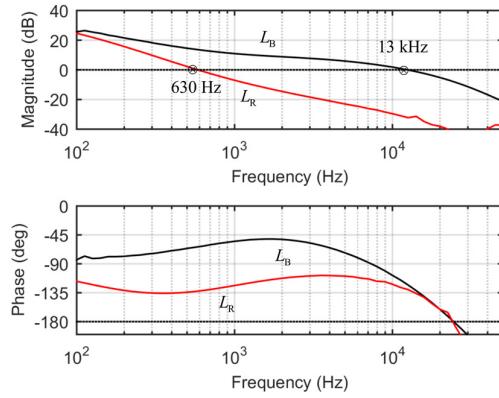


Fig. 9. The experimental frequency responses of the unterminated (black line) and load-resistor-affected (red line) output-current-feedback loop gains of the PCM-controlled buck converter operating in CCM at the input voltage of 20 V.

4. Conclusions

The small-signal modelling of the switched-mode converters have been performed usually assuming a resistor as a load. The popular text books in power electronics further promote this trend. As presented in this paper, the load-resistor-affected small-signal models can be usually used successfully for control design purposes, if the feedback-loop crossover frequency is placed at the sufficiently high frequencies (i.e., approximately at 1/10th of switching frequency or higher), and the output voltage is controlled constant. As discussed and demonstrated in this paper, there can be situations, where the load resistor hides the location of the low-frequency RHP poles, which are to be carefully considered in the control design. In case of output-current feedback control, the load-resistor hides the dynamic behaviour of the converter at the high frequencies, and therefore, the load-resistor-affected small-signal models cannot be used for control design purposes without

causing an instability to take place in practical applications. As a summary of this paper outcomes, it is highly recommend and also well justified to perform the small-signal modelling in unterminated mode to avoid problems in converter stability and transient performance. Only the unterminated small-signal models can be used for assessing the effects of the different load types in the converter dynamic behaviour.

5. References

- [1] Wester, GW., Middlebrook, RD., ‘Low-frequency characterization of switched DC-DC converters’, Proc. IEEE Power Electronics Specialists Conf., Atlantic City, NJ, USA, May 1972, pp. 9-20.
- [2] Wester, GW., Middlebrook, RD., ‘Low-frequency characterization of switched dc-dc converters’, IEEE Trans. Aerosp. Electron. Syst., 1973, AES-9, (3), pp. 376-385.
- [3] Middlebrook RD., Ćuk, S., ‘A general unified approaches to modeling switching-converter power stages’, Proc. IEEE Power Electronics Specialists Conf., Pasadena, CA, USA, June 1976, pp. 18-34.
- [4] Middlebrook, RD., Ćuk, S., ‘A general unified approach to modeling switching-converter power stages’, Int. J. Electron., 1977, 42, (6), pp. 521-550.
- [5] Hsu, SP., Brown, A., Rensink, L., et al., ‘Modeling and analysis of switching frequency of switching DC-to-DC converters in constant-frequency current programmed mode’, Proc. IEEE Power Electronics Specialists Conf., Sand Diego, CA, USA, June 1979, pp. 248-301.
- [6] Maranesi, PG., Tavazzi, V., Varoli, V., ‘Two-port characterization of PWM voltage regulators at low frequencies’, IEEE Trans. Ind. Electron., 1988, 35, (3), pp. 444-450.
- [7] Middlebrook, RD., ‘Small-signal modeling of pulse-width modulated switched-mode power converters’, Proc. IEEE, 1988, 76, (4), pp. 343-354.
- [8] Sanders, SR., Verghese, GC., ‘Synthesis of averaged circuit models for switched power converters’, IEEE Trans. Circuits Syst., 1991, 38, (8), pp. 905-915.
- [9] Ridley, RB., ‘A new continuous-time model for current-mode control’, IEEE Trans. Power Electron., 1991, 6, (2), pp. 271-280.
- [10] Tang, W., Lee, F. C., Ridley, RB., ‘Small-signal modeling of average current-mode control’, IEEE Trans. Power Electron., 1993, 8, (2), pp. 112-119.
- [11] Lehman, B., Bass, RM., ‘Switching frequency dependent averaged models for PWM DC-DC converters’, IEEE Trans. Power Electron., 1996, 11, (11), pp. 89-96.
- [12] Sun, J., Mitchell, DM., Greuel, MF., et al., ‘Averaged modeling of PWM converters operating in discontinuous conduction mode’, IEEE Trans. Power Electron., vol. 16, no. 4, pp. 482-492, Jul. 2001.
- [13] Suntio, T., ‘Analysis and modeling of peak-current-mode controlled buck converter in DICM’, IEEE Trans. Ind. Electron., 2001, 48, (1), pp. 127-135.
- [14] Qiu, Y., Xu, M., Sun, J., et al., ‘A generic high-frequency model for the nonlinearities in buck converter’, IEEE Trans. Power Electron., 2007, 22, (5), pp. 1970-1977.
- [15] Fang, CC., ‘Unified discrete-time modeling of buck converter in discontinuous mode’, IEEE Trans. Power Electron., 2011, 26, (8), pp. 2335-2342.

- [16] Qiu, Y., Chen, X., Zhong, C., et al., ‘Uniform models of PWM DC-DC converters for discontinuous conduction mode considering parasitics’, IEEE Trans. Ind. Electron., 2014, 61, (11), pp. 6071-6080.
- [17] Di Capua, G., Shirasavar, SA., Hallworth, MA., et al., ‘An enhanced model for small-signal analysis of the phase-shifted full-bridge converter’, IEEE Trans. Power Electron., 2015, 30, (3), pp. 1567-1576.
- [18] Smithson SC., Williamson SS., ‘A unified state-space model of constant-frequency current-mode-controlled power converters in continuous conduction mode’, IEEE Trans. Ind. Electron., 2015, 62, (7), pp. 4514-4524.
- [19] Amir, S., van der Zee, R., Nauta, B., ‘An improved modeling and analysis technique for peak current-mode control-based boost converters’, IEEE Trans. Power Electron., 2015, 30, (9), pp. 5309-5317.
- [20] Veerachary, M., ‘Analysis of minimum-phase fourth-order buck DC-DC converter’, IEEE Trans. Ind. Electron., 2016, 63, (1), pp. 144-154.
- [21] Das, M., Agarwal, V., ‘Generalized small signal modeling of coupled-inductor-based high-gain high-efficiency DC-DC converter’, IEEE Trans. Ind. Appl., 2017, 53, (3), pp. 2257-2270.
- [22] Zhang, Y., Li, D., Lu, H., et al., ‘Analysis and implementation of a high-performance-integrated KY converter,’ IEEE Trans. Power Electron., 2017, 32, (12), pp. 9051-9064.
- [23] Erickson, RW., Maksimović, D., ‘Fundamentals of Power Electronics’, (Kluwer Academic Publishers, 2001, 2nd edn).
- [24] Krein, PT., ‘Elements of Power Electronics’, (Oxford University Press, 2014, 2nd edn).
- [25] Choi, B., ‘Step load response of a current-mode-controlled DC-to-DC converter,’ IEEE Trans. Aerosp. Electron. Syst., 1997, 33, (4), pp. 1115-1121.
- [26] Li, P., Lehman, B., ‘Performance prediction of DC-DC converters with impedances as loads’, IEEE Trans. Power Electron., 2004, 19, (1), pp. 201-209.
- [27] Pidaparthi, SK., Choi, B., ‘Designing control loop for PWM converters in Dc-to-Dc power conversion’, Proc. IEEE Ind. Electron. Society Annual Conf., Dallas, TX, USA, Nov. 2014, pp. 5094-5100.
- [28] Pidaparthi, SK., Choi, B., ‘Control design and loop gain analysis of DC-to-DC converters intended for general load subsystems’, Mathematical Problems in Engineering, 2015, 2015, pp. 1-9.
- [29] Suntio, T., ‘Dynamic Profile of Switched-Mode Converter – Modeling, Analysis and Control’, (Wiley-VCH, 2009).
- [30] Suntio, T., Messo, T., Puukko, J. ‘Power Electronic Converters – Dynamics and Control in Conventional and Renewable Energy Applications’ (Wiley-VCH, 2017).
- [31] Suntio, T., Karppanen, M., Sippola,M., ‘Methods to characterize open-loop dynamics of current-mode-controlled converters’ Proc. IEEE Power Electronics Specialists Conf., Rhode Island, Greece, Jun. 2008, pp. 636-642.
- [32] Suntio, T., Viinamäki, J., Jokipii, J., et al., ‘Dynamic characterization of power electronic interfaces’, IEEE J., Emerg. Sel. Topics Power Electron., 2014, 2, (4), pp. 949-661.
- [33] Vesti S., Suntio, T., Oliver, JA., et al., ‘Effect of control method on impedance-based interactions in a buck converter’, IEEE Trans. Power Electron., 2013, 8, (11), pp. 5311-5322.
- [34] Suntio, T., Gadoura, I., ‘Dynamic analysis of switched-mode converters using two-port modelling technique’, Proc. Power Conversion and Intelligent Motion Conf., Nuremberg, Germany, May 2002, pp. 387-392.

- [35] Suntio, T., Gadoura, I., ‘Use of unterminated two-port modeling technique in analysis of input filter interactions in telecom DPS systems’, Proc. IEEE International Telecom. Energy Conf., Montreal, Canada, Sept./Oct. 2002, pp. 560-565.
- [36] Suntio, T., ‘Unified average and small-signal modeling of direct-on-time control’, IEEE Trans. Ind. Electron., 2006, 53, (1), pp. 287-295.
- [37] Cvetkovic, I., Boroyevich, D., Mattavelli, P., et al., ‘Unterminated small-signal behavioral model of DC-DC converters’, IEEE Trans. Power Electron., 2013, 28, (4), pp. 1870-1879.
- [38] Hankaniemi, M., Suntio, T., ‘Small-signal models for constant-current regulated converters’ Proc. International Telecom. Energy Conf., Providence, RI, USA, Sept. 2006, pp. 2037-2042.
- [39] Hankaniemi, M., Suntio, T., ‘Small-signal models for constant-current regulated converters’ Proc. IEEE Industrial Electronics Society Annual Conf., Paris, France, Nov. 2006, pp. 2037-2042.
- [40] Middlebrook, RD., ‘Null double injection and extra element theorem’, IEEE Trans. Educ., 1989, 32, (3), pp. 167-180.
- [41] Middlebrook, RD., ‘Design techniques for preventing input-filter oscillations in switched-mode regulators’, Proc. IEEE National Solid-State Power Conversion Conf., San Fransico, CA, USA, May 1978, pp. A3.1-A3.16.
- [42] Middlebrook, RD., ‘Input filter considerations in design and application of switching regulators’, Proc. IEEE Industry Application Society Annual Conf., Chicago, Illinois, USA, Oct. 1976, pp. 91-107.
- [43] Suntio, T., Hankaniemi, M., ‘Unified small-signal model for PCM control in CCM – Untermminated modeling approach’, HIT J. Science Eng. B, 2005, 2, (3-4), pp. 452-475.
- [44] Suntio, T., Hankaniemi, M., Roinila, T., ‘Dynamical modeling of peak-current-mode-controlled converter in continuous conduction mode’, J. Simul. Modeling Pract. Theory, 2007, 15, (10), pp. 1320-1337.
- [45] Suntio, T., ‘On dynamic modeling of PCM-Controlled Converters – Buck converter as an example’, IEEE Trans. Power Electron., 2017 (DOI: 10.1109/TPEL.2017.2737679) (in press).
- [46] Roinila, T., Vilkko, M., Suntio, T., ‘Fast loop gain measurement of switched-mode converter using binary signal with specified Fourier amplitude spectrum’, IEEE Trans. Power Electron., 2009, 24, (12), pp. 2746-2755.
- [47] Suntio, T., Kivimäki, J., ‘Physical insight into the factors affecting the load-transient response of a buck converter’, Proc. European Conf. on Power Electronics and Applications, Lappeenranta, Finland, Aug. 2014, pp. 1-10.