

Combination of E-jet and inkjet printing for additive fabrication of multilayer high-density RDL of silicon interposer

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Abstract— The additive nature and high resolution of electrohydrodynamic inkjet (E-jet) printing can be utilized for manufacturing micron scale conductive tracks such as those required in the high-density redistribution layers (RDL) of silicon interposers used in electronics packaging for 3D integration. Compared to the current lithographic fabrication method, this approach promises to increase the customizability of process and to reduce the amount of waste materials, thereby lowering the costs and environmental impact of the manufacturing process. In this study, multilayer interdigitated capacitor and meander resistor structures with 5/5 μm conductor width/spacing (W/S) are used to demonstrate the feasibility of E-jet printing of high-density multilayer RDLs. A sheet resistance of 28.5 $\text{m}\Omega/\text{square}$ was achieved for the first metallization layer (MET1) conductors and 313.2 $\text{m}\Omega/\text{square}$ for the MET2 conductors. The thickness of the conductors was 6.9 μm for MET1 and 5.4 μm for MET2.

Index Terms— Additive manufacturing, printed electronics, E-jet printing, high-density printing, electronics packaging, silicon interposer, 3D integration

I. INTRODUCTION

The direct deposition of functional inks by inkjet technology has been recognized as a potential candidate for reducing the costs and environmental impact of electronics manufacturing. The non-contact, on-demand deposition of controlled amounts of material on substrates ranging from stiff ceramics and metals to bendable and stretchable plastics demonstrates the flexibility of this technology [1]. So far, however, the main research effort on inkjet-based manufacturing has concentrated on the fabrication of low cost, large area devices such as antennas for RFID tags [2], sensors for body-monitoring purposes (temperature [3], chemicals [4], ECG [5] etc.) or solar cells for photovoltaic applications [6]. Meanwhile, progress towards low-cost, small-area applications has been hindered by the limited resolution of the conventional, thermal- and piezo-based inkjets. Although their resolution can be improved further by decreasing the spreading of the ink with techniques such as increasing the substrate temperature [7] or manipulating the substrate surface energy [8], the ultimate width of these conductors is still approximately 20 microns [1].

This might be enough when printing connections between the chips and printed circuit boards (e.g Chip-on-Board [9]) or between the chips and the package (e.g System-in-Package [10]), but it is not small enough for the high-density redistribution layers (RDLs) of silicon interposers, for which conductors with sub-ten micron width and spacing are required [11].

The silicon interposers are one of the main technologies enabling 3D integration and the further miniaturization of electronics packages. The purpose of the interposer is to reroute the signal paths from the high-density I/Os of the device (for example an IC-chip or a MEMS device) to the low-density I/Os of the package [12]. Fig. 1. shows the structure of the interposer: it consists of through silicon vias (TSVs) penetrating the Si-substrate and the multilayer RDL connecting the TSVs to the device I/O bumps. Currently, a complicated multi-step lithographic process is used for creating such structures. It involves the use of hazardous etching chemicals and produces a significant amount of waste material [12]. The benefits of additive manufacturing are therefore apparent: reduced consumption of materials; reduced environmental impact and an altogether simpler and more flexible process.

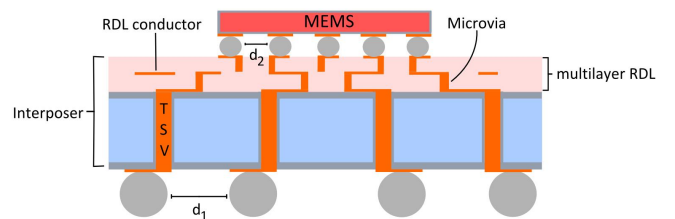


Fig. 1. Interposer to close the pitch gap ($d_1 \gg d_2$) between the I/O bumps of the device and the package.

Recently, high-resolution electrohydrodynamic inkjet (E-jet) technology has emerged as a viable alternative for dispensing minuscule amounts of ceramic [13], dielectric [14] or conductive materials [15] with a large range of viscosity (0.1 $\text{mPa}\cdot\text{s}$ to 10000 $\text{mPa}\cdot\text{s}$ [16]). The E-jet is capable of producing variable droplet sizes ranging down to sub-femtoliter volumes, thus allowing the additive fabrication of sub-micron conductive

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traces [15][16]; this makes it a potential alternative for fabricating the conductors of the high-density RDL. The rapid evaporation of the small droplets also enables the printing of pillar structures with diameters as small as $3\ \mu\text{m}$ [18], which could be used for fabrication of RDL microvias with diameters well below the current industry standard of $20\ \mu\text{m}$ [11]. However, many research groups have remarked on the challenging process control needed for the E-jet equipment, especially when printing on dielectric substrates where charge accumulation may occur. Such charging has been observed to cause droplet deflection and even droplet explosion during flight [19]. Such printing artifacts can, therefore, be detrimental to the electrical behavior of the circuitry and the reliability of the device.

Regarding the silicon interposers, E-jet technology has already been used for filling high density TSVs [20] and printing narrow Ag-conductors of varying thickness on silicon substrates [21]. This research studies the additive fabrication of multilayer high density RDLs. This is achieved by printing three test vehicles, each investigating one specific functional requirement of the RDL:

1. A multilayer interdigitated capacitor (IDC) with five micron conductor width and five micron spacing between the conductors ($W/S = 5/5\ \mu\text{m}$) to detect short circuits
2. A multilayer meander resistor (MR) structure with $5/5\ \mu\text{m}$ W/S for detecting open circuits and determining the sheet resistance
3. A microvia to demonstrate the electrical connection between the metallization layers

The W/S-values indicate the target widths of the design; the true widths of the conductors differ from this due to calibration process tolerance.

II. FABRICATION AND CHARACTERIZATION EQUIPMENT

The E-jet printer which was used to print the high-density conductors was a commercially available device, Super Inkjet, developed by SIJTechnology Inc., Japan. A schematic of the device's print head is shown in Fig. 2.

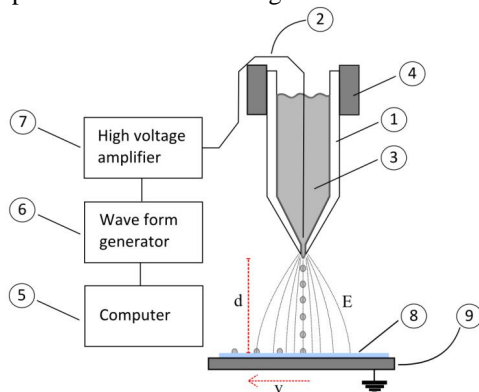


Fig. 2. Schematic of E-jet print head. E denotes the electric field and d the distance between the ink meniscus and the grounded xy-stage; v is for the velocity of the xy-stage or printing speed. The explanation for the numbered items is given below.

The print head consists of a glass capillary (1) which also acts as an ink chamber (3). During operation, the ink is charged using a charging electrode (2) whereby a potential difference between the ink meniscus and grounded xy-stage (9) is generated. When the strength of the electric field between the meniscus and the substrate (8) exceeds a threshold value, an ink droplet is pulled out. The voltage is controlled via the computer (5) and the waveform generator (6). The geometry of the printed pattern is determined by a vector-based print file which controls the movement of the xy-stage. This is in contrast to conventional inkjet technology which uses raster patterning and means that the resolution does not depend on the printing direction in similar fashion as in conventional inkjet printers. The movement resolution of the xy-stage is the same in both x- and y-directions ($0.1\ \mu\text{m}$). [22]

The operator can control the volume of the ejected droplets by manipulating the electric field (E), which depends on the voltage DC-level (V_{bias}) and peak value (V_{max}); and distance between the nozzle tip and the substrate (d). In addition to droplet volume, the dimensions of the printed pattern also depend on the relationship between the frequency of droplet ejection (f) and the printing speed (v) [7].

SIJ was used to print the conductive structures i.e. the high density conductors and the microvia pillars; the Super Fine nozzle (SIJ Technology) and gold nanoparticle ink Au Nanometal (ULVAC Inc, Japan) were used for this purpose. The dielectric layers for the IDC, MR and microvia structures were deposited with a Dimatix material printer (DMP-2831) using a DMC 10p1 cartridge and RUV-4001 UV-curable ink (SIJ Technology).

The UV-curing of the RUV-4001 was done with a DYMAX BlueWave 75 UV curing spot lamp using a radiant exposure of approximately $6000\ \text{mJ}/\text{mm}^2$.

Two-point measurements were performed for the IDC and MR structures using a Keysight Semiconductor Device Analyzer B1500A. The four-point resistance measurements for the microvia structures were performed using the Keithley 2400 multimeter.

The cross sections of the MR structure were fabricated using a silicon carbide cutting tool for the rough cut and broad ion beam (BIB) milling (Ilion Advantage PCSS, Gatan, Inc.) to create a defect-free cross-sectional surface; the ion beam was generated using argon gas and a 6 kV accelerating voltage. The thicknesses, widths and cross-sectional areas of the MR conductors were then determined using SEM and ImageJ image analysis software (version 1.50i).

III. TEST VEHICLE DESIGNS

A. Short and open circuit testing

The short-circuit detection test vehicle consists of interdigitated capacitors (IDC) in two metallization layers (MET1 and MET2) separated with a dielectric layer, as shown in Fig 3.1. The conductor width/spacing (W/S) is $5/5\ \mu\text{m}$.

The open-circuit detection test vehicle consists of meander resistors (MR) in both MET1 and MET2, with a dielectric in between, as shown in Fig 3.2. The W/S of this test vehicle is also $5/5\ \mu\text{m}$. The conductor length is $37930\ \mu\text{m}$.

B. Microvia

The electrical connection between the MET1 and MET2 is demonstrated using the microvia structure shown in Fig 3.3. The pillar diameter is 10 μm and the conductor width 5 μm . Two conductors in MET1 and MET2 are used to connect the microvia, which enables an accurate determination of the via resistance with a four-point resistance measurement set-up.

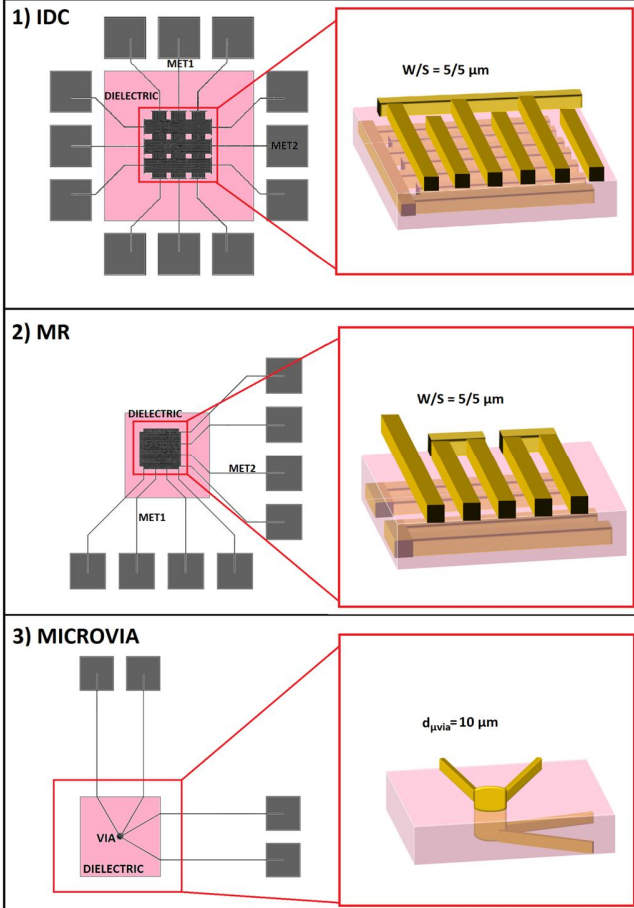


Fig. 3.1 Multilayer IDC and Fig. 3.2. MR structures both with $W/S = 5/5 \mu\text{m}$ for detecting short and open circuits. Fig. 3.3. Microvia test structure for measuring microvia resistance; microvia diameter is approximately 10 μm . Note that the dimensions of the dielectric layer, conductors and the microvia are not to scale.

IV. TEST VEHICLE FABRICATION

The test vehicles were fabricated by combining E-jet printing with conventional piezo-based inkjet technology. The E-jet-printed MET1 and MET2 conductors were printed with gold nanoparticle ink Au Nanometal, whereas the conventional inkjet-printed dielectric layer was printed with UV-curable dielectric ink RUV-4001. The material and processing parameters for the inks are given in Tables 1 and 2.

TABLE 1
ULVAC AU NANOMETAL INK PARAMETERS [23]

Parameter	Value
Solid content	50 wt%
Sintering conditions	250°C for 60 min
Resistivity	8 $\mu\text{Ohm}\cdot\text{cm}$
Solvent	Cyclododecene
Viscosity	10 mPa·s
Surface tension	27 mN/m

TABLE 2
RUV-4001 UV-CURABLE DIELECTRIC INK PARAMETERS [24]

Parameter	Value
Material	Epoxy resin
Solvent	2-n-Butoxyethylacetate
Pre-bake	80°C for 5 min
UV-curing	6000 mJ/mm ²
Hard-bake	180°C for 60 min
Viscosity	11.8 mPa·s
Surface tension	23.4 mN/m
Resistivity	$2.3 \cdot 10^6 \text{ Ohm}\cdot\text{cm}$

A. Structures for short and open circuit testing

The multilayer IDC and MR structures were fabricated on top of 675 μm thick silicon wafers covered with a 1.4-micron thermally deposited silicon oxide layer and a 0.1-micron sputtered Ti/W-layer on top (Silex Microsystems Ab, Sweden). The top layer acts as an adhesion promoter between the printed gold conductors and the silicon oxide, while simultaneously preventing the diffusion of metal atoms into the semiconducting bulk. The etching of Ti/W is the only subtractive step in the IDC and MR fabrication process, as shown in Fig. 4.

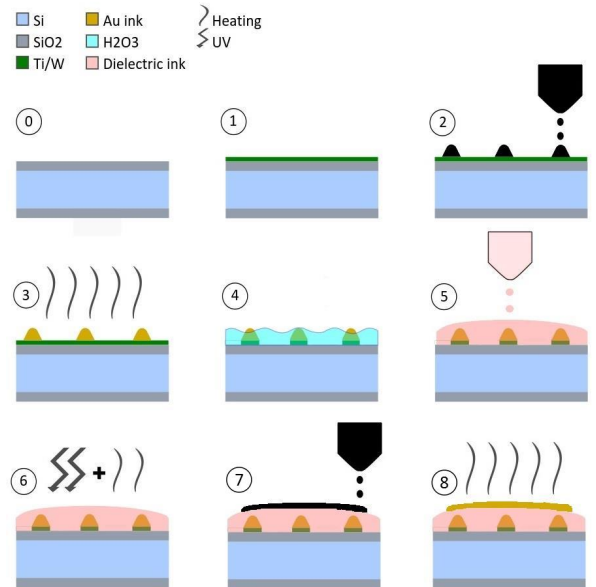


Fig. 4. Fabrication process of multilayer IDC and MR structures. Explanation for the numbered items is given below.

The fabrication process begins with the thermal oxidation of the silicon wafer (0), and the sputtering of the Ti/W adhesion promoter/diffusion barrier (1). The gold conductors of MET1 are then printed in step (2) using the E-jet printer and gold

nanoparticle ink, Au Nanometal. Since the height of a single E-jet-printed line is measured in tens of nanometers, multiple layers need to be printed to achieve conductivity [21]; in this case 70 layers were used. The lines deposited by the E-jet are then sintered at 250°C for one hour (3). This step causes the polymer capping layer of the nanoparticles to disintegrate which, in turn, enables the nanoparticles to diffuse into each other, thereby creating a porous, yet conductive microstructure [25]. The sintering is followed by etching of the Ti/W-layer with hydrogen peroxide (4); the conductors are unaffected by the etchant due to the inertness of gold. This is followed by deposition of the UV-curable dielectric ink, RUV-4001. Since the resolution in this printing step does not need to be as high as in the case of the high-density conductors, a conventional piezo-based inkjet, Dimatix DMP-2831, could be used to make the process faster (5). The dielectric ink layer is pre-baked at 80°C for 5 minutes to evaporate the solvent, UV-cured with a 6000 mJ/cm^2 dose to induce cross-linking, and hard-baked at 180°C for one hour to improve its chemical and structural stability (6). This is followed by repeating steps (2) and (3) on top of the dielectric in order to fabricate the MET2 conductors. 60 layers were printed in order to achieve the necessary thickness.

The print parameters for the E-jet printed MET1 and MET2 conductors are given in Table 3. Before each print, the line width was calibrated to approximately 5 μm using the procedure explained in [21]. Therefore, the V_{max} varies and is not listed in Table 3.

TABLE 3
E-JET PRINT PARAMETERS FOR MET1 AND MET2 OF MULTILAYER IDC AND MR STRUCTURES

Parameter	IDC MET1	IDC MET2	MR MET1	MR MET2
V _{bias} (V)	250	0	250	0
v (mm/s)	0.3	0.3	0.3	0.3
f (Hz)	1000	140	1000	140
d (μm)	50	50	50	50

Table 4 shows that the print parameters of the MET2 conductors differ notably from the parameters used for MET1. Since the MET1 conductors are printed on conductive Ti/W, there is no charge accumulation on top of the substrate and a unipolar voltage with high frequency can be used. However, when printing on top of the dielectric surface, charge compensation must be performed in order to prevent charge accumulation on the substrate and the concomitant print artifacts. This is achieved by printing the droplets alternately with a positive and a negative charge i.e. using bipolar voltage [26]. The droplet ejection frequency is twice the frequency of the driving voltage since both the negative and positive parts of the pulse will result in droplet ejection.

B. Microvia

The microvia structure was fabricated on similar silicon wafers using the same functional inks: Au Nanometal and RUV-4001.

The fabrication process is shown in Fig. 5.

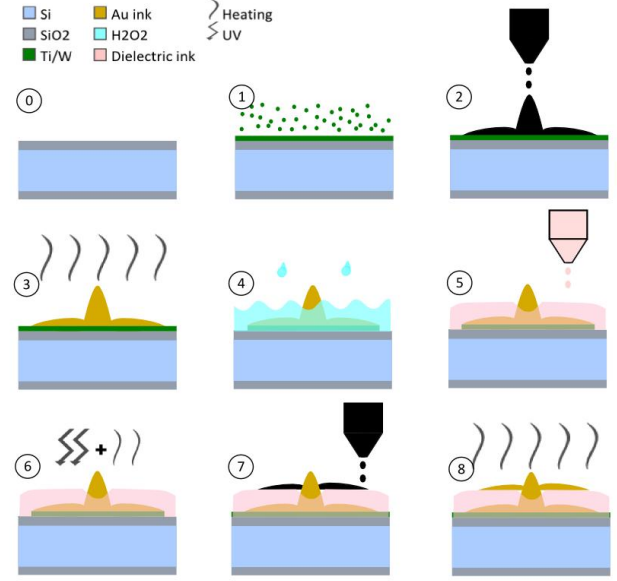


Fig. 5. Fabrication process of the microvia. Explanation for numbered items is given below.

Steps (0) and (1), the thermal oxidation and the Ti/W-sputtering of the silicon wafer, are the same as for the IDC and MR test vehicles. Au Nanometal ink is then deposited with the E-jet to fabricate the MET1 conductors and a pillar which will form the conductive filling of the microvia (2). Printing the pillar utilizes the fact that the evaporation rate of the solvent increases with the increasing surface area/volume ratio of the in-flight droplets. Since the volume of a single E-jet printed droplet is measured in femtoliters, the resulting evaporation rate is fast enough to cause most of the solvent to have already evaporated during the flight. This will result in the formation of a pillar, rather than a continuously-spreading ink puddle [18]. To further enhance the evaporation, a layer-by-layer approach was used. The diameter of the pillar is controlled by varying the voltage, and its height by varying the total ejection time. A larger diameter for the pillar should make it more robust against any mechanical stresses which may take place during the Ti/W-etching, or the printing of the dielectric layer. The pillar must be high enough to penetrate the dielectric layer. After printing the pillar and conductors, the printed structure is sintered (3) and the Ti/W-layer is removed with hydrogen peroxide (4). This is followed by deposition of the RUV-4001 (5) ink with the piezo-based inkjet, DMP-2831. In step (6) the RUV-4001 ink is pre-baked, UV-cured and hard-baked to increase the thermal and chemical stability of the cross-linked polymer structure. MET2 conductors are then printed on top of the dielectric by repeating steps (2) and (3) to connect the microvia to the MET2 measurement pads.

The E-jet print parameters for the microvia pillar are given in Table 4.

TABLE 4
E-JET PRINT PARAMETERS FOR THE MICROVIA PILLAR

Parameter	SAMPLE1	SAMPLE2	SAMPLE3	SAMPLE4
Jetting time per layer	1 s	1.5 s	2 s	2.5 s
Drying time between layers	1 s	1.5 s	2 s	2.5 s
Total jetting time	50 s	75 s	100 s	125 s

V. RESULTS AND ANALYSIS

A. Structures for short and open circuit testing

Optical microscope images of the multilayer IDC structure for short-circuit testing are shown in Fig. 6: pictures (a) and (b) show the situation after sintering the MET1 conductors and etching the Ti/W whereas (b) and (c) show the situation after all the process steps have been completed.

Based on Fig 6 (b), which shows the middle of a MET1 IDC, it seems that the conductor edge roughness is an issue for multilayer conductors. It is also apparent that there has been some misalignment towards the left between printing the top and bottom parts of the middle MET1 IDC. Picture (d), the top MET2 IDC, shows another type of misalignment. Here, the previously-printed conductor on one side (second conductor from the bottom) pulls the jet towards itself. However, if there are previously printed conductors on both sides, there is no corresponding change in the jetting direction. It seems that the previously printed conductors distort the electric field and this, in turn, will deflect a droplet's flight path.

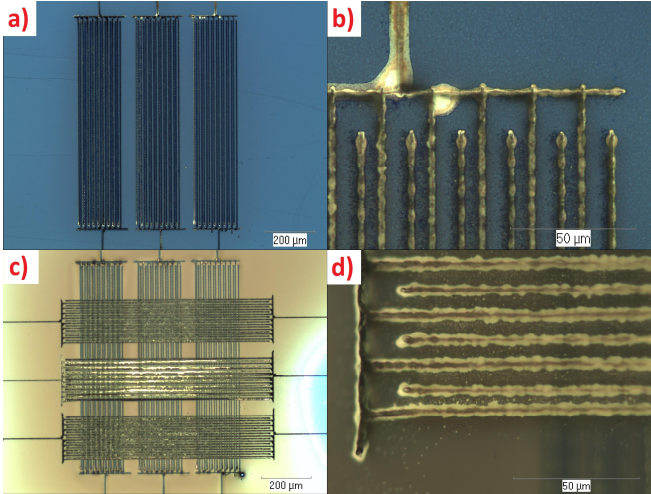


Fig. 6. Multilayer IDC for detecting short circuits: a) MET1 IDCs after removing the Ti/W layer (10X magnification); b) high magnification image of upper part of MET1 middle IDC (100X); c) MET2 IDCs after sintering (10X) and d) high magnification image of left part of MET2 top IDC (100X).

The resistance measurements showed that while there were no short circuits in the MET1 IDCs, in MET2 only the top capacitor has been printed without short circuits. Additionally, the left part of MET2 middle IDC had only three layers, and the

resistance measurement indicated an open circuit because of this. Visual inspection with a microscope showed that there was significant overlapping of the subsequent conductors which indicates that a small number of layers is not necessarily enough to achieve conductivity; similar results were achieved previously in [21].

The MR structure for open circuit testing is shown in Fig. 7. The inset of the upper picture shows Sample 1 before cutting, and the SEM image after cutting the sample. The lower pictures of Fig 7 show high magnification SEM images (15000X) of the MET1 and MET2 cross-sections.

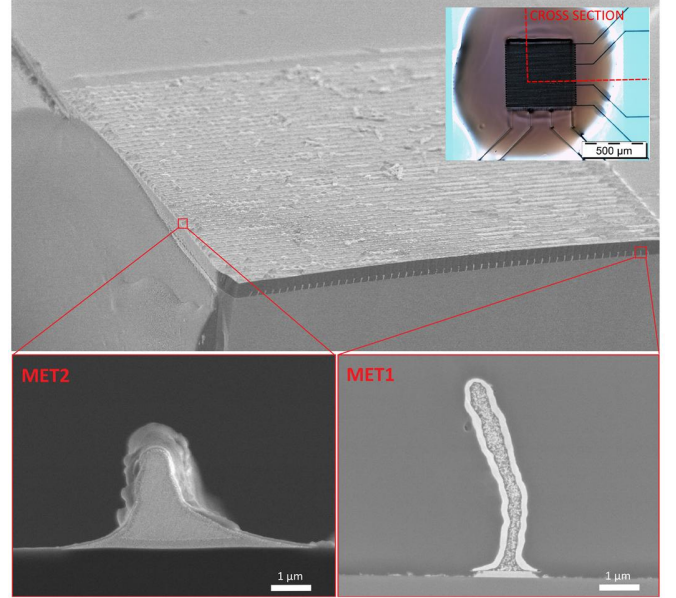


Fig. 7. MR structure for open-circuit testing (Sample 1). Inset of upper picture: sample before BIB cross-section. Upper picture: low magnification (170X) SEM image of the sample after BIB milling. Lower pictures: high magnification (15000X) SEM images of the MET2 and MET1 conductor cross-sections.

Based on Fig. 7. the MET2 conductors seem to have spread more during printing than the MET1 conductors. This is probably caused by the higher evaporation rate of the smaller droplets which were used to print the MET1 conductor. The morphologies of the MET1 and MET2 conductors seem to differ as well: the MET1 conductors have a dense, shell-like structure surrounding the central part of the conductor whereas the MET2 conductors have a more homogenous composition. During fabrication there is one key difference between MET1 and MET2, which could contribute to this type of behavior. The MET1 conductors undergo three heat treatments, compared to only one treatment for MET2 (sintering of MET1, hard baking of the dielectric and sintering of MET2).

Table 5 shows the average conductor width, thickness and cross sectional area for both MET1 and MET2, along with their respective resistance measurements. A two-point resistance measurement was deemed sufficient since the error resistance of the leads and measurement pads is very small compared to the overall resistance of the structure ($< 1\%$). The dimensions of the conductor were measured from the SEM pictures as an average of ten cross-sections using ImageJ image analysis tool. The cross-sectional area was measured by tracing the edges of

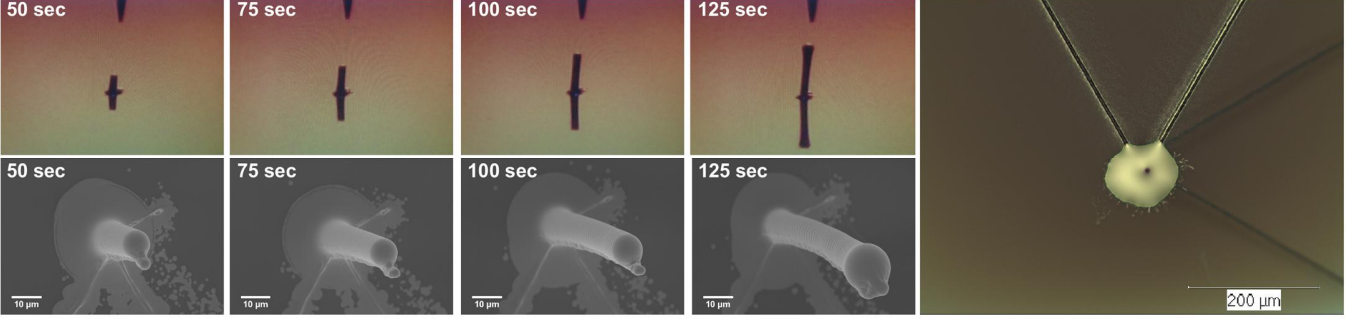


Fig. 8. Microvia pillars after deposition (optical image, first row) and after sintering (SEM image, second row). The pillar height is controlled by the total jetting time; for height reference, the distance between substrate surface and nozzle tip is 200 μm . The picture on the far right shows the Sample 1 after printing and sintering the MET2 conductors.

the conductor manually and measuring the enclosed area with the ImageJ area measurement function.

Both, the MET1 and MET2 MRs seem to be conductive, i.e. no open circuits could be detected. The sheet resistance of the conductors was calculated using the formula

$$R_{sheet} = R * \frac{W}{L} \quad (1)$$

where W is the width of the conductor and L the length (37930 μm). The resulting values for Sample1 and Sample 2 are shown in Table 5. Because the conductor cross-section is non-rectangular, the resistivity (ρ) has to be calculated using the formula:

$$\rho = R * \frac{A}{L} \quad (2)$$

where A is the cross-sectional area and L the length of the conductor. The resulting resistivity values for MET1 and MET2 of Sample 1 and Sample 2 are also listed in Table 5.

TABLE 5
DIMENSIONS AND ELECTRICAL CHARACTERISTICS OF THE MULTILAYER MR CONDUCTORS. THE LENGTH OF THE CONDUCTORS IS 37930 MICROMETERS.

Parameter	SAMPLE1		SAMPLE2	
	MET1	MET2	MET1	MET2
Width (μm)	2.1	4.9	2.0	5.5
Thickness (μm)	5.4	3.2	6.9	5.6
Cross-sectional area (μm^2)	4.5	5.2	5.6	8.0
Resistance (Ω)	800	3220	540	2160
Sheet resistance ($\text{m}\Omega/\text{square}$)	44.3	458.4	28.5	313.2
Resistivity ($\mu\Omega*\text{cm}$)	9.6	44.5	8.0	45.4

Despite the unconventional morphology of the MET1 conductors, the calculated resistivity values correspond well with the datasheet value of 8.0 $\mu\Omega*\text{cm}$. This value is still approximately three times higher than the resistivity of bulk gold (2.44 $\mu\Omega*\text{cm}$ [27]) since the nanoparticle conductors contain the remains of surfactants and the true cross-sectional

area of the conductor is lower because of the porosity of the material [28]. Generally, the resistivity of the nanoparticle conductors depends on the drying and annealing process. In oven sintering, the key parameters are temperature and time [23][29].

The MET2 conductors, however, have significantly higher resistivity when compared to the datasheet value. In a previous study [30], it was found that if the hard baking temperature of the polymer substrate is less than the sintering temperature of the printed conductors, there will be significant outgassing during the sintering phase and the resistivity of the conductors will therefore be higher. In this case, the hard baking temperature of the dielectric was 70 $^\circ\text{C}$ lower than the sintering temperature of the Au Nanometal ink. Additionally, there is a large CTE mismatch between the epoxy-based dielectric layer (45 to 65 ppm/K) and gold (14 ppm/K). This can cause delamination and cracking of the printed gold conductors, thereby increasing their resistance.

B. Microvia

Four microvias were printed using the process described in the previous section. The first row of Fig. 8. shows the optical images of the four samples taken with a side-view camera after deposition (for scale, the tip of the nozzle is approximately 200 μm from the substrate surface). The second row shows the respective SEM images taken after sintering and etching of the Ti/W. The right-most picture shows the complete microvia after printing and sintering the MET2 conductors. An ink puddle was printed on top of the pillar to ensure connection.

The height of the pillars was calculated from the SEM images shown in Fig. 8. using the formula:

$$h = \frac{m}{\sin(\alpha)} \quad (3)$$

where h is the true height of the pillar, m the measured height along tilt axis and α the tilt angle. It must be noted, however, that there is a slight tilt in the pillars themselves which will lead to an error in the measurement. Therefore, the values stated in Table 6 are only rough approximations of the true height. Table 6 also shows the resistance values for the microvia samples as measured with the 4-point measurement approach.

TABLE 6
APPROXIMATE HEIGHT OF THE PILLARS AND 4-POINT RESISTANCE
MEASUREMENTS FOR MICROVIA STRUCTURES

	SAMPLE1	SAMPLE2	SAMPLE3	SAMPLE4
Total jetting time (s)	50	75	100	125
Height (μm)	40	60	90	110
Resistance ($m\Omega$)	410	950	410	360

The resistance values seem to be independent of the height of the pillar. The apparent reason for this is that the thickness of the dielectric layer was not optimized for any particular pillar height. The electrical connection between the MET2 conductors and the pillar can therefore occur anywhere along the height of the pillar, i.e. the resistance measurement is not necessarily between the bottom and the top of the pillar. Furthermore, the resistance of the Sample 2 is over two times higher compared to the other samples. This is likely caused by poor electrical contact between the MET2 conductors and the pillar.

VI. CONCLUSION

Although E-jet printing is capable of producing conductors with very narrow line widths and a high aspect ratio, it seems that the multilayer printing approach results in significant edge and surface roughness. Additionally, the conductor's cross-sectional area will be smaller than its photolithographically fabricated counterpart of similar width. Therefore, its sheet resistance will be higher. However, if these challenges are set aside, the results show that the additive manufacturing of multilayer RDLs is possible: we have demonstrated that, high-density prints can be done on conductive and dielectric substrates without short or open circuits using $5/5 \mu\text{m}$ W/S and it is also possible to fabricate a $10 \mu\text{m}$ diameter microvia between the metallization layers.

The lowest sheet resistance value for the MET1 conductors was $28.5 \text{ m}\Omega/\text{sq}$ and lowest resistivity $8.0 \mu\Omega\cdot\text{cm}$; for MET2, the corresponding values were $313.2 \text{ m}\Omega/\text{sq}$ and $44.5 \mu\Omega\cdot\text{cm}$; the lowest measured microvia resistance was $360 \text{ m}\Omega$. For example, with a silicon interposer fabricated using conventional methods (i.e. laser drilling of microvias and Cu-electroplating of microvia and conductors), one to three Ohm through path resistance has been reported [31]. Since the resistance of TSV is quite low ($10.3 \pm 2.4 \text{ m}\Omega$), RDL microvias and conductors must make up most of the reported resistive losses. For E-jet printed MET1 conductors three Ohms corresponds to 105 squares and for MET2 conductors 10 squares. Taking into account the high microvia resistance, it is clear that the routing should be done preferably in MET1.

The results presented in this manuscript indicate that E-jet can be used for RDL fabrication. However, further development and optimization in patterning and material processing is required. Especially, the scaling of the fabrication process must be addressed.

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