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**Issues in Discontinuous Space-Vector Modulation and
Grid-Current Control of Three-Wire Three-Level Static
Synchronous Compensator**



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Abstract

In modern power systems, the quality of electric power should be maintained within statutory limits and tolerances to enable normal and uninterrupted operation of the load equipment in their electrical environment. However, the severity of power quality problems, as well as the frequency of their occurrence, has been in continuous increase because of growing energy consumption, proliferation of non-linear loads, and the sensitivity of modern loads to electromagnetic disturbances in the networks. Therefore, more efficient and faster-acting power quality conditioners are needed. Currently the broadest operating range and the fastest dynamics are provided by solid-state power quality conditioners based on pulse-width modulated power converters. Considering high power and medium to high voltage applications, the multilevel converter topologies have gained special interest because they can generate low-harmonic voltage and current waveforms by using lower switching frequencies and with no need for complex transformer circuits.

This thesis studies the digital control of a STATCOM (static synchronous compensator) based on the three-wire three-level neutral-point-clamped rectifier. The focus is on the control system functions that primarily determine the dynamic behaviour and the performance of the compensator. The main addressed research issues are the pulse-width modulation strategy and the grid current control, using a suitable combination of fundamental theory, computer-aided modelling and simulations, and laboratory experiments.

A discontinuous space-vector modulation algorithm is implemented for a three-level STATCOM. Space-vector theory is used to analyse the effect of switching sequence arrangement on the switching ripple current. It is revealed that the sequences should be arranged according to a specific method to maintain sinusoidal grid currents when an *LCL* grid interface filter is used. Furthermore, the output voltage distortion caused by the blanking times and the semiconductor voltage losses is studied and a compensation algorithm is developed. After that, two grid current control strategies are analysed by means of dynamic modelling and simulations. The main problems observed are poor capability to reject low-order grid voltage harmonics and the sensitivity to parametric uncertainties. The presented theoretical considerations are validated with laboratory tests of a 10 kVA three-wire three-level STATCOM prototype.

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Nomenclature

Abbreviations

AC	alternating current
AD	analogue-to-digital
CSC	current source converter
CPU	central processing unit
DC	direct current
DI/O	digital input/output
DLPF	discrete-time low-pass filter
DPWM	discontinuous pulse-width modulation
DSOGI	dual second-order generalised integrator
DSP	digital signal processor
DVR	dynamic voltage restorer
EN	European standard
EPRI	Electrical Power Research Institute
FACTS	flexible alternating current transmission systems
FFT	fast Fourier transform
FLL	frequency-locked loop
FPGA	field-programmable gate array
FWD	free-wheeling diode
GAL	generic array logic
GPC	giga processor card
GTAI	giga-transceiver analogue input
GTAO	giga-transceiver analogue output
GTDI	giga-transceiver digital input
GTIO	giga-transceiver input/output
GTO	gate turn-off (thyristor)
HIL	hardware-in-the-loop

I/O	input/output
IDVR	interline dynamic voltage restorer
IEEE	Institute of Electrical and Electronics Engineers
IEC	International Electrotechnical Committee
IGBT	insulated gate bipolar transistor
IPFC	interline power flow controller
MKP	Metallisierter Kunststoff Polypropylen (metallized plastic polypropylene)
MMCC	modular multilevel cascaded converter
NPC	neutral-point-clamped
NTV	nearest three vectors
PC	personal computer
PI	proportional-integral (control)
PLL	phase-locked loop
PVCC	predictive vector current controller
PWM	pulse-width modulation
QSG	quadrature signal generator
RMS	root mean square
RTDS	real-time digital simulator
SCI	serial communication interface
SCR	short circuit ratio
SHE	selective harmonic elimination
SOGI	second-order generalised integrator
SRF	synchronous reference frame
SSSC	static synchronous series compensator
STATCOM	static synchronous compensator
STATCON	static condenser
SVC	static VAr compensator
SVL	space-vector limit (method)
SVM	space-vector modulation
SVS	static VAr system
TCR	thyristor-controlled reactor
TCSC	thyristor-controlled series capacitor
THD	total harmonic distortion
TPU	time processing unit

TSC	thyristor-switched capacitor
UPFC	unified power flow controller
UPQC	unified power quality controller
VSC	voltage source converter
ZOH	zero-order hold

Symbols

a, b, c	wire labels of three-phase three-wire system
A	state matrix
$A_{i31/i3}$	current division coefficient
B	input matrix
c	scalar coefficient
C	output matrix
C	capacitor, capacitance
C_1	upper DC bus capacitor
C_2	lower DC bus capacitor
C_3	LCL filter capacitor
C_{s1}	snubber capacitor (mounted on the IGBT module DC terminals)
C_{s2}	snubber capacitor (mounted in parallel with a DC bus capacitor)
d	duty cycle, direct axis (rotating coordinates)
d'	modified duty cycle
D	feedforward matrix
D	diode
D_{ik}	diode $i \in \{1, 2, 3, 4, 5, 6\}$ in phase-leg $k \in \{a, b, c\}$
e	error variable
e	error variable (vector)
E	coefficient matrix
f	frequency
f_c	corner frequency (of a filter)
g	horizontal axis of 60° coordinates
G	controller
h	skew axis of 60° coordinates
H	feedforward matrix
i	instantaneous current, index
i_k	current in phase $k \in \{a, b, c\}$

i_C	IGBT collector current
i_F	diode forward current
i_n	negative DC bus current
i_o	DC bus midpoint current
i_p	positive DC bus current
i_1	rectifier current
i_2	grid current
i_3	LCL filter shunt branch current
i_{31}	the portion of i_3 through L_3
i_{32}	the portion of i_3 through R_d
$\langle \vec{i}_{\text{rip,pu}} \rangle_1$	per unit average ripple current of the preceding switching period
$\langle \vec{i}_{\text{rip,pu}} \rangle_2$	per unit average ripple current of the succeeding switching period
$\langle \vec{i}_{\text{rip,pu}} \rangle_{12}$	per unit average ripple current over two adjacent switching periods
\mathbf{I}	identity matrix
I	current
j	imaginary unit
k	index, scalar coefficient
K	gain of SOGI-QSG
K_i	integral gain
K_{i1}	control coefficient of i_1
K_{i2}	control coefficient of i_2
K_{i3}	control coefficient of i_3
K_p	proportional gain
K_{sp}	Smith predictor gain
K_{uC3}	control coefficient of u_{C3}
$\mathbf{K}_{\text{u2-x}}$	coefficient matrix of $\mathbf{x}(k)$ in the matrix equation of $\mathbf{u}_2(k)$
$\mathbf{K}_{\text{i1-x}}$	coefficient matrix of $\mathbf{x}(k)$ in the matrix equation of $\mathbf{i}_1(k)$
$\mathbf{K}_{\text{i1-u}}$	coefficient matrix of $\mathbf{u}(k)$ in the matrix equation of $\mathbf{i}_1(k)$
$\mathbf{K}_{\text{i1-w}}$	coefficient matrix of $\mathbf{w}(k)$ in the matrix equation of $\mathbf{i}_1(k)$
$\mathbf{K}_{\text{u2-u}}$	coefficient matrix of $\mathbf{u}(k)$ in the matrix equation of $\mathbf{u}_2(k)$
$\mathbf{K}_{\text{u2-w}}$	coefficient matrix of $\mathbf{w}(k)$ in the matrix equation of $\mathbf{u}_2(k)$
\vec{l}	triangle edge (vector)
L	inductor, inductance
L_g	grid inductance
L_{ix}	inductance of the RL cell $x \in \{1, 2, 3\}$ of the Foster equivalent circuit of inductor L_i , where $i \in \{1, 2, 3\}$

L_{tot}	sum inductance $L_1 + L_2$
L_1	boost inductor
L_2	grid-side filter inductor
L_3	inductor of the filter shunt branch
\mathbf{L}	observer gain matrix, control coefficient matrix
m	modulation index
m_1, m_2, m_{12}	scalar projections
m_a	amplitude modulation ratio
\mathbf{M}	control coefficient matrix
n	negative DC bus
N	neutral point of a three-phase system
\mathbf{N}	control coefficient matrix
o	DC bus midpoint
p	positive DC bus
p	instantaneous power, pole
\vec{p}	vector projection
P	process
\hat{P}	process model
\hat{P}_0	delayless process model
q	quadrature axis (of rotating coordinates), -90° phase-shift operator
r	circle radius, reference signal
r_{CE}	equivalent resistance of an on-state IGBT
r_{F}	equivalent resistance of a forward-biased diode
r_{L_i}	resistance of the Foster equivalent circuit of inductor L_i , $i \in \{1, 2, 3\}$, when $f \rightarrow \infty$
r_{sb}	resistance of the shunt branch of the LCL filter equivalent circuit when $f \rightarrow \infty$
r_{tot}	resistance of the short-circuited LCL filter equivalent circuit when $f \rightarrow \infty$
\mathbf{r}	reference signal (vector)
R	resistor, resistance
R_{C}	damping resistor in series with C_3
R_{d}	damping resistor in parallel with L_3
R_{dis}	discharging resistor
R_{g}	grid resistance

R_{ix}	resistance $x \in \{0, 1, 2, 3\}$ of the Foster equivalent circuit of inductor L_i , where $i \in \{1, 2, 3\}$
R_1	equivalent series resistance of L_1
R_2	equivalent series resistance of L_2
R_3	equivalent series resistance of L_3
s_{ik}	logic-type switch state of the switch $i \in \{1, 2, 3, 4\}$ in phase-leg $k \in \{a, b, c\}$
sw_k	switching function of the phase-leg $k \in \{a, b, c\}$
$\vec{s}\vec{w}$	switching vector
\mathbf{S}	control coefficient matrix
S	apparent power
S_{ik}	power semiconductor switch $i \in \{1, 2, 3, 4\}$ of phase-leg $k \in \{a, b, c\}$
T	time interval
T_d	time delay
$T_{d(\text{off})}$	turn-off delay
$T_{d(\text{on})}$	turn-on delay
T_i	integration time
T_s	sampling time, switching period
$\mathbf{T}_{\alpha\beta 0}$	transformation matrix from three-phase to stationary orthogonal $\alpha\beta$ coordinates
\mathbf{T}_{dq0}	transformation matrix from three-phase to rotating orthogonal dq coordinates
u	instantaneous voltage, input variable
u_1	phase-to-neutral rectifier voltage
u_2	phase-to-neutral grid voltage
u_3	voltage across the LCL filter shunt branch
u_{C1}	voltage of capacitor C_1
u_{C2}	voltage of capacitor C_2
u_{C3}	voltage of capacitor C_3
$u_{\text{CE,on}}$	IGBT on-state collector-emitter voltage
u_{DC}	DC bus voltage
u_{F}	diode forward voltage
$u_{k\text{N}}$	phase-to-neutral voltage of phase $k \in \{a, b, c\}$
u_{Nn}	voltage between the neutral point and the negative DC bus
u_{sk}	supply phase $k \in \{a, b, c\}$ to neutral voltage
u_{ko}	rectifier phase $k \in \{a, b, c\}$ to DC bus midpoint voltage

\vec{u}_{xyz}	voltage vector generated by the switch combination xyz , where $x, y, z \in \{\text{n, o, p}\}$
U	voltage
U_{CE0}	IGBT collector-emitter threshold voltage
U_{F0}	diode forward threshold voltage
\hat{U}_1	amplitude of the fundamental frequency modulated voltage
$\hat{U}_{1,\text{six-step}}$	amplitude of the fundamental frequency voltage in the six-step operating mode
\hat{U}_{control}	amplitude of the modulated control voltage
$\hat{U}_{\text{triangle}}$	amplitude of the triangular carrier wave
\mathbf{w}	disturbance (vector)
\mathbf{x}	state variable (vector)
$\bar{\mathbf{x}}$	reduced-order observer output (vector)
X	reactance
y	output variable
\mathbf{y}	output variable (vector)
\mathbf{z}	unmeasured state variable (vector)
Z	impedance
α	real axis (stationary reference frame), thyristor gating angle
α_{Lmax}	maximum gating angle of the TCSC in the inductive mode
α_{Cmin}	minimum gating angle of the TCSC in the capacitive mode
β	imaginary axis (stationary reference frame)
γ_{n}	length of negative short vector
γ_{p}	length of positive short vector
$\mathbf{\Gamma}$	input matrix (discrete-time system)
Δu_{C}	capacitor voltage imbalance
θ	angle
θ_{g}^+	angle of positive-sequence grid voltage
ρ	integration variable
τ	time constant
Φ	state matrix (discrete-time system)
ω_{g}	grid angular frequency
ω_{r}	angular frequency of rotating orthogonal reference frame
ω_0	center frequency (rad/s) of SOGI-QSC

Subscripts

0	refers to zero-sequence component
actual	refers to actual value
c	refers to clamp diode
comp	refers to compensation
d	refers to direct axis (rotating coordinates)
dt	refers to dead-time
e	refers to error
fwd	refers to free-wheeling diode
g	refers to g axis, refers to electrical grid
h	refers to h axis
ideal	refers to ideal value
init	refers to initial value
n	refers to negative DC bus, refers to nominal value
o	refers to observer, refers to DC bus midpoint
off	refers to off-time
on	refers to on-time
p	refers to positive DC bus
pu	per unit value
PI	refers to PI controller
q	refers to quadrature axis (rotating coordinates)
r	refers to rotating orthogonal reference frame, refers to reference signal
rip	refers to ripple waveform
s	refers to stationary orthogonal reference frame
sp	refers to Smith predictor
S1/S4	refers to power semiconductor switches S_1 and S_4
S2/S3	refers to power semiconductor switches S_2 and S_3
u	refers to input variable
w	refers to disturbance
x	refers to state variable
y	refers to output variable
z	refers to unmeasured state variable
zc	refers to zero crossing

Superscripts

$*$	reference signal, complex conjugate
$+$	positive-sequence quantity
$\alpha\beta$	refers to stationary reference frame
dq	refers to synchronous reference frame
u	refers to input variable
w	refers to disturbance

Notations

$\langle x \rangle$	average value of x
\hat{X}	amplitude of sinusoidal signal
\hat{x}	estimate of x
\tilde{x}	filtered signal x
\vec{x}	complex vector
x'	scaled x
Δx	error of x
$\text{sign}(x)$	sign of x
$\neg x$	negation of x

Chapter 1

Introduction

Uninterrupted and reliable generation, transmission, and distribution of electrical energy is essential for modern societies. Many everyday functions such as clean water, heating, waste-water disposal, public transportation, and communication systems could not be provided or kept operating without continuous electricity supply. The supplied electricity is also expected to fulfil other quality characteristics that enable normal operation of the customer equipment in their electrical environment. Continuous industrial processes, such as paper mills and oil refineries, demand an exact and reliable electricity supply. In such plants supply interruptions and power problems leading to device failures and malfunctions are critical, because downtime and lost production bring severe economic losses.

According to [1], concerns and awareness about the quality of electrical energy have been growing since 1980's among electric utilities and end users. A major reason behind this trend has been the increasing sensitivity of modern load equipment to electromagnetic disturbances in the networks [2]. On the other hand, modern loads are very often nonlinear and, more often than not, they are sources of disturbances themselves. For example, the proliferation of high-power rectifiers and inverters has increased the harmonic levels in the networks and complicated the resonance problems [3, 4, 5]. Also the development of standards and compatibility levels, as well as the improvements in the field of network monitoring technology, data collection and statistical analyses, have increased the awareness of power quality issues [6].

From the non-technical point of view, the interest towards power quality has been promoted by customer-utility relations emphasizing performance, reliability and quality. The manufacturing industry's push towards more efficient and productive processes has challenged the utilities to improve their services to fulfil the customers' expectations. Electrical energy has evolved into a commodity whose quality is measurable and with a direct impact on the customer's productivity [7]. As a result, delivering high quality electricity has become a competitive tool for utilities in the energy markets [8].

1.1 Power quality

The majority of electrical energy is transmitted and distributed to the end users via a three-phase AC network of cables. The AC power systems are designed to operate with a standard frequency, typically 50 or 60 hertz, and at different voltage levels [9]. Ideally, the voltage waveform is purely sinusoidal in every network location, the voltages are of nominal amplitude and frequency, and the displacement between the phase voltages is one third of the fundamental period. The currents, too, should have sinusoidal waveforms. The power transfer is maximised when the phase voltages and currents are in phase [1]. In practice, under normal network conditions, the voltage varies around the rated value and the current waveforms and their displacement with respect to the voltages are determined by the load characteristics.

The deviations of voltage and current from normal conditions fall within the realm of power quality. It deals with the interactions of the power system and the loads but an exact definition lacks general consensus [1, 2]. In [2], a power quality issue is described as *any power problem manifested in voltage or current, or frequency deviations that result in failure or malfunction of customer equipment*. In [1], power quality is considered to be a combination of the voltage quality and the current quality. Some other authors refer to it as a voltage quality problem [2, 10]. The broadest interpretation is to consider power quality equivalent to service quality which includes the supply reliability, the quality of power offered, and the information sharing about the reliability performance [8].

The power quality phenomena may be grouped to variations and events [1]. The variations are small deviations of amplitude, phase and frequency from the ideal, such as harmonic distortion, unbalance, fluctuations, and voltage notching. The events are occasional sudden voltage and current changes, such as interruptions, under/overvoltages, and heavily distorted overcurrents, which compromise the load and network equipment leading to malfunctions and failures. The events normally arise from network faults caused by environmental factors such as adverse weather and overgrown vegetation. Also, the operation of large loads, sudden load changes, interactions between the power system components and loads, and equipment failures, can trigger such events.

Normal operation of the customer equipment goes hand in hand with maintaining the power quality phenomena within prescribed limits and tolerances. Compatibility levels, as well as recommendations and guidelines for monitoring and improving the power quality, have been set by various national and international organizations. For example, the steady-state limits for current harmonics have been specified in IEEE Std. 519 [5] and the steady-state voltage quality characteristics in IEC 61000-2-2¹ [11] and EN 50160 [12]. Guidelines for power quality monitoring have been given in IEEE Std. 1159 [13] and for improving the power system voltage quality in IEEE Std. 1250 [14].

¹In the standard documents of IEC the term *electromagnetic compatibility* is used instead of *power quality*, but the two terms share similar characteristics.

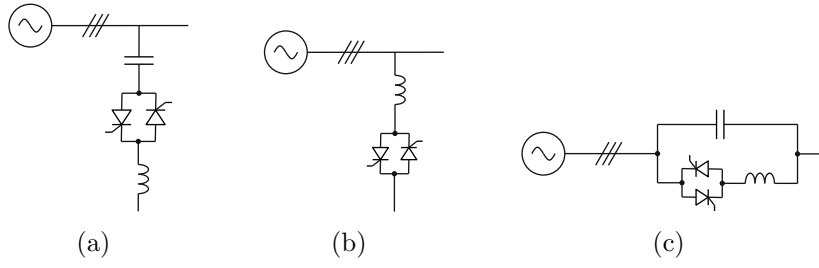


Fig. 1.1: The basic variable-impedance-type static compensators. (a) Thyristor-switched capacitor (TSC) including a current-limiting inductor, (b) Thyristor-controlled reactor (TCR), (c) Thyristor-controlled series capacitor (TCSC).

The improvement and maintenance of power quality may include various actions. For example, tree trimming programs, installation of additional protective equipment, and increased network automation and redundant equipment enhance the power quality [10]. Investing in monitoring equipment serves as a preventive action and assists in determining the correct solution to the power quality problem. The power quality conditioners are equipment that tend to mitigate the power quality phenomena by contributing to one or more of the network impedance, voltage, current, and transmission angle [15, 16]. The state-of-the-art power quality conditioners are based on power electronic AC-DC converters which yield fast response time and broad control range nearly independent of the network voltage [17]. This thesis focuses on the issues in digital control of a static reactive power compensator using a three-level voltage-source rectifier.

1.2 Passive and variable-impedance power quality conditioners

In the early days, the network voltage 'control' and power factor correction were mainly based on the use of shunt capacitors and reactors [18]. Precise and continuously adjustable reactive power control was achieved with synchronous condensers (machines) through the control of excitation field current [19, 20]. Single voltage harmonics were suppressed with tuned LC filters [3, 21]. Capacitors were installed in series with the power lines to increase the transmission capacity and also to suppress flicker problems caused by large industrial loads such as welding machines and arc furnaces [22, 23].

The synchronous condenser was the only fully controllable reactive power compensator until the mid-1970s. Then the development of high power thyristors created the basis for new variable-impedance-type static compensators which provided improved dynamic control over the network voltage, transmission angle, and impedance [20]. The new compensators were based on bi-directional back-to-back thyristor switches and reactive circuit components, as illustrated in Fig. 1.1.

The thyristor-switched capacitor (TSC), depicted in Fig. 1.1(a), comprises one

or more shunt-capacitor banks in parallel. The reactive power generated is adjustable in discrete steps by controlling the thyristor switches [20]. The thyristor-controlled reactor (TCR) consists of a shunt reactor in series with a thyristor switch, as depicted in Fig. 1.1(b). The gating delays of the thyristors are controlled between $\alpha = 90^\circ \dots 180^\circ$ with respect to the network voltage to control the current through the reactor. The TCR generates non-sinusoidal currents when $\alpha > 90^\circ$. The triplen harmonics do not enter the network if the TCR is connected in delta, and the current distortion is further reduced with twelve-pulse circuit arrangement or segmented control of parallel TCRs [15]. Large compensation systems, known as static VAr systems (SVS) or static VAr compensators (SVC), combine TCRs and TSCs with shunt-capacitor banks and shunt-reactors [24]. They are used in flicker compensation, oscillation damping, system voltage balancing, and voltage control [25, 26, 27, 28].

The thyristor-controlled series capacitor (TCSC), depicted in Fig. 1.1(c), comprises a TCR in parallel with a capacitor. The TCSC functions as a variable series reactance when the gating delay of the TCR is controlled between $\alpha = 90^\circ \dots 180^\circ$ with respect to the capacitor voltage² [15]. In the capacitive operating mode, with $\alpha_{\text{Cmin}} \leq \alpha < 180^\circ$, the voltage across the TCSC can be increased over that produced by the fixed capacitor and the given network current. In the inductive operating mode, with $90^\circ < \alpha \leq \alpha_{\text{Lmax}}$, the voltage across the capacitor is decreased. The TCSC functions as a fixed capacitor with $\alpha = 180^\circ$ and as a fixed reactor with $\alpha = 90^\circ$. Delay angles $\alpha_{\text{Lmax}} < \alpha < \alpha_{\text{Cmin}}$ are forbidden because of the LC parallel resonant frequency. The TCSC can be used to compensate the transmission line inductance, control the power sharing between parallel lines, and dampen the power oscillations. Furthermore, it can overcome the sub-synchronous resonance problem associated with fixed series capacitors [15].

1.3 Power quality conditioners based on AC-DC converters

During the mid-1980s, the high-power gate turn-off (GTO) thyristors became commercially available and accelerated the development of high-power converters [29, 30, 31, 32]. Concurrently, the Electrical Power Research Institute (EPRI) presented the concept of Flexible AC Transmission Systems (FACTS) technology which envisioned that in future the power-electronic-based and other static controllers would be used widely to improve on the network controllability and to increase the power transfer capacity [33]. The FACTS concept included a new group of shunt, series, and shunt-series controllers based on self-commutated power converters, providing the following major advantages: (i) significant size reduction of passive reactive components needed [34], (ii) the rated output current could be generated at nearly zero network voltage [32], (iii) the active and reactive power flows could be controlled in

²When the control is synchronised with the line current, the gating delay is controlled between $0^\circ \dots 90^\circ$ with respect to the current.

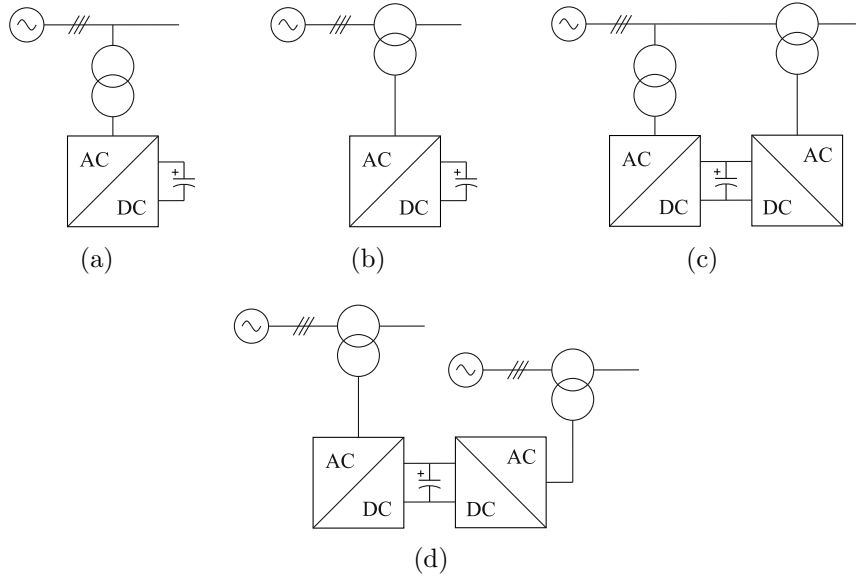


Fig. 1.2: The principal concepts of converter-based power FACTS controllers. (a) Static synchronous compensator (STATCOM), (b) Static synchronous series compensator (SSSC), (c) Unified power flow controller (UPFC), (d) Interline power flow controller (IPFC).

an almost instantaneous basis [34].

Fig. 1.2 exemplifies the main concepts of the converter-based FACTS controllers [15]. The static synchronous compensator (STATCOM) in Fig. 1.2(a), also known as static condenser (STATCON), is a shunt-connected reactive power controller. The static synchronous series compensator (SSSC) in Fig. 1.2(b) is connected in series with the power lines using a transformer. It provides fully controllable series compensation which is nearly independent of the line current. Both the STATCOM and the SSSC can control also the active power if an external DC power source is connected to the DC bus.

The unified power flow controller (UPFC) depicted in Fig. 1.2(c) combines the features of the STATCOM and the SSSC. The series converter injects fully controllable voltage in series with the network while the shunt converter supplies the required active power to the common DC bus [35]. The shunt converter can also control reactive power. The interline power flow controller (IPFC), illustrated in Fig. 1.2(d), comprises two or more SSSCs connected to different power lines at a substation. They can control the reactive power and transfer active power between the lines via the common DC bus [36].

The FACTS concept primarily deals with the transmission system. Another EPRI concept, the Custom power, was introduced in the early 90's and is concerned with maintaining and improving the quality and reliability of distribution systems to fulfil the requirements of industrial and commercial sensitive loads [37, 38]. The concept's overriding objective is to provide energy-efficient and lowest cost power quality solutions by means of solid-state power electronic controllers [17]. The network reconfiguring-type controllers include current limiting, current breaking and

current transferring devices [39]. The compensating type controllers include the distribution-level STATCOM (D-STATCOM or D-STATCON) [40], series connected dynamic voltage restorer (DVR) [41], shunt-series connected unified power quality conditioner (UPQC) [42], and series-series connected interline dynamic voltage restorer (IDVR) [43]. Their principles are similar to the ones depicted in Fig. 1.2 but the power rating is lower and higher switching frequencies are used. As a result, other control functions, such as active harmonic filtering, become available [44].

1.4 An overview on STATCOMs

1.4.1 System configurations and topologies

The STATCOM has found various applications in both the transmission system [45, 46, 47, 48, 49, 50] and the distribution system [51, 52, 53, 54]. A STATCOM may comprise a single converter or a parallel connection of several units [45]. Typically voltage source converter (VSC) topologies are preferred, because the current source converters (CSCs) provide lower efficiency and require reverse-voltage-blocking power semiconductor switches [51]. The classic three-phase six-switch VSC is the simplest one but the voltage ratings of commercially available power semiconductor modules limit its feasibility in medium and high voltage applications. The converter's voltage rating can be increased by connecting several power semiconductor modules in series. However, a complex gate driver and additional protection circuitry is needed to balance the dynamic and the off-state voltage sharing within the series connection [55].

The state-of-the-art STATCOM technology is based on converter topologies that generate multi-step AC voltage waveforms. They can be categorized in multipulse [56], multimodule pulse-width modulated (PWM) [57] and multilevel [58, 59, 60] topologies. The multipulse and multimodule PWM converters consist of parallel-connected converters sharing a common DC bus. The multipulse converters include a complex phase-shifting transformer which combines the outputs of fundamental-frequency-modulated parallel converters. The transformer is designed so that the dominant harmonics are cancelled. The remaining ones are filtered using passive filters to achieve nearly sinusoidal currents with a very low switching frequency. Therefore, the multipulse converters are favoured in very-high-power applications [61, 32, 47, 50, 62, 63]. However, they provide slow dynamic behaviour because the output voltage amplitude is adjusted through the DC bus voltage control [56, 64]. The multimodule PWM converters use a multi-secondary transformer instead of a phase-shifting transformer. The output voltage harmonics are minimised by keeping the fundamental frequency voltage components of the parallel converters in phase, but sequentially and equally phase-shifting the carrier-waves [64]. In the case of space-vector modulation, the converters receive the same voltage reference but the modulator sampling instants are interleaved [57]. The output voltage is controlled through the modulation index which yields faster dynamic behaviour compared to the multipulse converters but at the cost of increased switching losses [64].

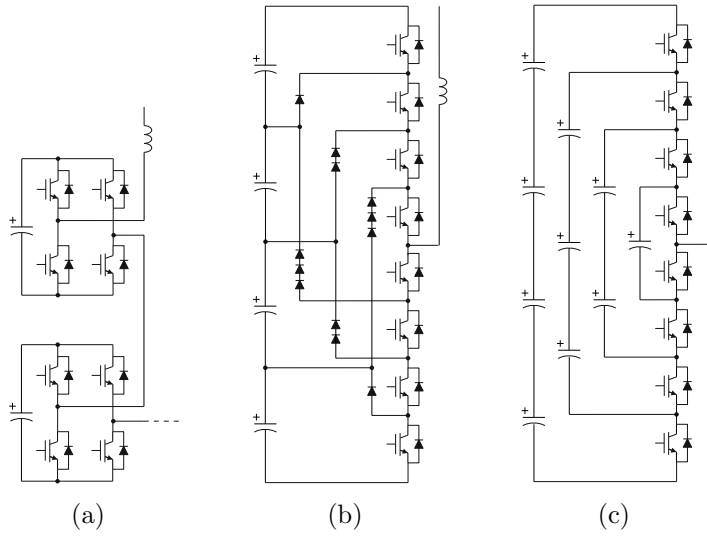


Fig. 1.3: One switch-arm of the three classic multilevel converter topologies. (a) Five-level MMCC consisting of full-bridge modules, (b) Five-level diode-clamped converter, (c) Five-level capacitor-clamped converter.

The multilevel converters generate line-to-line AC voltage waveforms with five or more voltage steps by using an array of power semiconductor switches and a number of voltage sources, typically capacitors. The three classic multilevel topologies illustrated in Fig. 1.3 are the modular multilevel cascaded converter (MMCC) consisting of full-bridge modules [65, 66], the diode-clamped (multi-point-clamped) converter [67], and the capacitor-clamped (flying-capacitor) converter [68]. Also a number of their variants and hybrid topologies have been researched [59, 69]. Currently, the two principal multilevel topologies in industrial STATCOMs are the MMCC [45, 46, 48] and the three-level diode-clamped converter which is also known as the neutral-point-clamped (NPC) converter [49, 52, 53, 70]. The advantage of the MMCC topologies is their modular structure, which allows building converters with numerous output voltage levels and of different circuit configurations [66]. They have a great deal of potential in applications requiring high output voltage and low switching frequency. The diode-clamped topology fits well in back-to-back converter applications such as shunt-series and series-series compensators. However, in general no more than three DC bus levels are favoured because of the unyielding complexity of the main circuit, higher losses and uneven loss distribution between the power semiconductor components, and the difficulties associated with the capacitor voltage balancing [59].

1.4.2 Control architecture

The main functions of the STATCOM's control architecture can be categorised in the five layers illustrated in Fig. 1.4 [71]. The highest layer is the system control which determines the operating mode such as reactive power control, power factor control, voltage control, flicker mitigation, or harmonic compensation. The system

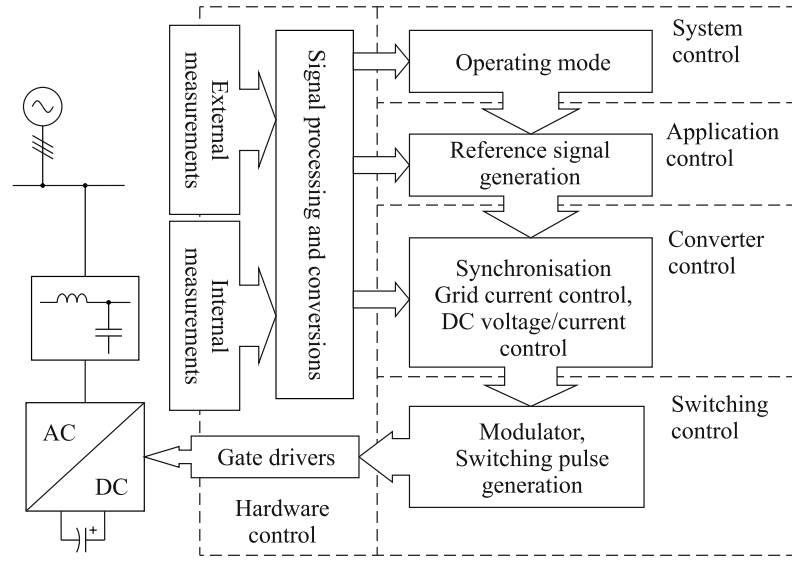


Fig. 1.4: STATCOM control architecture.

control can configure the STATCOM to operate in one or more operating modes at a time, and to change the operating mode upon request or variations in the network condition.

The application control includes the functions needed to complete the objectives of the system control. An important task concerns the generation of the reference signals for the converter control by using the sensed network voltages and currents. Also sensorless approaches have been proposed to minimise the measurement hardware requirements [72].

In the voltage control mode, the error between the given set point and the RMS network voltage is compensated by using, let say, a PI controller with a droop characteristic [73, 74]. To compensate the voltage imbalance, the positive and negative sequence voltages must be extracted from the sensed voltages [75]. For voltage harmonics filtering, the fundamental frequency voltage is separated from the harmonics [76, 77].

The references for harmonic current filtering, reactive power compensation, and load balancing can be generated by decomposing the sensed currents into components. Widely-used decomposition methods include discrete Fourier transformation [78, 79, 80, 81] and digital filtering in the grid-voltage-oriented vector reference frame and in the harmonic reference frames [82, 83, 84]. Alternative decomposition methods are based on the instantaneous power theories [85, 86, 87, 88, 89, 90, 91]. Also, methods based on artificial neural networks [82] and neuro-fuzzy algorithms [92] have been proposed in the scientific literature.

The converter control reacts on the references received from the control application based on the external measurements taken from the network and the internal measurements taken from the converter. Essential functions include the grid synchronisation, the DC bus voltage (or current) control, and the grid current control [93]. Various grid current control strategies have been put forward, including, for

example, proportional-resonant controllers [94], synchronous reference frame PI controls [95], state feedback control [96, 97, 98], and predictive control [99]. Nonlinear control strategies are studied in [100, 74]. For example, in [95, 101, 102, 103] the grid current is controlled in the synchronous reference frame using two PI controllers. The strategy is simple but poor stability margins can be a problem when it is applied to grid-parallel converters with an *LCL* filter [102, 103]. In theory, a very fast dynamic behaviour, so-called deadbeat response, is achievable with predictive controllers [104, 105, 99, 106]. However, the full state vector should be measured or estimated, which increases the complexity of either the hardware or the software. Furthermore, the control computation delay and parametric uncertainties may require lowering the controller gains, and loosening the response time, to achieve proper stability margins [99]. In addition, the generic current control strategies may provide insufficient performance in unbalanced and distorted grids. In such cases, control extensions are needed to achieve desired current waveform quality [107, 104, 108].

The core of the switching control layer is the pulse-width modulator that generates the control signals for the power semiconductor switches. Fig. 1.5 classifies the principal modulation strategies of the multilevel converters in low and high switching frequency methods [59, 109]. From the low frequency methods, the space vector control is attractive if the converter can generate a high number of output voltage steps [110]. Then high quality voltage waveform and low switching frequency are achieved by using only one output voltage combination during a sample period. In the selective harmonic elimination PWM (SHEPWM), the switching angles are computed offline and optimised to eliminate the harmonics of interest from the output voltage spectrum [111, 112].

From the high-frequency methods, the multi-carrier PWM can be divided in phase-shifted [113] and level-shifted methods [114], depending on the arrangement of the carrier waves [115]. The space-vector modulation (SVM) is favoured in several publications because it offers degrees of freedom to optimise the switching patterns [116, 117, 118, 119, 120, 121] and to balance the DC bus capacitor voltages [122, 123, 124].

On the lowest layer in Fig. 1.4 is the control hardware. It includes the gate drive units and the power supplies needed to control the power semiconductor switches, but also the current and voltage sensors, measurement circuits, and the analogue-to-digital conversions [71].

1.5 Scope and objectives

This thesis addresses the digital control of a static reactive power compensator based on the three-level neutral-point-clamped boost rectifier. The focus is on the pulse-width-modulation and the grid-current-control strategies because they determine the dynamic behaviour and the performance of the application.

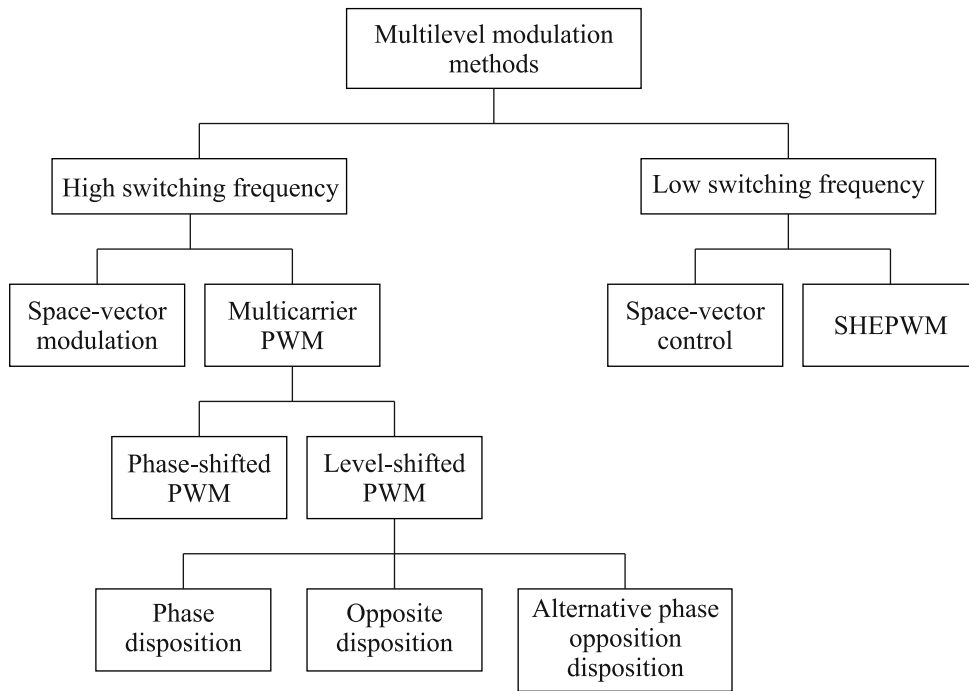


Fig. 1.5: Classification of multilevel modulation methods.

The first objective is to implement a space-vector modulation algorithm which uses discontinuous switching patterns to decrease the switching frequency. The non-linear voltage errors caused by capacitor voltage imbalances, blanking times, and voltage drops across the power semiconductors are to be studied and compensated. The arrangement of switching sequences during the transitions between the different regions of the voltage vector plane should be analysed to decide on how the transitions should be carried out. The modulation algorithm should control the capacitor voltage balance.

The second objective is to study the dynamic behaviour and the characteristics of two grid current control strategies implemented in the grid-voltage-oriented vector coordinates. The first one is the decoupled PI current control strategy. The second one is a predictive vector current control strategy which requires the feedback from the full state vector. Increasing the number of sensor-hardware is not desired. Therefore, the non-measured states should be estimated. An algorithm compensating the control computation delay should be included in the grid current control loop.

The third objective is to verify the theoretical considerations using simulations and laboratory experiments.

1.6 Scientific contributions

The main contributions of the thesis can be summarised as follows:

- The problems related to the application of discontinuous switching patterns on the three-level converter are revealed. A method resulting in correct switching pattern arrangement is proposed and verified.
- The methods to compensate the PWM voltage errors caused by the blanking times of the switch control signals and the on-state semiconductor voltage losses are proposed and verified.
- It is shown by means of dynamic modelling and simulations that the grid current controllers under study are incapable to reject background grid voltage distortion. Furthermore, the effects of modelling errors on the dynamic behaviour of the observer-based grid current controllers are revealed. The theoretical considerations are verified with experiments.

1.7 List of published papers

The following publications emanated during the course of this research. They were written and presented, and all the simulations and experiments were carried out, by the first author.

P. Lauttamus and H. Tuusa, *Comparison of five-level voltage-source inverter based STATCOMs*, Proc. 4th Power Conversion Conf. (PCC'07), pp. 659-666, 2-5 April 2007.

P. Lauttamus and H. Tuusa, *Unified space-vector modulation scheme for multilevel inverters*, Proc. 4th Power Conversion Conf. 2007 (PCC'07), pp. 1464-1471, 2-5 April 2007.

P. Lauttamus and H. Tuusa, *Three-level VSI based low switching frequency 10 MVA STATCOM in reactive power and harmonics compensation*, The 7th Int. Conf. Power Electron. (ICPE'07), pp. 536-541, 22-26 Oct. 2007.

P. Lauttamus and H. Tuusa, *Simulated electric arc furnace voltage flicker mitigation with 3-level current-controlled STATCOM*, The 23rd Annu. IEEE Applied Power Electron. Conf. and Expo. (APEC'08), pp. 1697-1703, 24-28 Feb. 2008.

P. Lauttamus and H. Tuusa, *Design of discontinuous switching sequences in the case of grid-connected three-level voltage-source converter*, Int. Power Electron. Conf. (IPEC'10), pp. 760-767, 21-24 June 2010.

P. Lauttamus and H. Tuusa, *Model-based cascade control of three-level STATCOM with a tuned LCL-filter*, The 26th Annu. IEEE Applied Power Electron. Conf. and Expo. (APEC'11), pp. 1569-1575, 6-11 March 2011.

1.8 Structure of the thesis

The rest of the thesis is organised as follows. Chapter 2 provides the theoretical backgrounds of the three-wire three-level NPC topology, multilevel space-vector modulation, and converter control.

Chapter 3 focuses on the dynamic modelling of the STATCOM under study. Average models are presented for the purposes of grid current controller design and analysis.

Chapter 4 presents the implemented discontinuous space vector modulation strategy. Firstly, the duty cycles solution and capacitor voltage balancing algorithm are presented. Then the switching waveforms during the transitions between different regions of the space-vector plane are analysed. Finally, a compensation method for the voltage errors caused by the blanking times and the voltage drops across the on-state power semiconductor is presented.

Chapter 5 focuses on the design and analysis of the grid current control loop. The characteristics of two current control strategies implemented in the grid-voltage-oriented vector coordinates are studied. A prediction of the rectifier output current is included in the control action to reduce the effects of control computation delay. The effect of grid impedance on the current controllers' stability is analysed.

Chapter 6 presents the laboratory prototype and the experimental results. The operation of the switching control strategy is demonstrated and the dynamics of the current controllers are evaluated by means of step-response tests.

Chapter 7 concludes the thesis and proposes future research topics.

Chapter 2

Theoretical backgrounds

2.1 Introduction

This chapter presents the theoretical background of the thesis. Section 2.2 gives an overview on the three-wire three-level neutral-point-clamped boost rectifier and on the forming of the output voltages. Also, the problems affiliated with blanking times, voltage loss across the on-state semiconductors, and DC bus capacitor voltage balancing are presented. In Section 2.3, the fundamentals of multilevel space-vector modulation are introduced. Section 2.4 provides an overview on a cascaded vector control scheme implemented in the grid-voltage-oriented reference frame. Section 2.5 draws the conclusions.

2.2 Three-wire three-level neutral-point-clamped rectifier

2.2.1 Switching states and output voltages

Fig. 2.1 depicts the schematic of the three-wire three-level neutral-point-clamped (NPC) rectifier. The topology was proposed by Nabae et. al in 1981 [67]. The phase-to-neutral supply voltages at the connection point of the rectifier are denoted as u_{sa} , u_{sb} , and u_{sc} . The boost inductors are presented with series RL elements. The DC bus comprises two series-connected capacitors C_1 and C_2 . The positive and the negative DC bus nodes are referred to as 'p' and 'n', respectively, and the midpoint is 'o'. Each rectifier phase-leg comprises four power semiconductor switches S_1 - S_4 with free-wheeling diodes (FWD) D_1 - D_4 . In addition, the clamp diodes D_5 and D_6 enable the current path to the DC bus midpoint 'o' and limit the voltage stresses of the switches to the voltage across one DC capacitor.

Conservatively, the switches are controlled based on the principle $S_{1k} \vee S_{3k}$ and

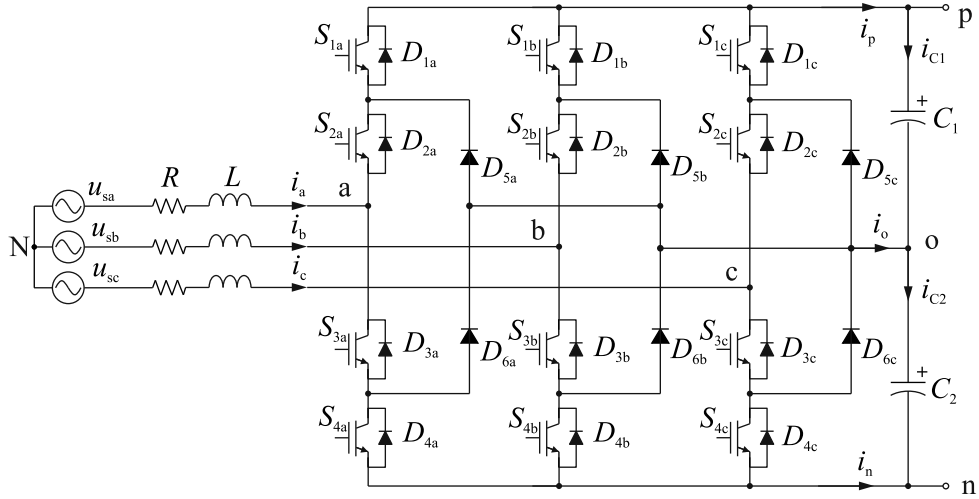


Fig. 2.1: The schematic of three-wire three-level neutral-point-clamped rectifier.

$S_{2k} \vee S_{4k}$ with $k \in \{a, b, c\}$. As a result, always two consecutive switches in each phase-leg are in the on-state. The switch states can be described with logic-type functions s_{1k} , s_{2k} , $s_{3k} = \neg s_{1k}$, and $s_{4k} = \neg s_{2k}$, which are defined 1 when true and 0 otherwise. The three possible switch combinations and the resulting voltages u_{kn} are summarised in Table 2.1.

Table 2.1: Switch states and phase voltages with respect to the negative DC bus rail

Voltage u_{kn}	s_{1k}	s_{2k}	s_{3k}	s_{4k}
$u_{C1} + u_{C2}$	1	1	0	0
u_{C2}	0	1	1	0
0	0	0	1	1

When the constraints imposed on the switch control are satisfied, the phase voltages with respect to 'n' can be expressed as

$$u_{kn} = s_{1k}s_{2k}(u_{C1} + u_{C2}) + s_{2k}(1 - s_{1k})u_{C2} \quad (2.1a)$$

$$= s_{2k}(1 + s_{1k})\frac{u_{DC}}{2} - s_{2k}(1 - s_{1k})\frac{\Delta u_C}{2} \quad (2.1b)$$

where the latter form describes u_{kn} in terms of the full DC bus voltage and the capacitor voltage imbalance $\Delta u_C = u_{C1} - u_{C2}$. In addition, the DC bus currents i_p , i_o , and i_n and the capacitor currents of an unloaded DC bus can be written as follows

$$i_p = s_{1a}s_{2a}i_a + s_{1b}s_{2b}i_b + s_{1c}s_{2c}i_c \quad (2.2)$$

$$i_o = s_{2a}(1 - s_{1a})i_a + s_{2b}(1 - s_{1b})i_b + s_{2c}(1 - s_{1c})i_c \quad (2.3)$$

$$i_n = (1 - s_{1a})(1 - s_{2a})i_a + (1 - s_{1b})(1 - s_{2b})i_b + (1 - s_{1c})(1 - s_{2c})i_c \quad (2.4)$$

$$i_{C1} = i_p \quad (2.5)$$

$$i_{C2} = i_p + i_o = -i_n \quad (2.6)$$

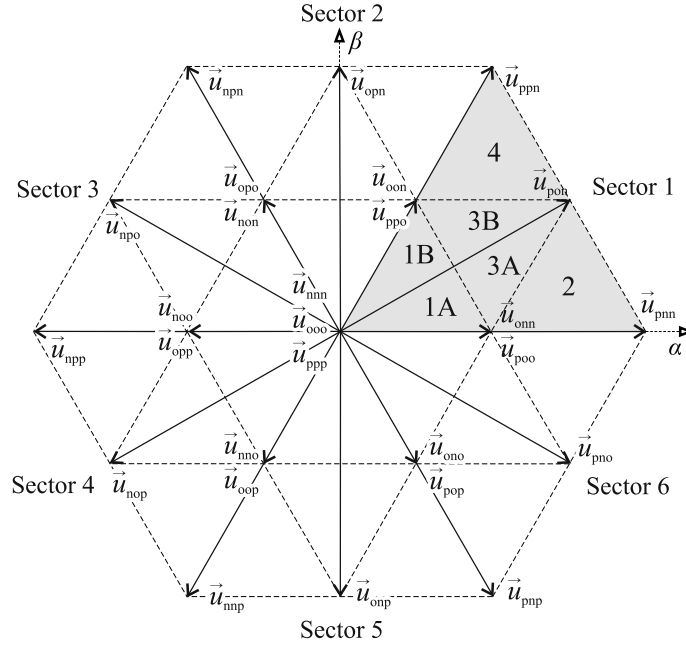


Fig. 2.2: Voltage vectors of the three-level NPC rectifier.

The switch combinations in Table 2.1 give altogether 27 different three-phase voltage combinations that can be expressed as complex vectors in the $\alpha\beta$ plane by using the Clarke transformation reviewed in Appendix A. Let us assume $u_{C1} = u_{C2}$. As a result, the last term of (2.1b) is eliminated and the output voltage vectors can be expressed as

$$\vec{u} = \frac{2}{3}(u_{an}e^{j0} + u_{bn}e^{j\frac{2\pi}{3}} + u_{cn}e^{j\frac{4\pi}{3}}) \quad (2.7a)$$

$$= \frac{2}{3}(sw_a e^{j0} + sw_b e^{j\frac{2\pi}{3}} + sw_c e^{j\frac{4\pi}{3}}) \frac{u_{DC}}{2} \quad (2.7b)$$

$$= \vec{sw} \frac{u_{DC}}{2} \quad (2.7c)$$

where sw_k is a switching function and \vec{sw} is a switching vector. The switching functions are defined as $sw_k = s_{2k}(1 + s_{1k})$ which yields $sw_k \in \{0, 1, 2\}$. The 27 voltage vectors are illustrated in Fig. 2.2 where the vector subscripts define the associated switch combination: $p \triangleq s_{1k} \wedge s_{2k}$, $o \triangleq s_{2k} \wedge s_{3k}$, and $n \triangleq s_{3k} \wedge s_{4k}$.

Table 2.2 classifies the voltage vectors in four groups based on their magnitudes: in zero, short, medium and long vectors. The long vectors are of length $\frac{2}{3}u_{DC}$. They divide the voltage hexagon, depicted in Fig. 2.2, in six 60° main sectors denoted as Sector 1 to Sector 6. The main sectors are split into smaller subsectors, numbered with 1 to 4, by the medium vectors of length $\frac{1}{\sqrt{3}}u_{DC}$ and the short vectors of length $\frac{1}{3}u_{DC}$. In addition, the medium vectors divide the subsectors 1 and 3 into regions 1A, 1B, 3A, and 3B. The overlapping redundant short vectors generate different

zero-sequence voltages but the same line-to-line voltages when $u_{C1} = u_{C2}$. During the zero vectors \vec{u}_{nnn} , \vec{u}_{ooo} , and \vec{u}_{ppp} all the phases are connected to the same DC bus potential.

Table 2.2 also presents the DC bus currents associated to each voltage vector, as well as the capacitor currents, when an unloaded rectifier is considered. The long vectors do not generate midpoint current i_o and, therefore, do not contribute to the DC bus capacitor voltage balance unless $C_1 \neq C_2$. The medium vectors connect one phase to each of the DC bus nodes. As a result, one capacitor is charged or discharged with respect to the other, depending on the polarity of i_o . The redundant short vectors can be categorised in positive and negative vectors. The positive short vectors circulate the DC bus current through the upper capacitor C_1 , yielding $i_{C1} = i_p = -i_o$, and charge (discharge) it with respect to C_2 . The negative short vectors affect only the charge of C_2 ($i_{C2} = -i_n = i_o$). The zero vectors do not contribute to the capacitor voltages, because they yield $i_p = i_o = i_n = 0$.

Table 2.2: Voltage vectors of the three-level neutral-point-clamped rectifier and the resulting DC bus currents. The tabulated capacitor currents assume an unloaded DC bus.

Vector	$\ \vec{u}\ $	i_p	i_o	i_n	i_{C1}	i_{C2}
Zero vectors						
\vec{u}_{nnn}	0	0	0	0	0	0
\vec{u}_{ooo}	0	0	0	0	0	0
\vec{u}_{ppp}	0	0	0	0	0	0
Positive short vectors						
\vec{u}_{poo}	$\frac{1}{3}u_{DC}$	i_a	$-i_a$	0	i_a	0
\vec{u}_{ppo}	$\frac{1}{3}u_{DC}$	$-i_c$	i_c	0	$-i_c$	0
\vec{u}_{opo}	$\frac{1}{3}u_{DC}$	i_b	$-i_b$	0	i_b	0
\vec{u}_{opp}	$\frac{1}{3}u_{DC}$	$-i_a$	i_a	0	$-i_a$	0
\vec{u}_{oop}	$\frac{1}{3}u_{DC}$	i_c	$-i_c$	0	i_c	0
\vec{u}_{pop}	$\frac{1}{3}u_{DC}$	$-i_b$	i_b	0	$-i_b$	0
Negative short vectors						
\vec{u}_{onn}	$\frac{1}{3}u_{DC}$	0	i_a	$-i_a$	0	i_a
\vec{u}_{oon}	$\frac{1}{3}u_{DC}$	0	$-i_c$	i_c	0	$-i_c$
\vec{u}_{non}	$\frac{1}{3}u_{DC}$	0	i_b	$-i_b$	0	i_b
\vec{u}_{noo}	$\frac{1}{3}u_{DC}$	0	$-i_a$	i_a	0	$-i_a$
\vec{u}_{nno}	$\frac{1}{3}u_{DC}$	0	i_c	$-i_c$	0	i_c
\vec{u}_{ono}	$\frac{1}{3}u_{DC}$	0	$-i_b$	i_b	0	$-i_b$
Medium vectors						
\vec{u}_{pon}	$\frac{1}{\sqrt{3}}u_{DC}$	i_a	i_b	i_c	i_a	$-i_c$
\vec{u}_{opn}	$\frac{1}{\sqrt{3}}u_{DC}$	i_b	i_a	i_c	i_b	$-i_c$
\vec{u}_{npo}	$\frac{1}{\sqrt{3}}u_{DC}$	i_b	i_c	i_a	i_b	$-i_a$
\vec{u}_{nop}	$\frac{1}{\sqrt{3}}u_{DC}$	i_c	i_b	i_a	i_c	$-i_a$
\vec{u}_{onp}	$\frac{1}{\sqrt{3}}u_{DC}$	i_c	i_a	i_b	i_c	$-i_b$
\vec{u}_{pno}	$\frac{1}{\sqrt{3}}u_{DC}$	i_a	i_c	i_b	i_a	$-i_c$
Long vectors						
\vec{u}_{pnn}	$\frac{2}{3}u_{DC}$	i_a	0	$-i_a$	i_a	i_a
\vec{u}_{ppn}	$\frac{2}{3}u_{DC}$	$-i_c$	0	i_c	$-i_c$	$-i_c$
\vec{u}_{npn}	$\frac{2}{3}u_{DC}$	i_b	0	$-i_b$	i_b	i_b
\vec{u}_{npp}	$\frac{2}{3}u_{DC}$	$-i_a$	0	i_a	$-i_a$	i_a
\vec{u}_{nnp}	$\frac{2}{3}u_{DC}$	i_c	0	$-i_c$	i_c	i_c
\vec{u}_{pnp}	$\frac{2}{3}u_{DC}$	$-i_b$	0	i_b	$-i_b$	$-i_b$

2.2.2 Switching nonidealities and their compensation

In practical VSCs, a blanking time is added between the turn-off and the turn-on of complementary switches to avoid cross-conduction within the bridge-leg [125]. The moment when the both switches are in the off-state is the dead-time. During the dead-time the AC terminal voltage of the converter is determined by the natural current commutation path and may therefore deviate from the desired. Also the voltage losses across the on-state semiconductors carrying the current deviate the phase voltages from the ideal. The aforementioned nonidealities increase the distortion of voltage and current waveforms, and can cause torque ripples in motor drive applications [126, 127], and estimation errors in sensorless control applications [128].

Blanking times

Table 2.3 classifies all the switch combinations of the NPC topology into six allowed ones and ten forbidden ones that lead to cross-conduction or possible switch overvoltage. The blanking times must be designed so that only the allowed combinations can occur, when the switching logic and the gate drive circuitry operate correctly. In summary, the following constraints must be fulfilled to prevent cross-conduction and overvoltages:

- To prevent cross-conduction, a blanking time must be inserted between the turn-off to turn-on transition of the switch pairs S_{ik} and $S_{(i+2)k}$ where $i \in \{1, 2\}$.
- To prevent overvoltages across the inner switches S_{2k} and S_{3k} , their turn-off must be delayed with respect to the turn-off of the outermost switches S_{1k} and S_{4k} .
- To prevent overvoltages across the inner switches S_{2k} and S_{3k} , the turn-on of S_{1k} and S_{4k} must be delayed with respect to the turn-on of S_{2k} and S_{3k} .

As a result, the blanking times must be designed so that the total turn-on and turn-off delays fulfil the following constraints: $T_{d(\text{off}),S1/S4} < (T_{d(\text{off}),S2/S3}, T_{d(\text{on}),S2/S3}) < T_{d(\text{on}),S1/S4}$.

Table 2.3: Classification of the switching states

	Allowed states	Cross-conduction or switch overvoltage	Possible switch overvoltage
s_{1k}	0 1 0 0 0 0	1 1 0 1 1	1 0 1 0 1
s_{2k}	0 1 1 0 1 0	1 1 1 1 0	0 0 0 1 0
s_{3k}	0 0 1 1 0 1	1 1 1 0 1	0 0 1 0 0
s_{4k}	0 0 0 1 0 0	1 0 1 1 1	0 1 0 1 1

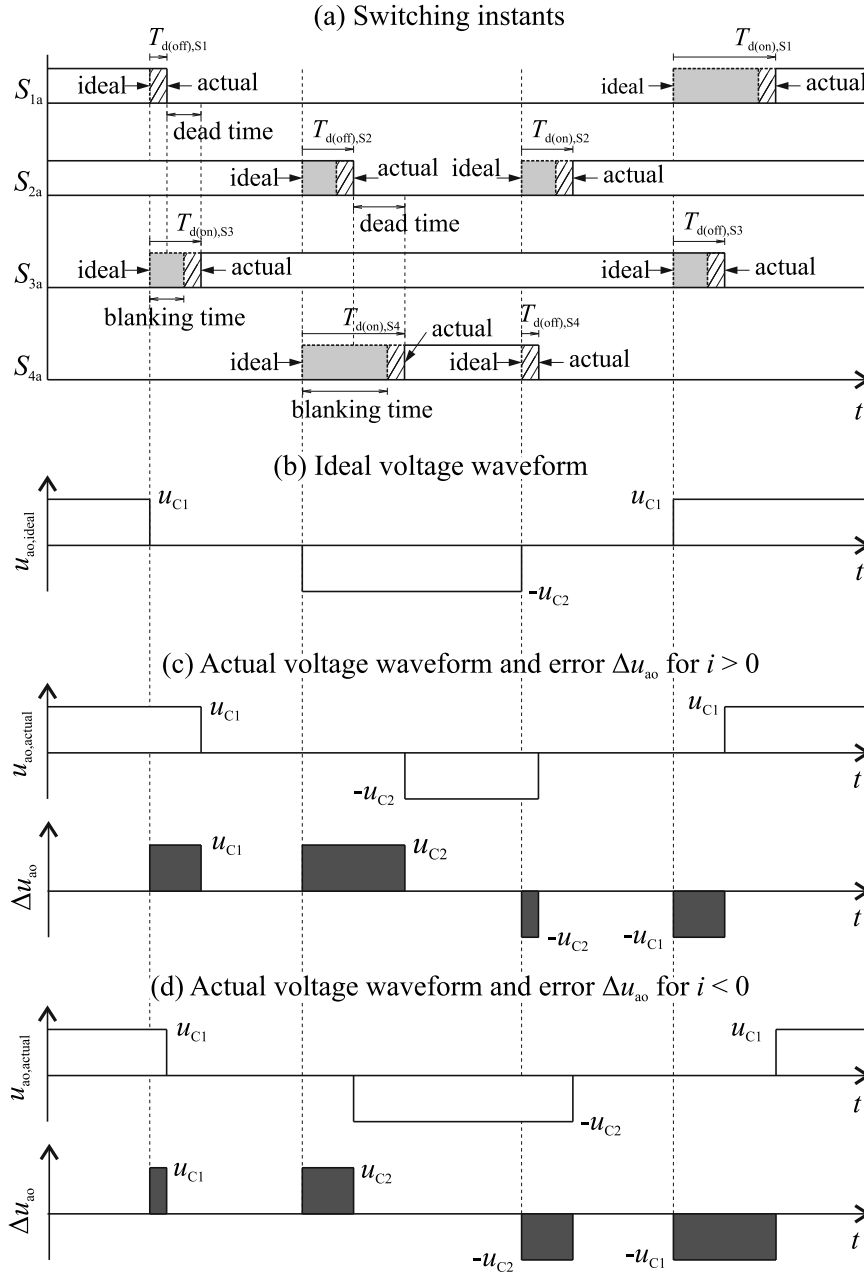


Fig. 2.3: Voltage errors generated by the switching delays. (a) Switching instants of S_{1a} to S_{4a} , (b) ideal u_{ao} waveform, (c) actual u_{ao} and error voltage waveform with positive phase current, (d) actual u_{ao} and error voltage waveform with negative phase current.

Fig. 2.3 illustrates the effect of blanking times and the finite switching times of the semiconductor switches on an example u_{ao} voltage waveform. The graph (a) shows the ideal and the actual switching instants of S_{1a} to S_{4a} . The graph (b) exemplifies the ideal voltage waveform. The graphs (c) and (d) depict the actual voltage waveform and the error voltage Δu_{ao} waveform with both positive and negative phase currents. The positive current is towards the converter. The lost (or gained) volt-seconds due to the blanking times and the switching delays are summarised in Table 2.4. It shows that the voltage error depends on three factors: (i) the switch transition applied, (ii) the phase current polarity at the switching instant, (iii) the delay between the ideal and the actual switch transition.

Table 2.4: Volt-second errors because of the blanking times and switching delays

u_{ko} voltage transition	$i > 0$	$i < 0$
$+u_{C1} \rightarrow 0$	$u_{C1}T_{d(on),S3}$	$u_{C1}T_{d(off),S1}$
$0 \rightarrow -u_{C2}$	$u_{C2}T_{d(on),S4}$	$u_{C2}T_{d(off),S2}$
$-u_{C2} \rightarrow 0$	$-u_{C2}T_{d(off),S4}$	$-u_{C2}T_{d(on),S2}$
$0 \rightarrow +u_{C1}$	$-u_{C1}T_{d(off),S3}$	$-u_{C1}T_{d(on),S1}$

Voltage losses across the on-state semiconductors

Fig. 2.4 illustrates the current paths in a bridge-leg. $u_{CE,on}$ denotes the on-state IGBT collector-to-emitter voltage and $u_{F,c}$ and $u_{F,fwd}$ denote the forward voltages of a clamp diode and a free-wheeling diode, respectively. The voltage losses are nonlinear functions of current but can be approximated as follows

$$u_{CE,on}(t) = U_{CE0} + r_{CE}i_C(t) \quad (2.8)$$

$$u_{F,fwd}(t) = U_{F0,fwd} + r_{F,fwd}i_{F,fwd}(t) \quad (2.9)$$

$$u_{F,c}(t) = U_{F0,c} + r_{F,c}i_{F,c}(t) \quad (2.10)$$

where U_{CE0} and U_{F0} denote the threshold voltages, r_{CE} and r_F denote the slope resistances, and $i_C(t)$ and $i_F(t)$ denote the IGBT collector current and the diode forward current, respectively. Based on Figs. 2.4(a) and 2.4(b), the actual phase voltage with respect to the DC bus midpoint can be expressed as summarised in Table 2.5. It shows that the volt-second error depends on the current polarity, on the applied switch combination, and its duty time.

Nonlinearity compensation methods

The two main categories of nonlinearity compensation methods found in scientific publications were originally developed for the two-level six-switch VSCs. In the case of average error compensation, the volt-seconds lost (or gained) during a switching period are calculated and the voltage reference is modified accordingly to cancel the

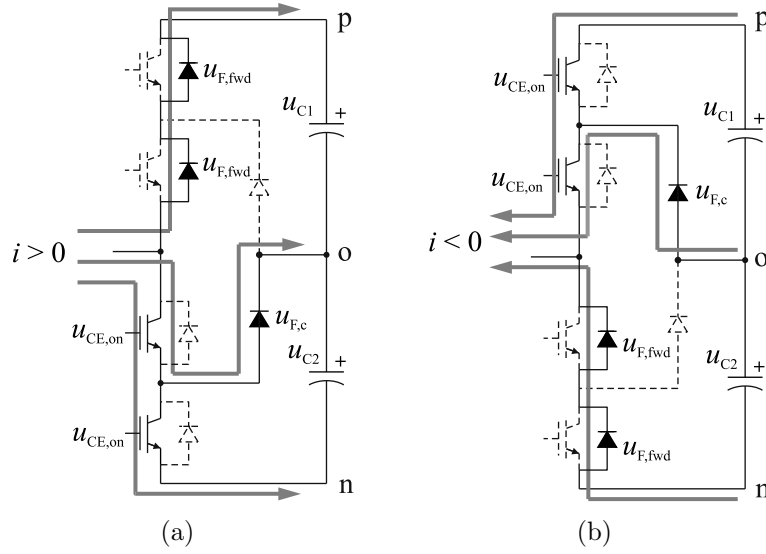


Fig. 2.4: Current paths in a bridge-leg with (a) positive phase current, and with (b) negative phase current.

Table 2.5: The phase-to-midpoint voltage when semiconductor voltage losses are considered

Ideal u_{ko} voltage	Actual voltage	
	$i > 0$	$i < 0$
$+u_{C1}$	$u_{C1} + 2u_{F,fwd}$	$u_{C1} - 2u_{CE,on}$
0	$u_{CE,on} + u_{F,c}$	$-u_{CE,on} - u_{F,c}$
$-u_{C2}$	$-u_{C2} + 2u_{CE,on}$	$-u_{C2} - 2u_{F,fwd}$

average error [126]. Regarding the pulse-based compensation, the duration of each PWM pulse is extended or reduced by the amount of dead-time before the blanking times are added [125].

The principles of aforementioned compensation methods have also been applied to the NPC converter [129, 130, 131, 132]. The dead-time compensation of a three-level GTO inverter is studied in [129] and three average error compensation methods are proposed. In [130], an average-error-based dead-time compensation method is proposed for a three-level-inverter-based induction motor drive. In [131], the dead-times of a five-level back-to-back converter are compensated using a pulse-based approach, and the semiconductor voltage losses are compensated on the average basis. In [132], the dead-times are compensated by manipulating the turn-on and the turn-off pulses through the control software.

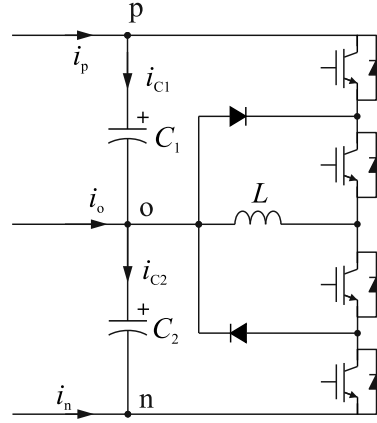


Fig. 2.5: A DC-DC converter for capacitor voltage balancing.

2.2.3 Capacitor voltage balancing

Unequal voltage distribution across the DC bus capacitors is a typical problem of multilevel converters. The DC voltage imbalance increases the switching losses and the thermal loading of the power semiconductors exhibiting increased voltage stress. Also overvoltage failures are possible. In addition, the output voltage and current distortion increases if the effect of imbalance on the output voltages is not compensated [133].

Next, the two main solutions to the capacitor voltage balancing problem of the NPC rectifier are presented. Firstly, additional circuitry can be used to control the voltage balance [134, 135, 136]. Fig. 2.5 illustrates the circuit proposed in [134]. It comprises an additional three-level switch-arm and an inductor, which is used as intermediate energy storage to exchange energy between the two DC capacitors. However, the drawbacks of the circuit are its complexity and, therefore, packaging problems, the need of additional control hardware, and the possibility of oscillations.

The other, the lowest cost solution, is to control the voltage balance by exploiting the switching state redundancy. In the case of carrier-based PWM, a feedback-controlled zero-sequence signal can be added to the reference voltages to control the duty time sharing between the redundant switching states [134]. Regarding the space-vector modulation (SVM), the duty time sharing of the redundant vectors can be manipulated directly [137]. However, the balancing strategies relying on the switching state redundancy are not problem-free. Firstly, if the duty times of the redundant vectors become too short, the control over the voltage balance can be lost. An exception is the SVM strategy proposed in [123]. It balances the capacitor voltages over the full output voltage range, but at the cost of higher switching frequency compared to the conventional SVM. Secondly, if the neutral-point voltage oscillation can not be fully suppressed, the output voltage distortion increases [137]. Thirdly, manipulation of the duty time distribution between the redundant vectors deviates the PWM waveform from the optimal and increases the voltage distortion [118, 117].

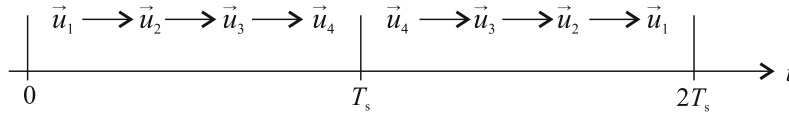


Fig. 2.6: Vector sequence over two switching periods T_s .

2.3 Multilevel space-vector modulation

The space-vector modulation (SVM), the concept of using space-vector quantities to compute the switching instants for a pulse-width modulated two-level six-switch voltage-source converter, was presented in the mid-1980s [138, 139]. Later, the theory has been extended to the modulation of multilevel converters [140, 116, 141, 142, 133, 143, 123, 121, 144, 72].

The multilevel SVM is more complex than the two-level SVM because of the larger number of available voltage vectors. More computational effort is needed to locate the reference vector within the voltage hexagon, to solve the duty cycles, and to determine the voltage vector sequence. On the other hand, the available vectors can be used to optimise the switching waveforms [117, 121, 119], to reduce the switching losses [118, 145], to balance the DC bus capacitor voltages [123], and to avoid the minimum-pulse-length violations [146].

2.3.1 Symmetric and asymmetric regular sampling

The concepts of symmetric and asymmetric regular sampling are known from the theory of digital pulse-width modulation [147]. In the case of regularly sampled sine-triangle PWM, the reference can be sampled at the positive and negative peaks of the carrier wave. Regarding the symmetrical sampling mode (single-update-mode), the reference is sampled once per a carrier period, either at the positive or the negative peaks. In the asymmetrical sampling mode (double-update-mode), the reference is sampled at the both peaks.

The both regular sampling modes can be applied to the SVM. Fig. 2.6 exemplifies a vector sequence during two adjacent switching periods T_s . The sequence of the latter period is reversed to minimise the switching frequency. In the asymmetric sampling mode, the duty cycles are updated in the beginning of each switching period, which is equivalent to sampling at the both peaks of the carrier wave. In the symmetric regular sampling mode, the duty cycles are updated only once per $2T_s$.

2.3.2 Continuous and discontinuous PWM

The characteristics of a PWM strategy can be modified by adding zero-sequence waveforms to the modulation signals [147]. As a result, benefits such as extended linear modulation range, improved waveform quality, reduced switching losses, and

diminished common-mode voltages can be achieved [148].

The minimum voltage harmonic content can be achieved with continuous PWM strategies [117, 118]. They use four switching states during a switching period which generates one switched transition in each leg [147]. Discontinuous PWM (DPWM) strategies yield suboptimal harmonic content but reduced switching frequency and losses [147]. DPWM is achieved by injecting a zero-sequence voltage to the control voltage so that the average volt-seconds do not change, but one voltage pulse is eliminated during each switching period. As a result, only three switching states are used during a switching period. Furthermore, by selecting a suitable zero-sequence signal, each phase-leg can be kept unswitched and clamped to one DC bus node for a given portion of the fundamental frequency period.

Discontinuous SVM of the three-level NPC converter can be implemented by using the phase-leg discontinuity patterns known from the two-level modulation theory [116, 148]. Based on the clamping period lengths, the DPWM patterns can be categorised as follows:

- DPWM0, DPWM1, and DPWM2 result in 60° clamping period.
- DPWM3 results in 30° clamping period.
- The patterns DPWMMAX and DPWMMIN yield 120° clamping periods and they are obtained by combining DPWM0 and DPWM2.

Fig. 2.7 illustrates the clamping periods generated by the DPWM patterns under study during one cycle around the voltage hexagon. Within each region of the voltage hexagon, the phase-leg clamping is expressed using three-character coding: (i) 'x' denotes that the phase-leg is being switched during a switching period, (ii) 'p', 'o', and 'n' describe the DC bus nodes to which the unswitched phase-leg is being clamped. Within the outermost subsectors, the unswitched phase-leg is clamped to either the positive or the negative DC bus. Within the inner subsectors, the clamping is done to the DC bus midpoint 'n', and therefore, the zero vectors \vec{u}_{nnn} and \vec{u}_{ppp} never get employed, similarly as in [120].

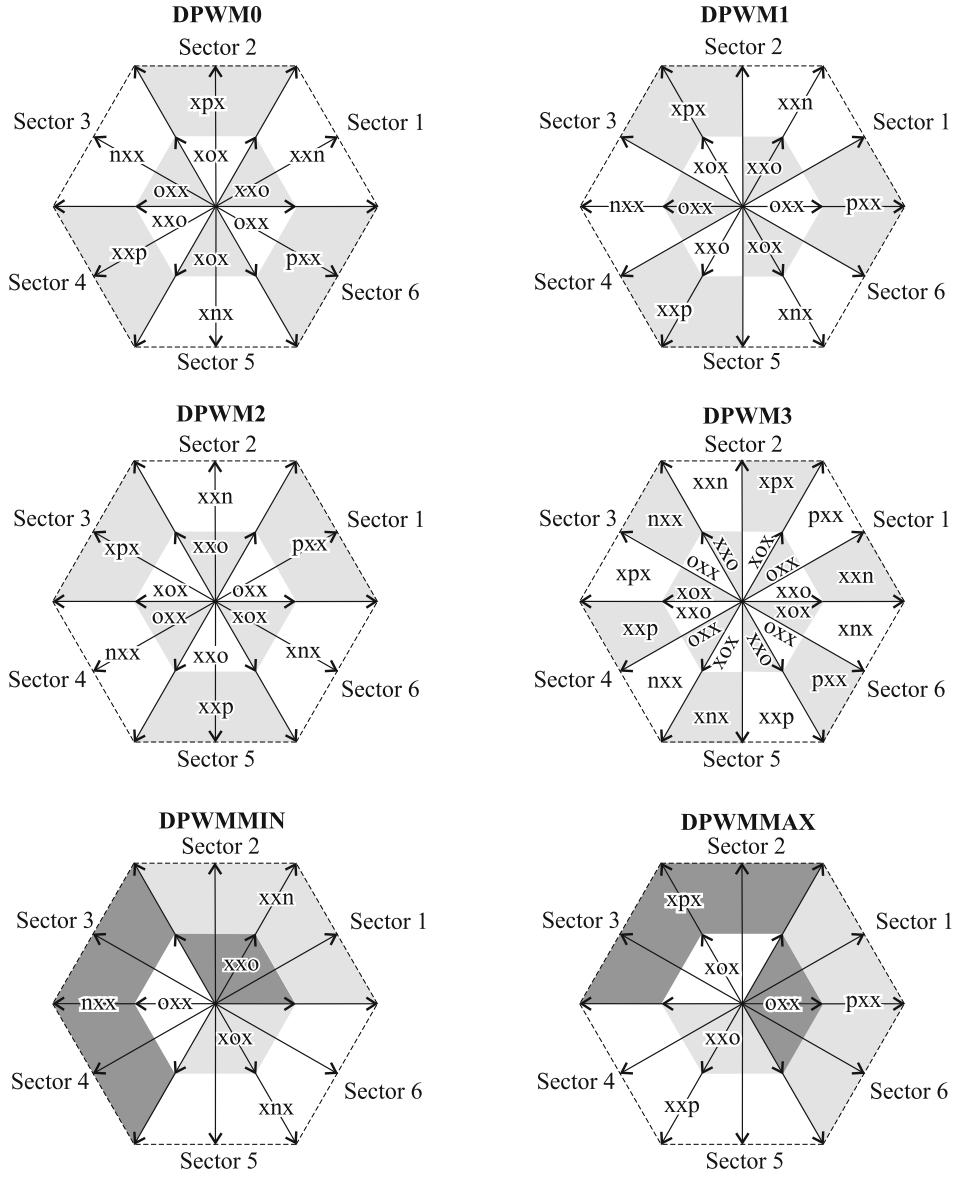


Fig. 2.7: Phase-leg discontinuities of the three-level converter when the DPWM patterns known from the modulation theory of two-level converters are applied.

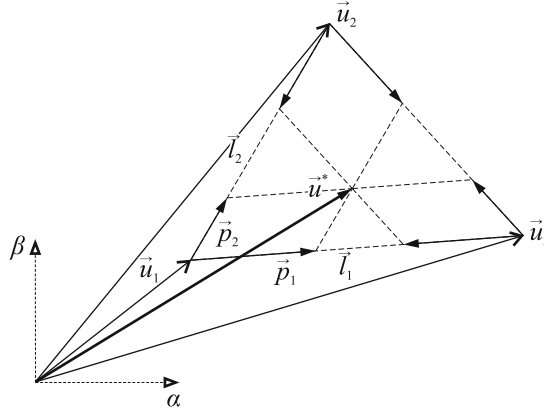


Fig. 2.8: Vector projections of \vec{u}^* along the edges of the triangular region defined by the nearest three vectors.

2.3.3 Duty cycles solution based on vector projections

The duty cycles can be solved by expressing the reference vector \vec{u}^* as a sum of a base vector and two vector projections. Fig. 2.8 illustrates the reference \vec{u}^* located within the triangular area (subsector) defined by \vec{u}_1 , \vec{u}_2 , and \vec{u}_3 . For example, if \vec{u}^* is projected in the direction of $\vec{l}_1 = \vec{u}_3 - \vec{u}_1$ and $\vec{l}_2 = \vec{u}_2 - \vec{u}_1$, the two vector projections \vec{p}_1 and \vec{p}_2 are obtained and \vec{u}^* can be expressed as

$$\vec{u}^* = \vec{u}_1 + \vec{p}_1 + \vec{p}_2 \quad (2.11)$$

If the lengths of \vec{p}_1 and \vec{p}_2 are proportioned to the lengths of \vec{l}_1 and \vec{l}_2 , respectively, one can obtain

$$\vec{u}^* = \vec{u}_1 + \frac{\|\vec{p}_1\|}{\|\vec{l}_1\|}(\vec{u}_3 - \vec{u}_1) + \frac{\|\vec{p}_2\|}{\|\vec{l}_2\|}(\vec{u}_2 - \vec{u}_1) \quad (2.12a)$$

$$= (1 - \frac{\|\vec{p}_1\|}{\|\vec{l}_1\|} - \frac{\|\vec{p}_2\|}{\|\vec{l}_2\|})\vec{u}_1 + \frac{\|\vec{p}_2\|}{\|\vec{l}_2\|}\vec{u}_2 + \frac{\|\vec{p}_1\|}{\|\vec{l}_1\|}\vec{u}_3 \quad (2.12b)$$

$$= d_1\vec{u}_1 + d_2\vec{u}_2 + d_3\vec{u}_3 \quad (2.12c)$$

where d_1 , d_2 , and d_3 are the duty cycles of \vec{u}_1 , \vec{u}_2 , and \vec{u}_3 , respectively, and subject to constraint $d_1 + d_2 + d_3 = 1$. Eq. (2.12b) applies irrespective of the converter topology and the number of DC bus voltage levels. It shows that the duty cycles solution requires the lengths of two triangle (subsector) edges and the projections of the reference vector along them.

2.3.4 Capacitor voltage feedforward

Various multilevel SVM algorithms assume that the DC bus capacitor voltages are perfectly balanced [116, 120, 141, 149]. In that case, the voltage vector hexagon is composed of equilateral triangular regions and can be normalised so that \vec{l}_1 and \vec{l}_2

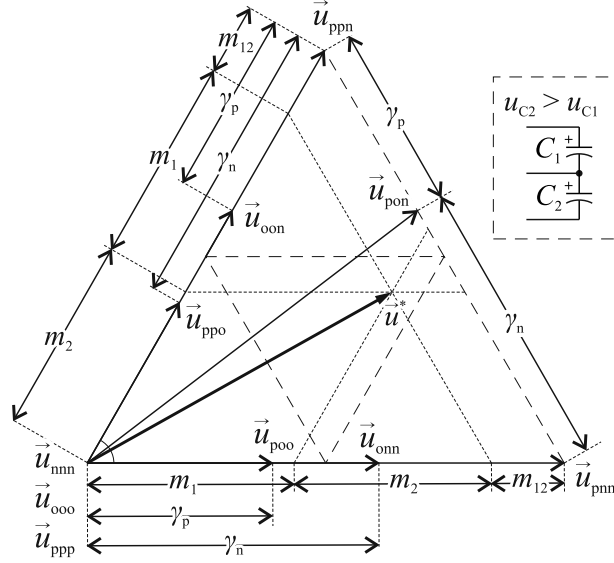


Fig. 2.9: The variables needed to compensate the effect of capacitor voltage imbalance.

in Fig. 2.8 are of unity lengths. As a result, only the projections lengths $\|\vec{p}_1\|$ and $\|\vec{p}_2\|$ are needed to solve (2.12b). However, if the capacitor voltages are unbalanced, the reference is not realised accurately and the distortion of converter voltage and current waveforms increases. It is shown in [137] that the neutral-point voltage variation of the three-level NPC converter can not be mitigated over the entire modulation index range when the modulation is based on the nearest three vectors (NTV). Therefore, it is justified that the modulation algorithm should consider the DC bus voltage imbalance.

Fig. 2.9 illustrates the Sector 1 when $u_{C2} > u_{C1}$. The imbalance varies the lengths of the short vectors and both the length and the angle of the medium vector \vec{u}_{pon} . The long vectors are affected only by the total DC bus voltage. According to [133], the voltage imbalance can be considered during the duty cycles solution with the help of variables m_1 , m_2 , m_{12} , γ_n , and γ_p depicted in Fig. 2.9. Next, the theory behind the method is reviewed.

The scalar projections m_1 and m_2 of \vec{u}^* along \vec{u}_{pnn} and \vec{u}_{ppn} are obtained using the *gh* transformation reviewed in Appendix A. The projections are normalised with base voltage $\frac{1}{3}u_{DC}$ which equals the short vector length when $u_{C1} = u_{C2}$. As a result, the third projection m_{12} can be expressed as

$$m_{12} = 2 - m_1 - m_2 \quad (2.13)$$

Variables γ_n and γ_p denote the lengths of the negative and the positive short vectors, respectively. Their normalised lengths are subject to constraint $\gamma_p + \gamma_n = 2$, and

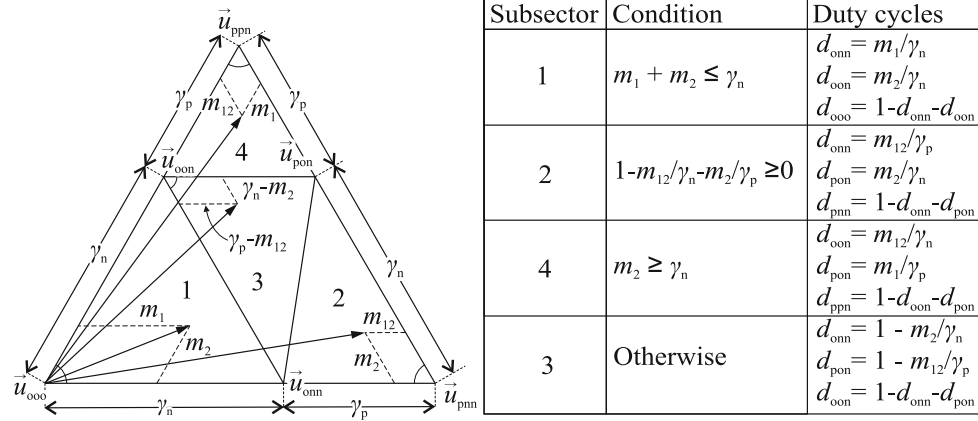


Fig. 2.10: An example of the duty cycles solution in subsectors 1-4 of Sector 1.

can be expressed as

$$\gamma_n = \frac{\frac{2}{3}u_{C2}}{\frac{1}{3}u_{DC}} = \frac{2u_{C2}}{u_{DC}} \quad (2.14)$$

$$\gamma_p = \frac{\frac{2}{3}u_{C1}}{\frac{1}{3}u_{DC}} = \frac{2u_{C1}}{u_{DC}} \quad (2.15)$$

The duty cycles can be solved according to (2.12b) if two edge lengths of the triangle enclosing \vec{u}^* and the scalar projections of \vec{u}^* on those two edges are known. Based on Fig. 2.9, the two constraints are fulfilled by the NTV combinations which require only two switched transitions per a switching period, because

- at least two subsector edge lengths can be described with γ_n and γ_p
- lengths of at least two projections of \vec{u}^* on the subsector edges can be described with m_1 , m_2 , and m_{12}

Fig. 2.10 gives an example of the duty cycles calculation in subsectors 1-4 of Sector 1. The base vector is always selected from the subsector edge which measures a 60° angle. The same principle can be applied to the other main sectors, and to the DPWM patterns discussed in Section 2.3.2.

2.3.5 Limiting of the reference vector length

The modulation index describes the normalised fundamental frequency voltage generated with pulse-width modulation. In [150], the modulation index of two-level VSC is defined as the ratio of the fundamental frequency modulated voltage \hat{U}_1 to

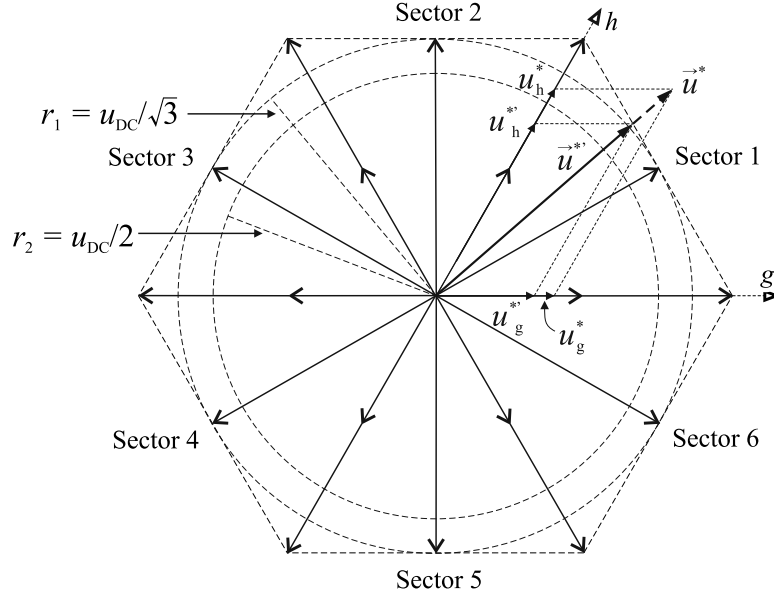


Fig. 2.11: The principle of the space-vector limit method implemented in the gh coordinates.

the fundamental frequency voltage $\hat{U}_{1,\text{six-step}}$ during the six-step operating mode:

$$m = \frac{\hat{U}_1}{\hat{U}_{1,\text{six-step}}} = \frac{\hat{U}_1}{\frac{2}{\pi}u_{\text{DC}}} \quad (2.16)$$

In [151], the amplitude modulation ratio m_a of sine-triangle PWM without zero-sequence voltage injection is defined as follows

$$m_a = \frac{\hat{U}_{\text{control}}}{\hat{U}_{\text{triangle}}} = \frac{\hat{U}_1}{\frac{1}{2}u_{\text{DC}}} \quad (2.17)$$

where \hat{U}_{control} is the control voltage amplitude and $\hat{U}_{\text{triangle}}$ is the amplitude of triangular carrier wave. Within the linear region, with $m_a \leq 1$, the modulation generates sinusoidal fundamental frequency voltages superimposed by the PWM harmonics. Overmodulation starts when $m_a > 1$ and the waveform approaches six-step. With suitable zero-sequence voltage injection, the linear region can be extended by the factor $2/\sqrt{3}$. The same extension is provided by the SVM.

In Fig. 2.11, \vec{u}^* extends outside the voltage hexagon and must be limited to enable correct operation of the SVM. Various reference length limiting methods, including the space-vector limit (SVL), have been put forward in [152]. The principle of the SVL method is illustrated in Fig. 2.11 in the gh reference frame¹. Basically, it

¹The gh reference frame transformation is reviewed in Appendix A

retains the angle of \vec{u}^* , but scales its length so that the whole voltage hexagon is used.

The reference extends outside the hexagon, and must be limited, if

$$\|\vec{u}^*\| = u_g^* + u_h^* > \frac{2}{3}u_{DC} \quad (2.18)$$

The vector components of the scaled reference $\vec{u}^{*'}$ can be expressed as

$$u_g^{*'} = u_g^* \frac{\frac{2}{3}u_{DC}}{u_g^* + u_h^*} \quad (2.19)$$

$$u_h^{*'} = u_h^* \frac{\frac{2}{3}u_{DC}}{u_g^* + u_h^*} \quad (2.20)$$

In Fig. 2.11, the circle with radius $r_1 = u_{DC}/\sqrt{3}$ is the boundary of linear modulation range for SVM and for sine-triangle PWM modified with an injection of suitable zero-sequence voltage. The circle with radius $r_2 = u_{DC}/2$ is $m_a = 1$ for the conventional sine-triangle PWM.

2.4 Vector control of STATCOM

Fig. 2.12 illustrates a control block scheme of a STATCOM based on the three-level NPC rectifier. The LC filter is inserted on the grid-side of the boost inductor L_1 to reduce the switching harmonic currents entering the grid [153, 154]. The vector control scheme is implemented in the grid-voltage-oriented dq reference frame². The angle θ_g^+ of the positive-sequence grid voltage is needed in the $abc - dq$ and $dq - \alpha\beta$ transformations. It is solved by the phase-locking loop (PLL) which synchronises with the grid.

The control comprises two nested feedback loops. The outer loop regulates the DC bus voltage and provides the reference i_{1d}^* for the d -axis current. The inner loop controls the feedback current and provides the reference \vec{u}_1^* for the space-vector modulator (SVM). The feedback is taken from either the rectifier current or the grid current. The grid voltage feedforward is typically used to improve the current control performance. Also other filter state variables, such as the filter capacitors' voltages or currents, or the currents from the both sides of the filter, can be measured for control purposes [155].

The benefit of grid-voltage-oriented vector control is that it turns the fundamental frequency currents and voltages into DC quantities. Therefore, the steady-state errors can be eliminated with PI compensators. On the other hand, similar performance is also achieved with proportional-resonant controllers implemented in the $\alpha\beta$ reference frame [94]. Other control strategies studied in scientific literature include direct power control [156], model predictive control [157], and voltage-mode control [158]. However, this thesis focuses on the control scheme described in Fig. 2.12.

²The theory of dq transformation is reviewed in Appendix A

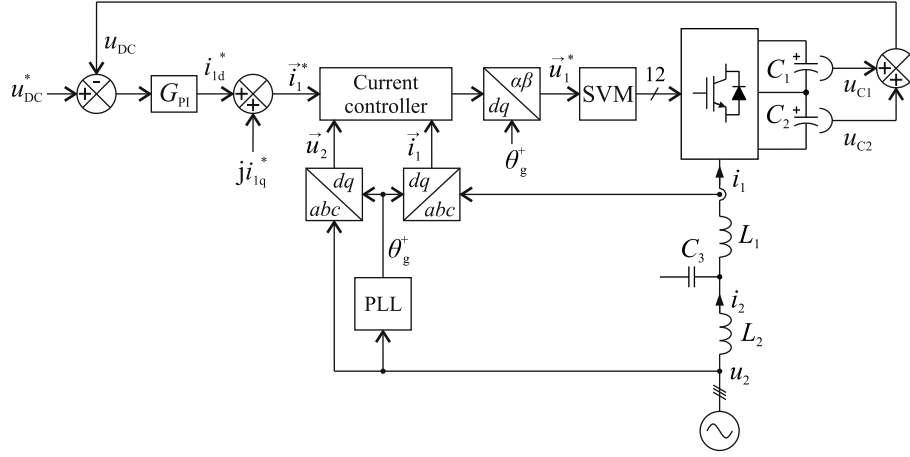


Fig. 2.12: Block scheme of a STATCOM based on the three-level NPC rectifier and a vector control system implemented in the grid-voltage-oriented dq reference frame.

2.4.1 Synchronisation with the grid

The STATCOM should stay online during the abnormal grid conditions and support the network so that the other equipment could operate uninterruptedly. Therefore, a robust synchronisation strategy is needed. At simplest, the phase-angle can be solved by observing the zero-crossing instants of the grid voltages, or by calculating the angle of the $\alpha\beta$ reference frame grid voltage vector. The dynamics of the former method is limited because the phase-tracking is not possible between the zero-crossings [159]. The problem of the latter solution is that it works only with sinusoidal and symmetrical voltages. More advanced PLLs can detect the grid phase-angle in the synchronous reference frame [159, 160] or employ adaptive filters to increase the phase-tracking accuracy and selectivity [161, 162].

Fig. 2.13 illustrates the block diagram of the dual second-order generalised integrator frequency-locked loop (DSOGIFLL) which is used in this thesis to synchronise the STATCOM with the grid. The DSOGIFLL is frequency adaptive and provides very good performance also in unbalanced and distorted grids [163, 162]. It extracts the fundamental frequency grid voltage components in the $\alpha\beta$ reference frame using two adaptive band-pass filters, namely the SOGI-QSGs³. The first filter generates the in-quadrature signals $\tilde{u}_{2\alpha}$ and $q\tilde{u}_{2\alpha}$ where q denotes a -90° phase-shift. The second filter generates the signals $\tilde{u}_{2\beta}$ and $q\tilde{u}_{2\beta}$. The gain K determines the filter bandwidth [162]. The center frequency ω_0 of the SOGI-QSGs is adapted to the grid frequency ω_g by the frequency-locked loop (FLL). At the center frequency, the filters have unity gains.

The FLL input is the product $(u_{2\alpha} - \tilde{u}_{2\alpha})q\tilde{u}_{2\alpha}$. It has been shown in [164] that $u_{2\alpha} - \tilde{u}_{2\alpha}$ and $q\tilde{u}_{2\alpha}$ are in phase when $\omega_g < \omega_0$, and in the opposite phase when $\omega_g > \omega_0$. Therefore, the average value of $u_{2\alpha} - \tilde{u}_{2\alpha}$ is positive for $\omega_g < \omega_0$, negative for $\omega_g > \omega_0$, and zero for $\omega_g = \omega_0$. As a result, an integrating controller with a negative gain $-K_i$ compensates the error and regulates ω_0 at the grid frequency. In

³SOGI-QSG = Second-order generalised integrator - quadrature signal generator

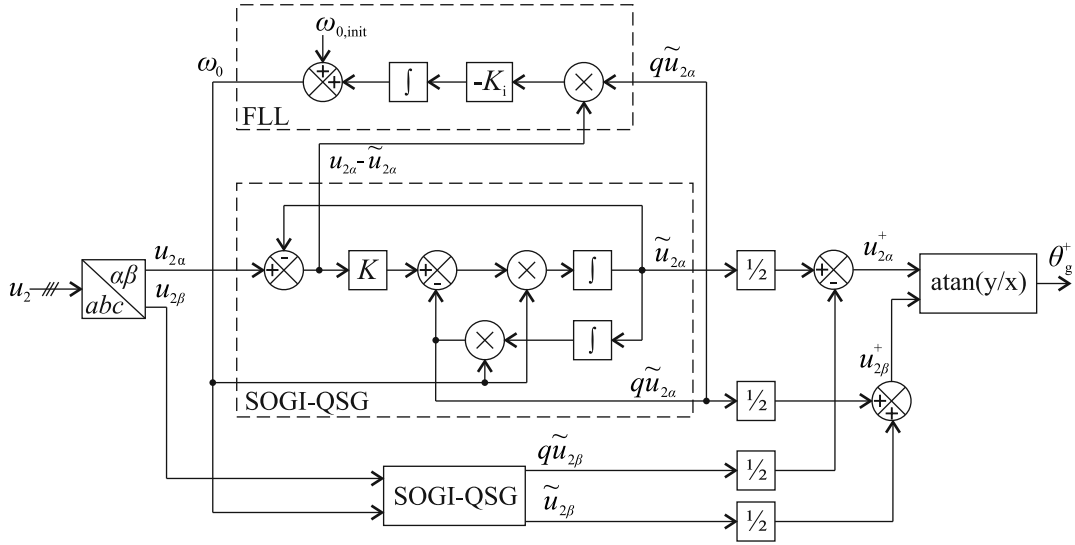


Fig. 2.13: Block diagram of the dual second-order generalised integrator frequency-locked loop (DSOGIFLL).

Fig. 2.13, the initial value $\omega_{0,\text{init}}$ equals the nominal grid angular frequency and its purpose is to reduce the settling time of the synchronisation.

Finally, the positive-sequence grid voltage components are calculated from the SOGI-QSG outputs using the following transformation [163]

$$\begin{bmatrix} u_{2\alpha}^+ \\ u_{2\beta}^+ \end{bmatrix} = \begin{bmatrix} \frac{1}{2} & -\frac{1}{2}q \\ \frac{1}{2}q & \frac{1}{2} \end{bmatrix} \begin{bmatrix} \tilde{u}_{2\alpha} \\ \tilde{u}_{2\beta} \end{bmatrix} \quad (2.21)$$

and the angle θ_g^+ is solved by calculating the arctangent of $u_{2\alpha}^+$ and $u_{2\beta}^+$.

2.4.2 DC voltage control

The DC bus voltage is regulated at the given setpoint by controlling the active power drawn from the network. At steady state, the active power equals the STATCOM power losses. The instantaneous power of the STATCOM can be expressed in the grid-voltage-oriented dq reference frame as follows:

$$p = \frac{3}{2} \text{Re}\{\vec{u}_2 \vec{i}_2^*\} = \frac{3}{2} (u_{2d} i_{2d} + u_{2q} i_{2q}) \quad (2.22)$$

Let us assume sinusoidal and balanced three-phase network. Then, u_{2d} equals the peak value of the phase voltage and u_{2q} is zero. As a result, the instantaneous power flow between the grid and the STATCOM can be controlled through the d -axis current.

The error between the reference and the actual DC bus voltage is compensated with a PI controller. The bandwidth of the control loop must be designed substantially low to prevent it reacting on the low-frequency harmonic components present in the DC voltage. Otherwise, the rectifier will inject low frequency current harmonics

to the network. Typically the dominant DC bus voltage harmonic is the sixth. The second harmonic is superimposed on the DC voltage if the rectifier controls fundamental frequency negative sequence current.

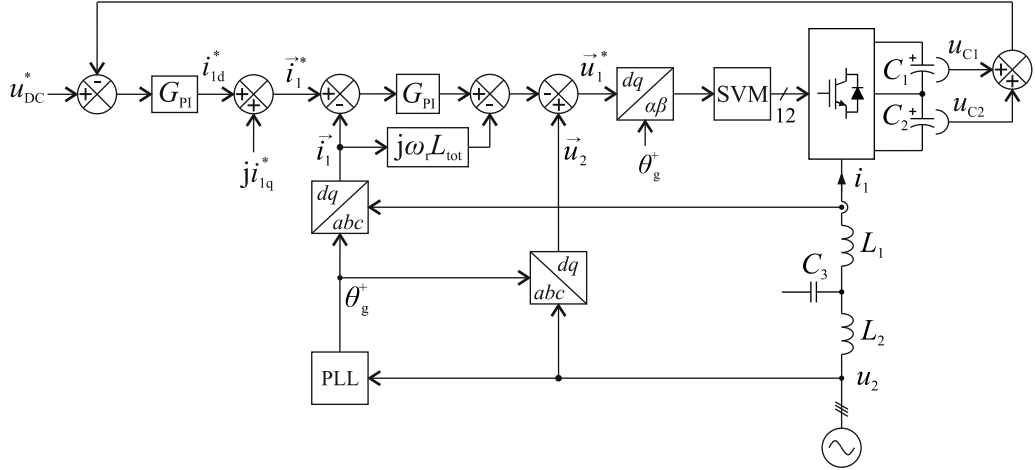
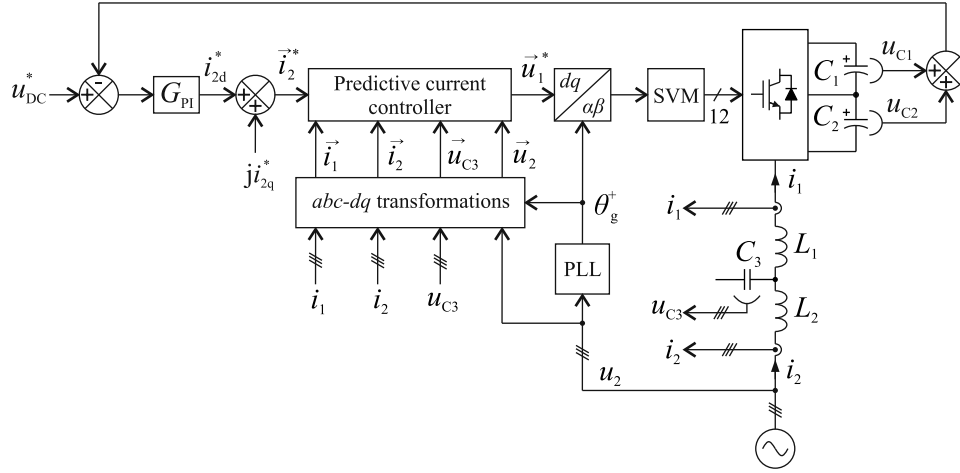
2.4.3 Grid current control

The key issues of the grid current control are dynamics, disturbance rejection capability, and stability. Grid voltage background distortion causes current harmonics if the control bandwidth is insufficient. Proportional-resonant harmonic controller [165] or repetitive controller [108] in parallel with the main controller has been proposed as a solution. In [107], multiple rotating vector reference frames and integrating controllers are used to eliminate the effect of grid voltage distortion and to maintain sinusoidal currents. However, grid impedance variations can compromise the stability of the harmonic current controllers [165]. Also sudden grid voltage changes, especially asymmetrical voltage dips, can cause control problems such as current distortions and asymmetry, power oscillations, and DC bus oscillations [107]. In [107, 166], two vector reference frames, one for the positive sequence and the other for the negative sequence, are used to improve the converter performance during unbalanced grid voltages.

Another problem is the resonant peak of the LCL filter, which may cause oscillations and instability. The resonant peak can be mitigated by increasing the natural filter damping but it deteriorates the filtering efficiency and increases the power losses. Active damping can be used to avoid extra losses if the resonance is within the control bandwidth [154]. However, parametric uncertainty [155, 154] and grid impedance variation [165] can compromise the stability. Also additional voltage or current sensors may be needed [167].

This thesis studies the current control strategies illustrated in Figs. 2.14 and 2.15. In Fig. 2.14, the rectifier current is controlled using PI controllers. The scheme is based on the approximation that, sufficiently below the LCL filter resonance, the grid current is proportional to the voltage across the series inductance $L_{\text{tot}} = L_1 + L_2$ and the filter capacitor mainly affects the phase-angle of the fundamental frequency grid current [153]. The cross-coupling resulting from the $abc - dq$ transformation is compensated with the term $j\omega_r L_{\text{tot}} \vec{i}_1$, where ω_r is the angular frequency of the rotating synchronous reference frame. When the synchronisation is ideal, $\omega_r = \omega_g$. The feedback is taken from the rectifier current which enables overcurrent protection of the semiconductor bridge. The effect of the LC filter on the power factor can be compensated by adding an offset term to i_{1q}^* [101, 102, 84].

Fig. 2.15 describes a predictive vector current control scheme, which uses the system model to predict the future behaviour of the grid current [104, 105, 99, 106, 152, 168, 169, 170]. The optimum controller actuation, the deadbeat response, compensates the control error within the minimum possible number of control sampling intervals. In practice, it might be necessary to parametrise the controller with fractions of deadbeat gains, because measurement noise and parametric uncertainty can cause

**Fig. 2.14:** Decoupled PI current controllers.**Fig. 2.15:** Predictive vector current controller.

oscillations, even instability [166]. The controller needs the feedback of all filter state variables or, alternatively, the non-measured states can be estimated.

2.4.4 Control delays

The modulator is updated at the beginning of each switching period based on the previous control algorithm iteration. As a result, a delay equal to one control computation interval is automatically included in the control action. Also the modulator causes a delay between its input and output [171, 103]. The delays limit the current control bandwidth [172] and may cause oscillatory responses, amplification of harmonic currents, and stability problems [173].

The modulator delay

The delays of single and double-update-mode regularly sampling digital PWM have been studied in [171]. The double-update-mode provides smaller delay which is equal to half the switching period. The delay can be reduced further if the sampling frequency of the feedback signals is increased with respect to the carrier frequency [172, 174]. Multi-sampling provides broader control bandwidth compared to single-sampling control but a suitable ripple cancellation technique is needed to remove the switching ripple from the feedback currents. Additionally, a powerful DSP and/or FPGA is needed to implement the time-critical algorithms [172].

The effect of computation delay on the dq transformation

The control computation and single-sampling PWM yield a total delay $T_d \approx \frac{3}{2}T_s$, where T_s is the sampling time. During T_d the positive-sequence grid voltage vector rotates $\Delta\theta_g^+ = \omega_g T_d$ and reaches the value $\|\vec{u}_2\|e^{j(\theta_g^+ + \Delta\theta_g^+)}$. The effect of T_d on the dq transformations can be compensated by modifying the angle used in the $dq - \alpha\beta$ transformation of the rectifier voltage reference as follows: $\vec{u}_1^{*\alpha\beta} = \vec{u}_1^{*dq} e^{j(\theta_g^+ + \Delta\theta_g^+)}$.

Compensation of the control computation delay

Various methods have been proposed in scientific literature to compensate the control computation delay. In [175], the sampling instant of single-sampling control is delayed by the amount of CPU time that remains unused during the control update interval. It decreases the control delay but the currents are no longer sampled at the zero-crossings of the ripple waveform. Therefore, the ripple component included in the measurement has to be removed accurately to prevent it disrupting the control action.

Another way to reduce the delay in the control action is to manipulate the reference signals [176, 177, 173, 178, 179, 180, 83]. A simple method to predict the reference signal evolution is to use linear extrapolation [176]. If the reference signal is periodic and repeating, the data of one full period can be stored into the random-access memory of the control hardware. Then, at each control update interval, the stored data points are advanced by the length of the delay to compensate it [179, 177].

Alternatively, the discrete frequency components of interest can be extracted from the reference signal, phase-advanced, and then summed to reconstruct the signal [181, 173, 178]. A similar result is achieved using integrating controllers [179, 182, 180]. The methods provide satisfactory accuracy during the steady state but the finite settling times of the filters and integrating controllers limit the dynamic performance.

It is common to the delay compensation methods based on the manipulation of the reference signals that the delay inherent in the control loop remains intact.

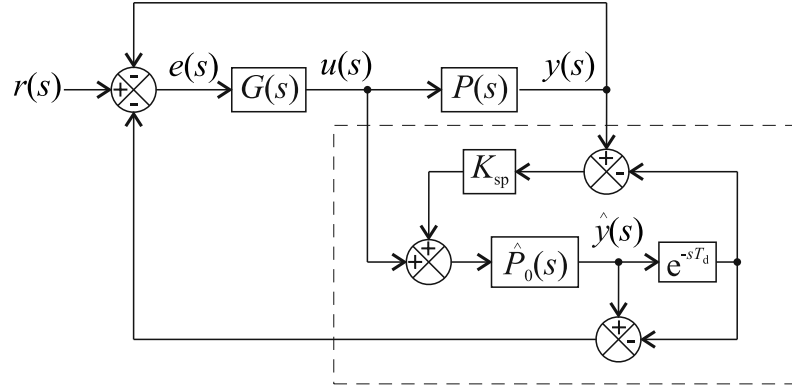


Fig. 2.16: Block scheme of the Smith predictor.

Smith predictor

Fig. 2.16 presents the block scheme of the Smith predictor [183] which has been applied to the control delay compensation of power converter applications in few scientific publications such as [152, 106, 166]. The predictor comprises a delayless process model $\hat{P}_0(s)$ in parallel with the actual process $P(s)$ with the time delay e^{-sT_d} . The process model output $\hat{y}(s)$ is the prediction of what $y(s)$ would be without the delay. The feedback $K_{sp}(y(s) - \hat{y}(s)e^{-sT_d})$ is added to the process model input to compensate load disturbances. The predicted delayless output $\hat{y}(s)$ and the error $y(s) - \hat{y}(s)e^{-sT_d}$ are fed back to the controller $G(s)$. The control error is given as

$$e(s) = r(s) - (y(s) - \hat{y}(s)e^{-sT_d}) - \hat{y}(s) \quad (2.23)$$

where $r(s)$ is the reference signal. The closed-loop transfer function from the reference to the output can be written as

$$\frac{y(s)}{r(s)} = \frac{G(s)P(s)(1 + K_{sp}\hat{P}(s))}{1 + G(s)\hat{P}_0(s) + G(s)(P(s) - \hat{P}(s)) + K_{sp}(\hat{P}(s) + G(s)P(s)\hat{P}_0(s))} \quad (2.24)$$

If $\hat{P}(s) = P(s)$ and $K_{sp} = 0$, (2.24) reduces to

$$\frac{y(s)}{r(s)} = \frac{G(s)\hat{P}_0(s)}{1 + G(s)\hat{P}_0(s)} e^{-sT_d} \quad (2.25)$$

which shows that the closed-loop response is similar to the delayless system, but it has the time delay T_d . As a result, in the ideal case, the controller can be designed similarly as for a delayless system.

2.5 Conclusions

Firstly, the fundamentals of the three-level neutral-point clamped boost rectifier were reviewed in this chapter. After that, the following problems affiliated with the rectifier control were studied:

1. Voltage errors caused by blanking times and voltage loss across the on-state semiconductors
2. Capacitor voltage balancing
3. Discontinuous multilevel space-vector modulation and duty cycles solution
4. Vector current control in the grid-voltage-oriented coordinates

The first three problems relate to the first objective of this thesis, that is implementing of the modulation strategy. Based on the literature review, it can be said that various solutions exist to each of the problems. However, they typically focus on one problem at a time. There is an obvious gap for a research of modulation algorithms that compensate simultaneously the effects of capacitor voltage imbalance, dead-times, and voltage losses across the on-state semiconductors. Therefore, further research is needed to investigate on how such modulators should be implemented and what problems they enclose.

The last problem area considered the vector current control of STATCOM. The grid current controller mainly determines the performance of the application. The three key issues are disturbance rejection capability, dynamic behaviour, and stability. The grid current control is a very active research topic because it provides highly important research problems for various power conversion applications. This thesis studies the characteristics of two vector current control strategies which were briefly introduced in Section 2.4.3. Based on the literature survey, the issues with control delays have also been widely studied but only a few studies focus on the delay compensation using the Smith predictor. Therefore, further research is needed to reveal the performance of the predictor and its suitability to practical power converter applications. In this thesis, the Smith predictor is incorporated in the applied grid current controllers.

Chapter 3

Modelling

3.1 Introduction

This chapter introduces the studied STATCOM and its analytical models are developed for the purposes of grid current control design and analysis. Firstly, the schematic of the STATCOM is presented in Section 3.2, and a linear, time-invariant average model is developed. In Section 3.3, the filter inductors are modelled with frequency-dependent equivalent circuits and are included in the average model. In Section 3.4, the grid impedance is included in the models to assess its effect on the current control stability. The conclusions are drawn in Section 3.5.

3.2 Average model

Fig. 3.1 shows the schematic of the three-level STATCOM. It is connected to a three-phase mains by using a passively damped *LCL* filter circuit. The inductors L_3 have been inserted in parallel with the damping resistors R_d to reduce the ohmic losses caused by the fundamental frequency shunt branch current. The series resonance of L_3C_3 is tuned at half the modulation frequency, at 1800 Hz, to increase the attenuation of switching harmonics. The series resistors R_C were inserted in the circuit after the first laboratory prototype tests to increase the filter resonance damping. However, inserting passive damping in series with the filter capacitors is not desirable, which should be considered in the future research. The frequency responses of the filter circuit are presented in Appendix C.

Let us assume that the rectifier shown in Fig. 3.1 is supplied from an ideal three-phase grid, there is no path for the zero-sequence current, and the impedances are frequency-independent and symmetrical between the three phases. Then, the state variables of the filter circuit, as well as the filter shunt branch voltage, can be

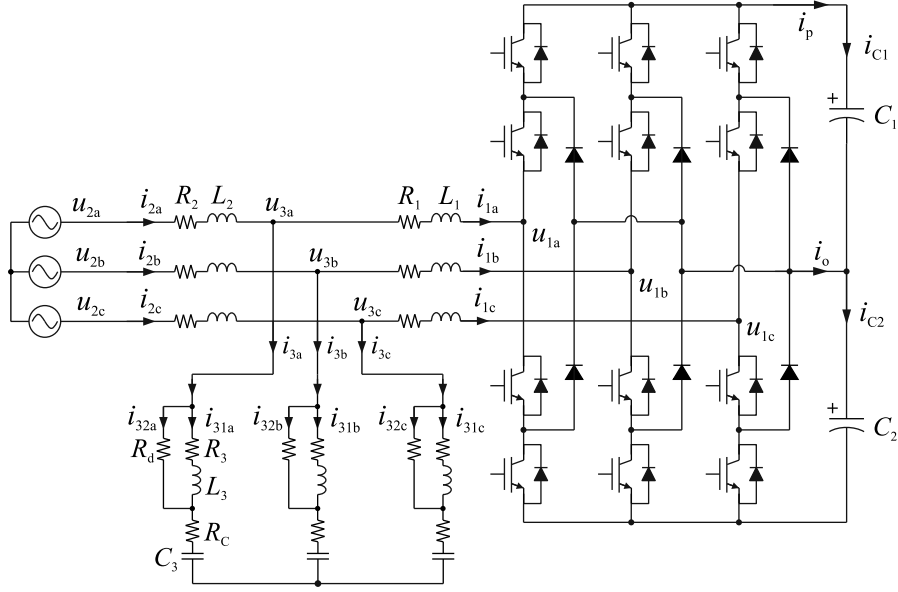


Fig. 3.1: Schematic of the STATCOM based on three-level NPC rectifier.

expressed in the stationary $\alpha\beta$ reference frame as follows:

$$L_1 \frac{d\vec{i}_1^{\alpha\beta}(t)}{dt} = \vec{u}_3^{\alpha\beta}(t) - \vec{u}_1^{\alpha\beta}(t) - R_1 \vec{i}_1^{\alpha\beta}(t) \quad (3.1)$$

$$L_2 \frac{d\vec{i}_2^{\alpha\beta}(t)}{dt} = \vec{u}_2^{\alpha\beta}(t) - \vec{u}_3^{\alpha\beta}(t) - R_2 \vec{i}_2^{\alpha\beta}(t) \quad (3.2)$$

$$L_3 \frac{d\vec{i}_{31}^{\alpha\beta}(t)}{dt} = R_d \left(\vec{i}_2^{\alpha\beta}(t) - \vec{i}_1^{\alpha\beta}(t) - \vec{i}_{31}^{\alpha\beta}(t) \right) - R_3 \vec{i}_{31}^{\alpha\beta}(t) \quad (3.3)$$

$$C_3 \frac{d\vec{u}_{C3}^{\alpha\beta}(t)}{dt} = \vec{i}_2^{\alpha\beta}(t) - \vec{i}_1^{\alpha\beta}(t) \quad (3.4)$$

$$\vec{u}_3^{\alpha\beta}(t) = \vec{u}_{C3}^{\alpha\beta}(t) + R_C (\vec{i}_2^{\alpha\beta}(t) - \vec{i}_1^{\alpha\beta}(t)) + R_d \left(\vec{i}_2^{\alpha\beta}(t) - \vec{i}_1^{\alpha\beta}(t) - \vec{i}_{31}^{\alpha\beta}(t) \right) \quad (3.5)$$

Next, (3.1)-(3.5) are transformed into the grid-voltage-oriented dq reference frame, which yields

$$L_1 \frac{d\vec{i}_1^{dq}(t)}{dt} = \vec{u}_3^{dq}(t) - \vec{u}_1^{dq}(t) - (R_1 + j\omega_r L_1) \vec{i}_1^{dq}(t) \quad (3.6)$$

$$L_2 \frac{d\vec{i}_2^{dq}(t)}{dt} = \vec{u}_2^{dq}(t) - \vec{u}_3^{dq}(t) - (R_2 + j\omega_r L_2) \vec{i}_2^{dq}(t) \quad (3.7)$$

$$L_3 \frac{d\vec{i}_{31}^{dq}(t)}{dt} = R_d \left(\vec{i}_2^{dq}(t) - \vec{i}_1^{dq}(t) - \vec{i}_{31}^{dq}(t) \right) - (R_3 + j\omega_r L_3) \vec{i}_{31}^{dq}(t) \quad (3.8)$$

$$C_3 \frac{d\vec{u}_{C3}^{dq}(t)}{dt} = \vec{i}_2^{dq}(t) - \vec{i}_1^{dq}(t) - j\omega_r C_3 \vec{u}_{C3}^{dq}(t) \quad (3.9)$$

$$\vec{u}_3^{dq}(t) = \vec{u}_{C3}^{dq}(t) + R_C (\vec{i}_2^{dq}(t) - \vec{i}_1^{dq}(t)) + R_d \left(\vec{i}_2^{dq}(t) - \vec{i}_1^{dq}(t) - \vec{i}_{31}^{dq}(t) \right) \quad (3.10)$$

where ω_r is the angular frequency of the synchronous reference frame.

From here on, the superscripts $\alpha\beta$ and dq of the vector variables are omitted and the notation refers to the dq reference frame if not specified otherwise. Also time

notations are omitted. By substituting (3.10) in (3.6)-(3.7), the coefficient matrices of the state-space equation given in (3.11)-(3.15) can be solved. The matrices **A**, **B**, **C**, and **D** are defined in (3.16) to (3.19).

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \quad (3.11)$$

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t) \quad (3.12)$$

$$\mathbf{x}(t) = [i_{1d} \ i_{1q} \ i_{2d} \ i_{2q} \ i_{31d} \ i_{31q} \ u_{C3d} \ u_{C3q}]^T \quad (3.13)$$

$$\mathbf{u}(t) = [u_{1d} \ u_{1q} \ u_{2d} \ u_{2q}]^T \quad (3.14)$$

$$\mathbf{y}(t) = [i_{1d} \ i_{1q} \ i_{2d} \ i_{2q} \ i_{31d} \ i_{31q} \ u_{C3d} \ u_{C3q}]^T \quad (3.15)$$

$$\mathbf{A} = \quad (3.16)$$

$$\begin{bmatrix} \frac{-R_1-R_d-R_C}{L_1} & \omega_r & \frac{R_d+R_C}{L_1} & 0 & \frac{-R_d}{L_1} & 0 & \frac{1}{L_1} & 0 \\ -\omega_r & \frac{-R_1-R_d-R_C}{L_1} & 0 & \frac{R_d+R_C}{L_1} & 0 & \frac{-R_d}{L_1} & 0 & \frac{1}{L_1} \\ \frac{R_d+R_C}{L_2} & 0 & \frac{-R_2-R_d-R_C}{L_2} & \omega_r & \frac{R_d}{L_2} & 0 & \frac{-1}{L_2} & 0 \\ 0 & \frac{R_d+R_C}{L_2} & -\omega_r & \frac{-R_2-R_d-R_C}{L_2} & 0 & \frac{R_d}{L_2} & 0 & \frac{-1}{L_2} \\ \frac{-R_d}{L_3} & 0 & \frac{R_d}{L_3} & 0 & \frac{-R_3-R_d}{L_3} & \omega_r & 0 & 0 \\ 0 & \frac{-R_d}{L_3} & 0 & \frac{R_d}{L_3} & -\omega_r & \frac{-R_3-R_d}{L_3} & 0 & 0 \\ \frac{-1}{C_3} & 0 & \frac{1}{C_3} & 0 & 0 & 0 & 0 & \omega_r \\ 0 & \frac{-1}{C_3} & 0 & \frac{1}{C_3} & 0 & 0 & -\omega_r & 0 \end{bmatrix}$$

$$\mathbf{B} = \begin{bmatrix} -\frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & -\frac{1}{L_1} & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_2} & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & \frac{1}{L_2} & 0 & 0 & 0 & 0 \end{bmatrix}^T \quad (3.17)$$

$$\mathbf{C} = \mathbf{I}_8 \quad (3.18)$$

$$\mathbf{D} = \mathbf{0}_{8 \times 4} \quad (3.19)$$

If the losses of the semiconductor bridge and the DC bus are neglected, the instantaneous power p through the AC terminals equals the power of the DC circuit:

$$\overbrace{\frac{3}{2}(u_{1d}i_{1d} + u_{1q}i_{1q})}^{=p} = u_{C1}i_p + u_{C2}(i_p + i_o) \quad (3.20)$$

When (3.20) is solved for i_p , the voltage derivatives of the DC capacitors can be expressed as

$$\frac{du_{C1}}{dt} = \frac{1}{C_1}i_p = \frac{1}{C_1} \frac{p - u_{C2}i_o}{u_{C1} + u_{C2}} \quad (3.21)$$

$$\frac{du_{C2}}{dt} = \frac{1}{C_2}(i_p + i_o) = \frac{1}{C_2} \frac{p + u_{C1}i_o}{u_{C1} + u_{C2}} \quad (3.22)$$

If the capacitor voltages are maintained in balance by the control, it can be assumed that $u_{C1} \approx u_{C2}$ and $i_o \approx 0$. When $C = C_1 = C_2$, the derivative of the full DC bus voltage can be expressed as

$$\frac{du_{DC}}{dt} = \frac{du_{C1}}{dt} + \frac{du_{C2}}{dt} \quad (3.23a)$$

$$= \frac{2}{C} \frac{p}{u_{DC}} \quad (3.23b)$$

$$= \frac{3}{C} \frac{(u_{1d}i_{1d} + u_{1q}i_{1q})}{u_{DC}} \quad (3.23c)$$

By averaging the converter voltage components in (3.23c) over a control sampling interval T_s , they can be expressed as

$$u_{1d}(t|t + T_s) \approx k \frac{u_{DC}}{2} d_d \quad (3.24)$$

$$u_{1q}(t|t + T_s) \approx k \frac{u_{DC}}{2} d_q \quad (3.25)$$

where d_d and d_q denote the duty cycles in the dq reference frame and k is the modulator constant. Within the linear modulation range d_d and d_q are subject to constraints

$$\sqrt{u_{1d}^2 + u_{1q}^2} \leq k \frac{u_{DC}}{2} \sqrt{d_d^2 + d_q^2} \quad (3.26)$$

$$\sqrt{d_d^2 + d_q^2} \leq 1 \quad (3.27)$$

where $k = \frac{2}{\sqrt{3}}$ in the case of space-vector modulation, because the linear modulation range limits to $\frac{u_{DC}}{\sqrt{3}}$. As a result, (3.23c) yields

$$\frac{du_{DC}}{dt} = \frac{3}{C} \frac{(kd_d \frac{u_{DC}}{2} i_{1d} + kd_q \frac{u_{DC}}{2} i_{1q})}{u_{DC}} \quad (3.28a)$$

$$= \frac{3k}{2C} (d_d i_{1d} + d_q i_{1q}) \quad (3.28b)$$

where (3.28b) is similar to the DC bus voltage derivative presented in [184] for a two-level three-phase rectifier.

The DC bus voltage derivative (3.28b) can be included in (3.13) to obtain the average model (3.29) where the submatrix \mathbf{A} is defined in (3.16). The model is linear but time-variant because of d_d and d_q present in the state matrix.

$$\frac{d}{dt} \begin{bmatrix} i_{1d} \\ i_{1q} \\ i_{2d} \\ i_{2q} \\ i_{31d} \\ i_{31q} \\ u_{C3d} \\ u_{C3q} \\ u_{DC} \end{bmatrix} = \left[\begin{array}{cccc|c} & & & & \frac{-k}{2L_1} d_d \\ & & & & \frac{-k}{2L_1} d_q \\ & & & & 0 \\ & & & & \vdots \\ \hline \frac{3k}{2C} d_d & \frac{3k}{2C} d_q & 0 & \dots & 0 \end{array} \right] \begin{bmatrix} i_{1d} \\ i_{1q} \\ i_{2d} \\ i_{2q} \\ i_{31d} \\ i_{31q} \\ u_{C3d} \\ u_{C3q} \\ u_{DC} \end{bmatrix} + \begin{bmatrix} \mathbf{B}(:, 3:4) \\ \mathbf{0} \end{bmatrix} \begin{bmatrix} u_{2d} \\ u_{2q} \end{bmatrix} \quad (3.29)$$

Eq. (3.29) could be linearised at a given steady-state operating point to make it useful for control design. Alternatively, it can be assumed that the DC bus capacitance is sufficiently large to keep u_{DC} approximately constant over a sampling interval T_s [184]. Then the response of the AC circuit during T_s becomes independent of u_{DC} and (3.29) simplifies to

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \quad (3.30)$$

$$\mathbf{x}(t) = [i_{1d} \ i_{1q} \ i_{2d} \ i_{2q} \ i_{31d} \ i_{31q} \ u_{C3d} \ u_{C3q}]^T \quad (3.31)$$

$$\mathbf{u}(t) = [u_{1d} \ u_{1q} \ u_{2d} \ u_{2q}]^T \quad (3.32)$$

where \mathbf{A} is (3.16), \mathbf{B} is (3.17), and the input variables u_{1d} and u_{1q} are

$$u_{1d} = k \frac{u_{\text{DC}}}{2} d_d \quad (3.33)$$

$$u_{1q} = k \frac{u_{\text{DC}}}{2} d_q \quad (3.34)$$

The reduced model (3.30) is linear and time-invariant and, therefore, can be used as such to analyse the current control loop. However, the model reduction omits the interaction between the AC and the DC circuits. Therefore, a small-signal model including the DC bus voltage dynamics should be derived to analyse the DC bus voltage control loop.

3.3 Modelling of the filter inductors' frequency characteristics

In the previous section, the filter inductors of the STATCOM under study were modelled with series RL equivalent circuits. Next, the RL equivalents are replaced with third-order Foster equivalent circuits, as illustrated in Fig. 3.2, which provide more accurate approximation of the filter inductor frequency characteristics. The development of Foster equivalent circuits and their parameters are presented in Appendix C. A linear, time-invariant average model of the STATCOM is derived and it will be used in Chapter 5 to study the effects of inductor frequency characteristics on the grid current control loop.

Firstly, the expressions for the currents \vec{i}_1 , \vec{i}_2 , and \vec{i}_{31} are derived. Based on Fig. 3.2, the voltages across the Foster equivalent circuits can be expressed as

$$\vec{u}_{L1} = \vec{u}_3 - \vec{u}_1 = R_{10}\vec{i}_1 + \sum_{x=1}^3 R_{1x}(\vec{i}_1 - \vec{i}_{L1x}) \quad (3.35)$$

$$\vec{u}_{L2} = \vec{u}_2 - \vec{u}_3 = R_{20}\vec{i}_2 + \sum_{x=1}^3 R_{2x}(\vec{i}_2 - \vec{i}_{L2x}) \quad (3.36)$$

$$\vec{u}_{L3} = R_{30}\vec{i}_{31} + \sum_{x=1}^3 R_{3x}(\vec{i}_{31} - \vec{i}_{L3x}) \quad (3.37)$$

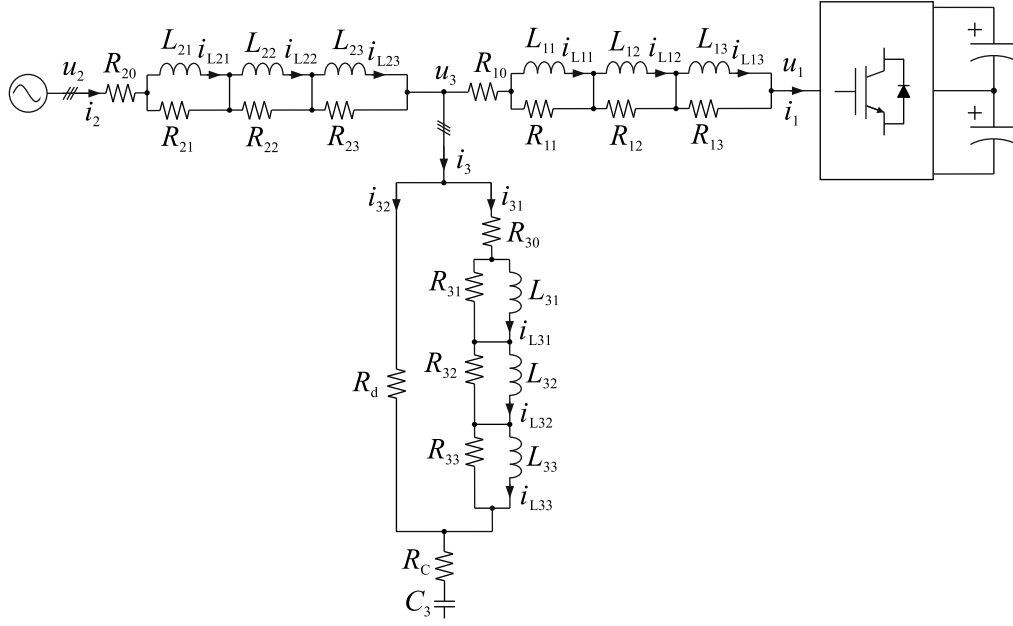


Fig. 3.2: Schematic of the STATCOM when the filter inductors are approximated with third-order Foster equivalent circuits.

The currents \vec{i}_1 and \vec{i}_2 can be solved from (3.35) and (3.36), respectively, which yield

$$\vec{i}_1 = \frac{1}{r_{L1}} \left(\vec{u}_3 - \vec{u}_1 + \sum_{x=1}^3 R_{1x} \vec{i}_{L1x} \right) \quad (3.38)$$

$$\vec{i}_2 = \frac{1}{r_{L2}} \left(\vec{u}_2 - \vec{u}_3 + \sum_{x=1}^3 R_{2x} \vec{i}_{L2x} \right) \quad (3.39)$$

where r_{L1} and r_{L2} are

$$r_{L1} = R_{10} + R_{11} + R_{12} + R_{13} \quad (3.40)$$

$$r_{L2} = R_{20} + R_{21} + R_{22} + R_{23} \quad (3.41)$$

The current \vec{i}_{31} can be solved from (3.37) using the Kirchhoff's law of current, as follows

$$\vec{i}_{31} = \vec{i}_2 - \vec{i}_1 - \vec{i}_{32} \quad (3.42a)$$

$$= \vec{i}_2 - \vec{i}_1 - \frac{\vec{u}_{L3}}{R_d} \quad (3.42b)$$

$$= A_{i31/i3} \left(\vec{i}_2 - \vec{i}_1 + \frac{1}{R_d} \sum_{x=1}^3 R_{3x} \vec{i}_{L3x} \right) \quad (3.42c)$$

where $A_{i31/i3}$ is

$$A_{i31/i3} = \frac{R_d}{R_d + r_{L3}} \quad (3.43)$$

and r_{L3} in (3.43) is

$$r_{L3} = R_{30} + R_{31} + R_{32} + R_{33} \quad (3.44)$$

The voltage \vec{u}_3 present in (3.38) and (3.39) can be solved when (3.38), (3.39), and (3.42c) are substituted in (3.10), which yields

$$\begin{aligned}\vec{u}_3 = & \frac{r_{\text{tot}}}{r_{\text{sb}}} \vec{u}_{C3} + \frac{r_{\text{tot}}}{r_{L1}} \vec{u}_1 + \frac{r_{\text{tot}}}{r_{L2}} \vec{u}_2 - \frac{r_{\text{tot}}}{r_{L1}} \sum_{x=1}^3 R_{1x} \vec{i}_{L1x} \\ & + \frac{r_{\text{tot}}}{r_{L2}} \sum_{x=1}^3 R_{2x} \vec{i}_{L2x} - \frac{A_{i31/i3} r_{\text{tot}}}{r_{\text{sb}}} \sum_{x=1}^3 R_{3x} \vec{i}_{L3x}\end{aligned}\quad (3.45)$$

where r_{sb} is the equivalent resistance of the filter shunt branch when the inductances L_{3x} are considered open circuits ($f \rightarrow \infty$), and r_{tot} is the equivalent resistance of the short-circuited LCL filter equivalent circuit when the inductances L_{1x} , L_{2x} , L_{3x} are considered open circuits. The resistances r_{sb} and r_{tot} are defined as follows:

$$r_{\text{sb}} = R_C + r_{L3} || R_d \quad (3.46)$$

$$r_{\text{tot}} = (r_{L1} || r_{L2}) || r_{\text{sb}} \quad (3.47)$$

Finally, the currents \vec{i}_1 , \vec{i}_2 , and \vec{i}_{31} can be solved by combining (3.38), (3.39), (3.42c), and (3.45). They can be expressed as follows:

$$\begin{aligned}\vec{i}_1 = & \frac{r_{L1} - r_{\text{tot}}}{r_{L1}^2} \sum_{x=1}^3 R_{1x} \vec{i}_{L1x} + \frac{r_{\text{tot}}}{r_{L1} r_{L2}} \sum_{x=1}^3 R_{2x} \vec{i}_{L2x} \\ & - \frac{A_{i31/i3} r_{\text{tot}}}{r_{L1} r_{\text{sb}}} \sum_{x=1}^3 R_{3x} \vec{i}_{L3x} + \frac{r_{\text{tot}}}{r_{L1} r_{\text{sb}}} \vec{u}_{C3} + \frac{r_{\text{tot}} - r_{L1}}{r_{L1}^2} \vec{u}_1 + \frac{r_{\text{tot}}}{r_{L1} r_{L2}} \vec{u}_2\end{aligned}\quad (3.48)$$

$$\begin{aligned}\vec{i}_2 = & \frac{r_{\text{tot}}}{r_{L1} r_{L2}} \sum_{x=1}^3 R_{1x} \vec{i}_{L1x} + \frac{r_{L2} - r_{\text{tot}}}{r_{L2}^2} \sum_{x=1}^3 R_{2x} \vec{i}_{L2x} + \frac{A_{i31/i3} r_{\text{tot}}}{r_{L2} r_{\text{sb}}} \sum_{x=1}^3 R_{3x} \vec{i}_{L3x} \\ & + \frac{-r_{\text{tot}}}{r_{L2} r_{\text{sb}}} \vec{u}_{C3} + \frac{-r_{\text{tot}}}{r_{L1} r_{L2}} \vec{u}_1 + \frac{r_{L2} - r_{\text{tot}}}{r_{L2}^2} \vec{u}_2\end{aligned}\quad (3.49)$$

$$\begin{aligned}\vec{i}_{31} = & \frac{-A_{i31/i3} r_{\text{tot}}}{r_{L1} r_{\text{sb}}} \sum_{x=1}^3 R_{1x} \vec{i}_{L1x} + \frac{A_{i31/i3} r_{\text{tot}}}{r_{L2} r_{\text{sb}}} \sum_{x=1}^3 R_{2x} \vec{i}_{L2x} \\ & + \left(\frac{1}{R_d + r_{L3}} + \frac{A_{i31/i3}^2 r_{\text{tot}}}{r_{L2} r_{\text{sb}}} + \frac{A_{i31/i3}^2 r_{\text{tot}}}{r_{L1} r_{\text{sb}}} \right) \sum_{x=1}^3 R_{3x} \vec{i}_{L3x} \\ & + \left(-\frac{A_{i31/i3} r_{\text{tot}}}{r_{L2} r_{\text{sb}}} - \frac{A_{i31/i3} r_{\text{tot}}}{r_{L1} r_{\text{sb}}} \right) \vec{u}_{C3} + \frac{A_{i31/i3} r_{\text{tot}}}{r_{L1} r_{\text{sb}}} \vec{u}_1 + \frac{A_{i31/i3} r_{\text{tot}}}{r_{L2} r_{\text{sb}}} \vec{u}_2\end{aligned}\quad (3.50)$$

Next, the state-space equation modelling the circuit depicted in Fig. 3.2 is developed. Firstly, a voltage equation is developed for each cell of the three Foster equivalent circuits and the inductor current derivatives are solved. Also the derivative of the filter capacitor C_3 voltage is solved. The aforementioned derivatives can

be expressed as follows:

$$\frac{d\vec{i}_{L1x}}{dt} = \frac{u_{L1x}}{L_{1x}} = \frac{R_{1x}}{L_{1x}}(\vec{i}_1 - \vec{i}_{L1x}) - j\omega_r \vec{i}_{L1x} \quad (3.51)$$

$$\frac{d\vec{i}_{L2x}}{dt} = \frac{u_{L2x}}{L_{2x}} = \frac{R_{2x}}{L_{2x}}(\vec{i}_2 - \vec{i}_{L2x}) - j\omega_r \vec{i}_{L2x} \quad (3.52)$$

$$\frac{d\vec{i}_{L3x}}{dt} = \frac{u_{L3x}}{L_{3x}} = \frac{R_{3x}}{L_{3x}}(\vec{i}_{31} - \vec{i}_{L3x}) - j\omega_r \vec{i}_{L3x} \quad (3.53)$$

$$\frac{d\vec{u}_{C3}}{dt} = \frac{1}{C_3}(\vec{i}_2 - \vec{i}_1) - j\omega_r \vec{u}_{C3} \quad (3.54)$$

Finally, the currents \vec{i}_1 , \vec{i}_2 , and \vec{i}_{31} from (3.48)-(3.50) can be substituted in (3.51)-(3.54) to derive the following state-space representation for the circuit

$$\dot{\mathbf{x}}(t) = \begin{bmatrix} \mathbf{A}_1^1 & \dots & \mathbf{A}_1^4 \\ \vdots & \ddots & \vdots \\ \mathbf{A}_4^1 & \dots & \mathbf{A}_4^4 \end{bmatrix} \mathbf{x}(t) + \begin{bmatrix} \mathbf{B}_1 \\ \vdots \\ \mathbf{B}_4 \end{bmatrix} \mathbf{u}(t) \quad (3.55)$$

where the state and the input vector are defined as follows

$$\mathbf{x}(t) = [\mathbf{i}_{L1} \quad \mathbf{i}_{L2} \quad \mathbf{i}_{L3} \quad \mathbf{u}_{C3}]^T \quad (3.56)$$

$$\mathbf{i}_{L1} = [i_{L11d} \quad i_{L11q} \quad i_{L12d} \quad i_{L12q} \quad i_{L13d} \quad i_{L13q}] \quad (3.57)$$

$$\mathbf{i}_{L2} = [i_{L21d} \quad i_{L21q} \quad i_{L22d} \quad i_{L22q} \quad i_{L23d} \quad i_{L23q}] \quad (3.58)$$

$$\mathbf{i}_{L3} = [i_{L31d} \quad i_{L31q} \quad i_{L32d} \quad i_{L32q} \quad i_{L33d} \quad i_{L33q}] \quad (3.59)$$

$$\mathbf{u}_{C3} = [u_{C3d} \quad u_{C3q}] \quad (3.60)$$

$$\mathbf{u}(t) = [u_{1d} \quad u_{1q} \quad u_{2d} \quad u_{2q}]^T \quad (3.61)$$

The state matrix \mathbf{A} in (3.55) is of size 20×20 and is partitioned into 16 submatrices $\mathbf{A}_i^j \{i, j \in 1, 2, 3, 4\}$. The matrices $\mathbf{A}_i^j \{i, j \in 1, 2, 3\}$ are of size 6×6 and include the coefficients linking the inductor currents to each other. The 6×2 matrices $\mathbf{A}_i^4 \{i \in 1, 2, 3\}$ link the filter capacitor voltages to the inductor currents. The matrices $\mathbf{A}_4^j \{j \in 1, 2, 3\}$ are of size 2×6 and describe the portion of filter capacitor voltages that is dependent on the inductor currents. The 2×2 matrix \mathbf{A}_4^4 describes the cross-coupling between u_{C3d} and u_{C3q} . The input matrix \mathbf{B} is of size 20×4 .

3.4 Inclusion of the grid impedance

In Sections 3.2 and 3.3, the grid was modelled with three ideal AC voltage sources with zero internal impedances. In practice, the grid impedance is non-zero and it varies. The grid impedance variation changes the resonant frequency of the *LCL* filter, which can cause stability issues [165]. Additionally, the STATCOM current produces a voltage drop across the grid impedances, which changes the voltage at its connection point. As a result, the STATCOM will interact with its own control action, because the voltage at the connection point is measured and feedforwarded

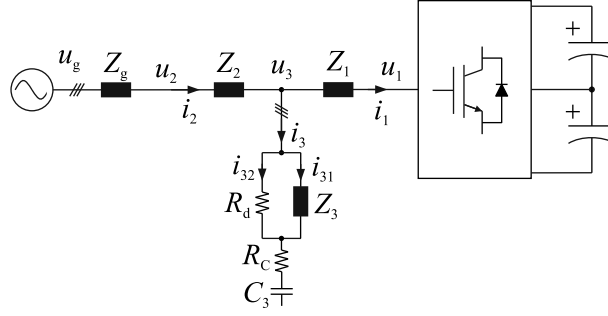


Fig. 3.3: Equivalent circuit including the grid impedances.

to the grid current controller. Next, to study the aforementioned phenomena, the grid impedance is included in the average models presented in the two previous sections.

In Fig. 3.3, the grid is modelled with ideal voltage sources u_g behind grid impedances $Z_g = R_g + j\omega_r L_g$. The voltage at the STATCOM's connection point is u_2 . The impedances Z_1, Z_2, Z_3 denote the filter inductors. Firstly, let us consider the case when the filter inductors are modelled with series RL elements, similarly as in Section 3.2. Based on Fig. 3.3, the grid current derivative can be expressed as

$$\frac{d\vec{i}_2}{dt} = \frac{1}{L_g}(\vec{u}_g - \vec{u}_2) - \frac{1}{L_g}(R_g + j\omega_r L_g)\vec{i}_2 \quad (3.62a)$$

$$= \frac{1}{L_2}(\vec{u}_2 - \vec{u}_3) - \frac{1}{L_2}(R_2 + j\omega_r L_2)\vec{i}_2 \quad (3.62b)$$

The voltage \vec{u}_2 can be solved from (3.62a) and (3.62b), as follows, when \vec{u}_3 is substituted with (3.10):

$$\begin{aligned} \vec{u}_2 = & -\frac{(R_C + R_d)L_g}{L_g + L_2}\vec{i}_1 + \frac{(R_C + R_d + R_2)L_g - R_g L_2}{L_g + L_2}\vec{i}_2 - \frac{R_d L_g}{L_g + L_2}\vec{i}_{31} \\ & + \frac{L_g}{L_g + L_2}\vec{u}_{C3} + \frac{L_2}{L_g + L_2}\vec{u}_g \end{aligned} \quad (3.63)$$

After that, (3.63) is substituted in (3.62b) and the grid current derivative is rewritten as follows

$$\begin{aligned} \frac{d\vec{i}_2}{dt} = & \frac{R_C + R_d}{L_g + L_2}\vec{i}_1 - \left(\frac{R_g + R_2 + R_C + R_d}{L_g + L_2} + j\omega_r \right)\vec{i}_2 + \frac{R_d}{L_g + L_2}\vec{i}_{31} \\ & - \frac{1}{L_g + L_2}\vec{u}_{C3} + \frac{1}{L_g + L_2}\vec{u}_g \end{aligned} \quad (3.64)$$

Finally, the grid impedance is included in the state-space equation (3.30) by substituting the derivative of \vec{i}_2 with (3.64). In addition, the voltage \vec{u}_2 in the input vector $\mathbf{u}(t)$ is replaced with the stiff grid voltage \vec{u}_g . The resulting state-space equation is of form

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \quad (3.65)$$

$$\mathbf{x}(t) = [i_{1d} \ i_{1q} \ i_{2d} \ i_{2q} \ i_{31d} \ i_{31q} \ u_{C3d} \ u_{C3q}]^T \quad (3.66)$$

$$\mathbf{u}(t) = [u_{1d} \ u_{1q} \ u_{gd} \ u_{gq}]^T \quad (3.67)$$

Next, the grid impedance is included in the average model presented in Section 3.3. Firstly, the shunt branch voltage \vec{u}_3 of the LCL filter is re-expressed using (3.10), (3.48), and (3.50) as follows

$$\begin{aligned}\vec{u}_3 &= \vec{u}_{C3} - (R_C + R_d)\vec{i}_1 + (R_C + R_d)\vec{i}_2 - R_d\vec{i}_{31} \\ &= -\frac{r_{i3}}{r_{L1} + r_{i3}} \sum_{x=1}^3 R_{1x}\vec{i}_{L1x} + \frac{r_{L1}r_{i3}}{r_{L1} + r_{i3}}\vec{i}_2 \\ &\quad - \frac{r_{L1}A_{i31/i3}}{r_{L1} + r_{i3}} \sum_{x=1}^3 R_{3x}\vec{i}_{L31x} + \frac{r_{L1}}{r_{L1} + r_{i3}}\vec{u}_{C3} + \frac{r_{i3}}{r_{L1} + r_{i3}}\vec{u}_1\end{aligned}\quad (3.68)$$

where the coefficients r_{L1} and $A_{i31/i3}$ are defined in (3.40) and (3.43), respectively, and the equivalent resistance r_{i3} along the i_3 path, when $f \rightarrow \infty$, is

$$r_{i3} = R_C + R_d(1 - A_{i31/i3}) \quad (3.69)$$

After that, (3.68) is substituted in (3.48), (3.50), and (3.36) to solve \vec{i}_1 , \vec{i}_{31} , and \vec{u}_2 as follows

$$\begin{aligned}\vec{i}_1 &= \frac{1}{r_{L1}} \left(\vec{u}_3 - \vec{u}_1 + \sum_{x=1}^3 R_{1x}\vec{i}_{L1x} \right) \\ &= \frac{1}{r_{L1} + r_{i3}} \sum_{x=1}^3 R_{1x}\vec{i}_{L1x} - \frac{A_{i31/i3}}{r_{L1} + r_{i3}} \sum_{x=1}^3 R_{3x}\vec{i}_{L31x} + \frac{1}{r_{L1} + r_{i3}}\vec{u}_{C3} \\ &\quad + \frac{r_{i3}}{r_{L1} + r_{i3}}\vec{i}_2 - \frac{1}{r_{L1} + r_{i3}}\vec{u}_1\end{aligned}\quad (3.70)$$

$$\begin{aligned}\vec{i}_{31} &= -\frac{A_{i31/i3}}{r_{L1} + r_{i3}} \sum_{x=1}^3 R_{1x}\vec{i}_{L1x} + \left(\frac{A_{i31/i3}^2}{r_{L1} + r_{i3}} + \frac{A_{i31/i3}}{R_d} \right) \sum_{x=1}^3 R_{3x}\vec{i}_{L31x} \\ &\quad - \frac{A_{i31/i3}}{r_{L1} + r_{i3}}\vec{u}_{C3} + \frac{r_{L1}A_{i31/i3}}{r_{L1} + r_{i3}}\vec{i}_2 + \frac{A_{i31/i3}}{r_{L1} + r_{i3}}\vec{u}_1\end{aligned}\quad (3.71)$$

$$\begin{aligned}\vec{u}_2 &= -\frac{r_{i3}}{r_{L1} + r_{i3}} \sum_{x=1}^3 R_{1x}\vec{i}_{L1x} - \sum_{x=1}^3 R_{2x}\vec{i}_{L2x} - \frac{r_{L1}A_{i31/i3}}{r_{L1} + r_{i3}} \sum_{x=1}^3 R_{3x}\vec{i}_{L31x} \\ &\quad + \frac{r_{L1}}{r_{L1} + r_{i3}}\vec{u}_{C3} + \frac{r_{L1}r_{L2} + r_{i3}(r_{L1} + r_{L2})}{r_{L1} + r_{i3}}\vec{i}_2 + \frac{r_{i3}}{r_{L1} + r_{i3}}\vec{u}_1\end{aligned}\quad (3.72)$$

In addition, the grid current derivative is expressed based on Fig. 3.3 as follows

$$\frac{d\vec{i}_2}{dt} = \frac{1}{L_g}(\vec{u}_g - \vec{u}_2) - \frac{1}{L_g}(R_g + j\omega_r L_g)\vec{i}_2 \quad (3.73)$$

The resulting linear and time-invariant average model is

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) \quad (3.74)$$

$$\mathbf{x}(t) = [\mathbf{i}_{L1} \quad \mathbf{i}_{L2} \quad \mathbf{i}_{L3} \quad \mathbf{u}_{C3} \quad \mathbf{i}_2]^T \quad (3.75)$$

$$\mathbf{i}_{L1} = [i_{L11d} \quad i_{L11q} \quad i_{L12d} \quad i_{L12q} \quad i_{L13d} \quad i_{L13q}] \quad (3.76)$$

$$\mathbf{i}_{L2} = [i_{L21d} \quad i_{L21q} \quad i_{L22d} \quad i_{L22q} \quad i_{L23d} \quad i_{L23q}] \quad (3.77)$$

$$\mathbf{i}_{L3} = [i_{L31d} \quad i_{L31q} \quad i_{L32d} \quad i_{L32q} \quad i_{L33d} \quad i_{L33q}] \quad (3.78)$$

$$\mathbf{u}_{C3} = [u_{C3d} \quad u_{C3q}] \quad (3.79)$$

$$\mathbf{i}_2 = [i_{2d} \quad i_{2q}] \quad (3.80)$$

$$\mathbf{u}(t) = [u_{1d} \quad u_{1q} \quad u_{gd} \quad u_{gq}]^T \quad (3.81)$$

The coefficient matrices \mathbf{A} and \mathbf{B} can be derived by substituting (3.70)-(3.72) in (3.51)-(3.54) and solving the derivatives $\frac{d}{dt}\vec{i}_{L1x}$, $\frac{d}{dt}\vec{i}_{L2x}$, $\frac{d}{dt}\vec{i}_{L3x}$, and $\frac{d}{dt}\vec{u}_{C3}$. The grid current components i_{2d} and i_{2q} are introduced in the state vector as new state variables. Their derivatives can be solved from (3.73) when \vec{u}_2 is substituted with (3.72).

3.5 Conclusions

This chapter presented the schematic of the STATCOM under study and, to assess the characteristics of the grid current control loop, dynamic models were developed for it. In the first model, the filter inductors were modelled with series RL elements. After that, the model was extended by approximating the filter inductors' frequency characteristics with third-order Foster equivalent circuits. Finally, the effect of grid impedance was included in the two first models.

Chapter 4

Modulation algorithm

4.1 Introduction

This chapter presents the functions and the program flow of the implemented modulation algorithm. Section 4.2 describes the computation of reference vector projections and limiting of reference magnitude. After that, the duty cycles solution and the switching sequence generation are discussed in Section 4.3 and the capacitor voltage balancing algorithm is presented in Section 4.4. Then, the switching waveforms and the arrangement of NTV sequences of consecutive switching periods are studied in Section 4.5. A nonlinearity compensation function reducing the effects of dead-times and on-state semiconductor voltage drops is presented in Section 4.6. Finally, the modulator program flow is reviewed in Section 4.7 and the conclusions are drawn in Section 4.8.

4.2 Solution of vector projections

At the start of the modulator update routine, the reference vector \vec{u}^* is rotated to the first sextant of the voltage hexagon to solve the vector projections needed in the duty cycles computation. As shown in Appendix A, an arbitrary $\alpha\beta$ plane vector $\|\vec{x}\|e^{j\theta} = x_\alpha + jx_\beta$ can be rotated 60° clockwise as follows

$$\|\vec{x}\|e^{j(\theta-\frac{\pi}{3})} = \frac{1}{2}(x_\alpha + \sqrt{3}x_\beta) + j\frac{1}{2}(-\sqrt{3}x_\alpha + x_\beta) \quad (4.1)$$

The rotation of \vec{u}^* to Sector 1 is implemented by repeating (4.1) until the following constraints are fulfilled

$$u_\alpha^* \geq 0 \ \& \ u_\beta^* \geq 0 \ \& \ u_\beta^* \leq \sqrt{3}u_\alpha^* \quad (4.2)$$

The original sector of \vec{u}^* can be determined from the number of the rotations applied.

After the rotation, \vec{u}^* is normalised and transformed into gh coordinates to obtain the projections m_1 and m_2 on the Sector 1 boundaries:

$$\begin{bmatrix} m_1 \\ m_2 \end{bmatrix} = \frac{1}{\frac{1}{3}u_{DC}} \begin{bmatrix} 1 & -\frac{1}{\sqrt{3}} \\ 0 & \frac{2}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} u_\alpha^* \\ u_\beta^* \end{bmatrix} \quad (4.3)$$

If $m_1 + m_2 > 2$, the reference extends outside the voltage hexagon and the SVL method discussed in Section 2.3.5 is applied to scale it to the hexagon boundary. The SVL method is implemented in the normalised gh coordinates as follows

$$m_1' = m_1 \frac{2}{m_1 + m_2} \quad (4.4)$$

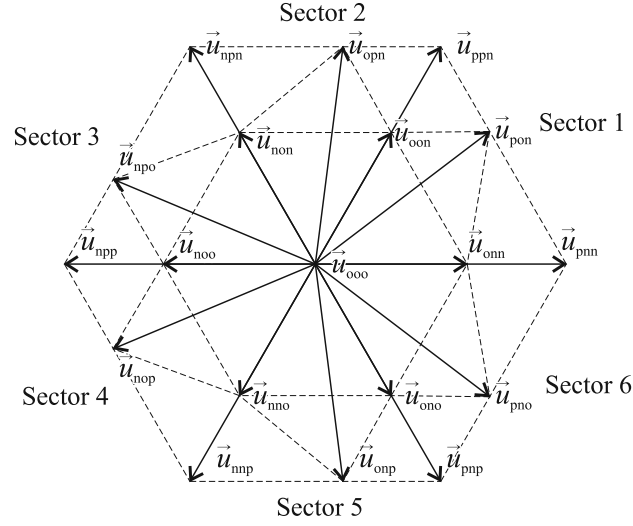
$$m_2' = m_2 \frac{2}{m_1 + m_2} \quad (4.5)$$

where m_1' and m_2' denote the scaled components.

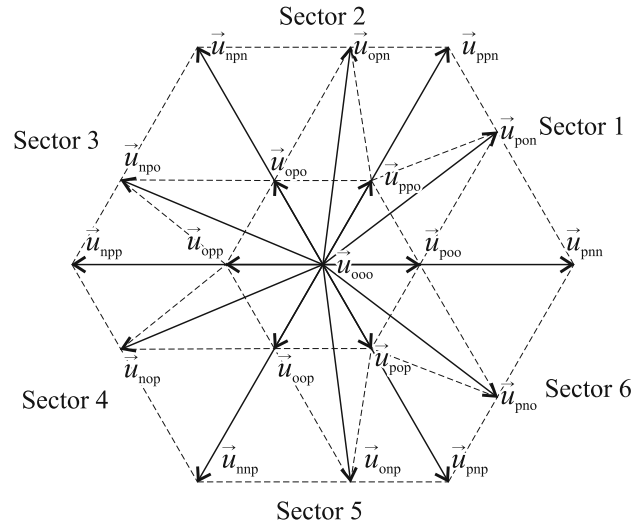
4.3 Duty cycles solution and switching sequence generation

The modulation is based on the DPWM patterns reviewed in Section 2.3.2. The patterns under study can be developed by using suitable combinations of the NTVs illustrated in Figs. 4.1(a) and 4.1(b) which assume unbalanced capacitor voltages ($u_{C1} < u_{C2}$). Fig. 4.1(a) is obtained by omitting all the positive and Fig. 4.1(b) by omitting all the negative short vectors. It can be seen that the both figures consist of two type of main sector geometries when $u_{C1} \neq u_{C2}$. By taking advantage of the main sector symmetries, the duty cycles of all the odd sectors can be solved using the geometry of Sector 1. Also, the duty cycles of all the even sectors can be solved using the geometry of Sector 2. As a result, four different main sector geometries need to be considered to implement the modulator. Moreover, all the subsector geometry variations shown in Figs. 4.1(a) and 4.1(b) need to be considered.

Fig. 4.2 highlights the geometric alternatives of Sector 1 and Sector 2. The duty cycles of the NTV combinations can be solved using the theory reviewed in Section 2.3.4 and are summarised in Table 4.1 for Sector 1, and in Table 4.2 for Sector 2. The tables also indicate how the location (subsector) of the reference is identified using the normalised vector projections m_1 , m_2 , and m_{12} , and the normalised short vector lengths γ_p and γ_n . The duty cycles and switch combinations for Sector 3 and Sector 5 are found by applying the switch combination transformations reviewed in Appendix B on Table 4.1. Similarly, the duty cycles and switch combinations of Sector 4 and Sector 6 are found by using the transformations on Table 4.2.



(a)



(b)

Fig. 4.1: The effect of neutral-point voltage imbalance on the voltage vectors when $u_{C2} > u_{C1}$. Three-vector combinations obtained by using (a) only the negative short vectors and (b) only the positive short vectors.

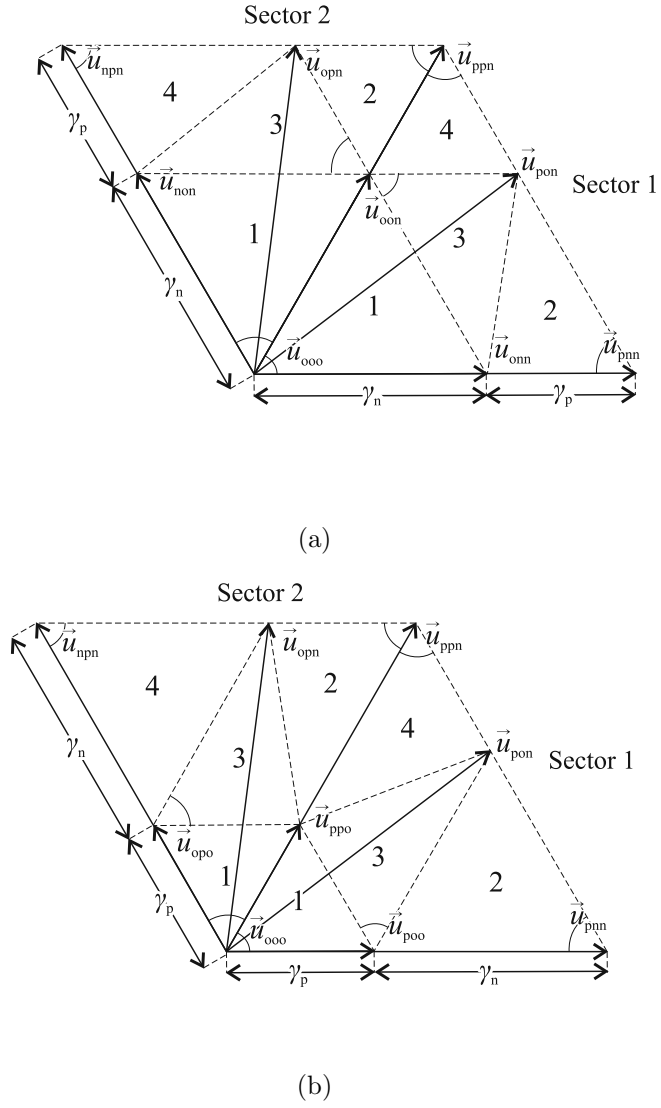


Fig. 4.2: Geometries of Sector 1 and Sector 2 when $u_{C1} < u_{C2}$ and (a) only the negative short vectors are used, (b) only the positive short vectors are used.

Table 4.1: Duty cycles of the three-vector combinations in Sector 1

NTV combinations based on negative short vectors (Fig. 4.2(a))					
Subsector	Condition	Duty cycles			
1	$m_1 + m_2 \leq \gamma_n$	$d_{onn} = \frac{m_1}{\gamma_n}$	$d_{oon} = \frac{m_2}{\gamma_n}$	$d_{ooo} = 1 - d_{onn} - d_{oon}$	
2	$1 - \frac{m_{12}}{\gamma_p} - \frac{m_2}{\gamma_n} \geq 0$	$d_{onn} = \frac{m_{12}}{\gamma_p}$	$d_{pon} = \frac{m_2}{\gamma_n}$	$d_{pnn} = 1 - d_{onn} - d_{pon}$	
4	$m_2 \geq \gamma_n$	$d_{oon} = \frac{m_{12}}{\gamma_p}$	$d_{pon} = \frac{m_1}{\gamma_p}$	$d_{ppn} = 1 - d_{oon} - d_{pon}$	
3	Otherwise	$d_{onn} = 1 - \frac{m_2}{\gamma_n}$	$d_{pon} = 1 - \frac{m_{12}}{\gamma_p}$	$d_{oon} = 1 - d_{onn} - d_{pon}$	

NTV combinations based on positive short vectors (Fig. 4.2(b))					
Subsector	Condition	Duty cycles			
1	$m_1 + m_2 \leq \gamma_p$	$d_{poo} = \frac{m_1}{\gamma_p}$	$d_{ppo} = \frac{m_2}{\gamma_p}$	$d_{ooo} = 1 - d_{poo} - d_{ppo}$	
2	$m_1 \geq \gamma_n$	$d_{poo} = \frac{m_{12}}{\gamma_n}$	$d_{pon} = \frac{m_2}{\gamma_n}$	$d_{pnn} = 1 - d_{poo} - d_{pon}$	
4	$1 - \frac{m_{12}}{\gamma_n} - \frac{m_1}{\gamma_p} \geq 0$	$d_{ppo} = \frac{m_{12}}{\gamma_n}$	$d_{pon} = \frac{m_1}{\gamma_p}$	$d_{ppn} = 1 - d_{ppo} - d_{pon}$	
3	Otherwise	$d_{ppo} = 1 - \frac{m_1}{\gamma_p}$	$d_{pon} = 1 - \frac{m_{12}}{\gamma_n}$	$d_{poo} = 1 - d_{ppo} - d_{pon}$	

Table 4.2: Duty cycles of the three-vector combinations in Sector 2

NTV combinations based on negative short vectors (Fig. 4.2(a))					
Subsector	Condition	Duty cycles			
1	$m_1 + m_2 \leq \gamma_n$	$d_{non} = \frac{m_2}{\gamma_n}$	$d_{oon} = \frac{m_1}{\gamma_n}$	$d_{ooo} = 1 - d_{non} - d_{oon}$	
2	$m_1 \geq \gamma_n$	$d_{oon} = \frac{m_{12}}{\gamma_p}$	$d_{opn} = \frac{m_2}{\gamma_p}$	$d_{ppn} = 1 - d_{oon} - d_{opn}$	
4	$1 - \frac{m_{12}}{\gamma_n} - \frac{m_2}{\gamma_p} \geq 0$	$d_{non} = \frac{m_{12}}{\gamma_p}$	$d_{opn} = \frac{m_1}{\gamma_n}$	$d_{npn} = 1 - d_{non} - d_{opn}$	
3	Otherwise	$d_{non} = 1 - \frac{m_1}{\gamma_n}$	$d_{opn} = 1 - \frac{m_{12}}{\gamma_p}$	$d_{oon} = 1 - d_{non} - d_{opn}$	

NTV combinations based on positive short vectors (Fig. 4.2(b))					
Subsector	Condition	Duty cycles			
1	$m_1 + m_2 \leq \gamma_p$	$d_{opo} = \frac{m_2}{\gamma_p}$	$d_{ppo} = \frac{m_1}{\gamma_p}$	$d_{ooo} = 1 - d_{opo} - d_{ppo}$	
2	$1 - \frac{m_{12}}{\gamma_p} - \frac{m_2}{\gamma_n} \geq 0$	$d_{ppo} = \frac{m_{12}}{\gamma_n}$	$d_{opn} = \frac{m_2}{\gamma_p}$	$d_{ppn} = 1 - d_{ppo} - d_{opn}$	
4	$m_2 \geq \gamma_n$	$d_{opo} = \frac{m_{12}}{\gamma_n}$	$d_{opn} = \frac{m_1}{\gamma_n}$	$d_{ppn} = 1 - d_{opo} - d_{opn}$	
3	Otherwise	$d_{ppo} = 1 - \frac{m_2}{\gamma_p}$	$d_{opn} = 1 - \frac{m_{12}}{\gamma_n}$	$d_{poo} = 1 - d_{ppo} - d_{opn}$	

4.4 Balancing of the DC bus capacitor voltages

The DC bus voltage balance is controlled using the redundant short vectors. The balancing algorithm is implemented by changing between the DPWM patterns discussed in Section 2.3.2 so that the voltage difference between the capacitors is forced towards zero. This way the capacitor voltages can be balanced on the average-basis, but the low frequency neutral-point voltage oscillation cannot be fully suppressed [133]. Furthermore, at high modulation ratios, the application times of the redundant vectors become short, which deteriorates the control over the voltage balance. The voltage balancing limits of the applied method have not been determined within the scope of this thesis.

To implement the balancing control algorithm, the voltage hexagon is divided in six 60° regions that are centred on the short vectors, as illustrated in Fig. 4.3. The selection between the redundant short vectors is made based on the capacitor voltage difference, and the polarity of the DC bus midpoint current i_o resulting from the applied short vectors. The short vector selection is updated every 30° which enables to follow the DPWM patterns depicted in Fig. 2.7.

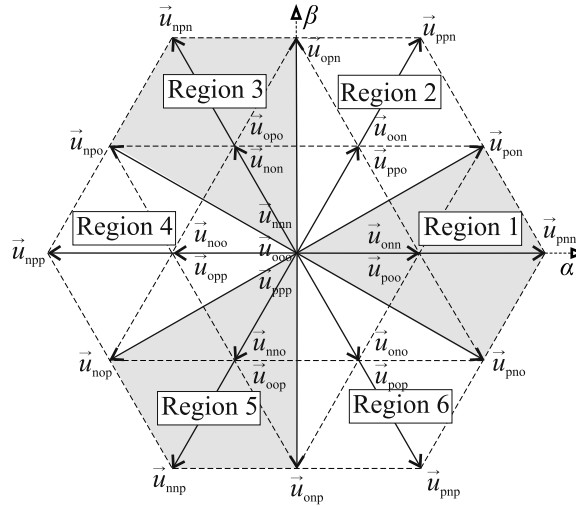


Fig. 4.3: The division of the voltage hexagon in six sectors centered on the short vectors.

The midpoint current is solved based on the applied switch combination and the measured phase currents, as described in Table 4.3 (see also Table 2.2 in Section 2.2). The current polarity towards the rectifier is positive, which yields (4.6) where $k \in \{a, b, c\}$. The sign of the capacitor voltage difference is defined in (4.7). The selection between the positive and the negative short vectors is done based on the criteria summarised in Table 4.4. In conclusion, the algorithm tends to equalize the capacitor voltages by using the short vectors which drive the voltage error towards zero.

$$\text{sign}(i_k) = \begin{cases} 1 & \text{if } i_k \geq 0 \\ -1 & \text{if } i_k < 0 \end{cases} \quad (4.6)$$

$$\text{sign}(\Delta u_C) = \begin{cases} 1 & \text{if } u_{C1} \geq u_{C2} \\ -1 & \text{if } u_{C1} < u_{C2} \end{cases} \quad (4.7)$$

Table 4.3: DC bus midpoint current during the short vectors

Short vector	i_o
$\vec{u}_{onn}, \vec{u}_{opp}$	$+i_a$
$\vec{u}_{poo}, \vec{u}_{noo}$	$-i_a$
$\vec{u}_{oon}, \vec{u}_{oop}$	$-i_c$
$\vec{u}_{ppo}, \vec{u}_{nno}$	$+i_c$
$\vec{u}_{non}, \vec{u}_{pop}$	$+i_b$
$\vec{u}_{opo}, \vec{u}_{ono}$	$-i_b$

Table 4.4: Summary of the voltage balancing strategy

Region	IF TRUE use the negative short vector ELSE use the positive short vector
1	$\text{sign}(i_a) = \text{sign}(\Delta u_C)$
2	$\text{sign}(i_c) \neq \text{sign}(\Delta u_C)$
3	$\text{sign}(i_b) = \text{sign}(\Delta u_C)$
4	$\text{sign}(i_a) \neq \text{sign}(\Delta u_C)$
5	$\text{sign}(i_c) = \text{sign}(\Delta u_C)$
6	$\text{sign}(i_b) \neq \text{sign}(\Delta u_C)$

4.5 Switching sequence arrangement

Discontinuous modulation results in two switched transitions per a switching period: one turn-off-turn-on combination in two phase-legs and the third remains unswitched [118, 147]. If the NTV combination remains unchanged, the switching frequency is minimised when the modulator alternates between the direct and inverse vector sequences [118], let say, between $\vec{u}_1 - \vec{u}_2 - \vec{u}_3$ and $\vec{u}_3 - \vec{u}_2 - \vec{u}_1$. Additional switched transitions may though occur when the NTV combination changes, for example, because of the change of the subsector, or the applied DPWM patterns. Typically, it is recommended to realise such transitions with minimum extra switchings to save in switching losses [147, 185, 119]. This section focuses on the arrangement of consecutive NTV combinations and their effects on the voltage and current waveforms.

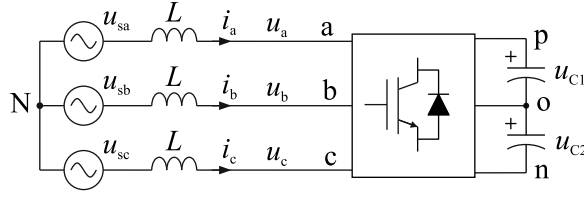


Fig. 4.4: Simple equivalent circuit of the three-wire three-level converter.

4.5.1 Switching ripple analysis

The switching ripple waveforms are analysed using vector quantities, similarly as in [186, 148], and the simplified circuit illustrated in Fig. 4.4. The following assumptions have been made for analysis purposes:

- The DC bus voltage is constant and $u_{C1} = u_{C2}$.
- The rectifier is connected to a three-phase AC source with sinusoidal, symmetrical and balanced voltages.
- The impedances in the three phases are balanced and purely inductive.
- The sampling frequency is high enough to allow considering the AC source voltages constants over a switching period T_s .
- Asymmetric regular sampling method is used.

Based on Fig. 4.4, the converter voltages with respect to 'N' can be expressed with (4.8), and they are subject to constraint $u_{aN} + u_{bN} + u_{cN} = 0$, which yields the zero-sequence component (4.9). The AC source is symmetrical and balanced and, therefore, $u_{saN} + u_{sbN} + u_{scN} = 0$.

$$u_{kN}(t) = u_{kn}(t) - u_{Nn}(t) \quad (4.8)$$

$$u_{Nn}(t) = \frac{1}{3}(u_{an}(t) + u_{bn}(t) + u_{cn}(t)) \quad (4.9)$$

When the voltages in (4.8) are transformed into $\alpha\beta$ coordinates, the zero-sequence component is cancelled out. Thus, the inductor current in the $\alpha\beta$ coordinates is

$$\vec{i}(t) = \frac{1}{L} \int_{t_0}^t (\vec{u}_s(t) - \vec{u}(t)) dt + \vec{i}(t_0) \quad (4.10)$$

Considering a switching period $t \in [kT_s, (k+1)T_s]$, as follows, the pulse-width modulated converter voltage can be separated into an average voltage component and a pulsating harmonic voltage component

$$\vec{u}(t) = \frac{1}{T_s} \int_{kT_s}^{(k+1)T_s} \vec{u}(t) dt + (\vec{u}(t) - \frac{1}{T_s} \int_{kT_s}^{(k+1)T_s} \vec{u}(t) dt) \quad (4.11a)$$

$$= \langle \vec{u} \rangle + (\vec{u}(t) - \langle \vec{u} \rangle) \quad (4.11b)$$

$$= \vec{u}^* + (\vec{u}(t) - \vec{u}^*) \quad (4.11c)$$

where $\langle \vec{u} \rangle$ denotes the average of $\vec{u}(t)$ over T_s , and is equal to \vec{u}^* . Also the inductor current can be split into a ripple-free component and a ripple component when (4.11c) is substituted in (4.10):

$$\vec{i}(t) = \frac{1}{L} \int_{kT_s}^{(k+1)T_s} (\vec{u}_s(t) - \vec{u}^*) dt + \frac{1}{L} \int_{kT_s}^{(k+1)T_s} (\vec{u}^* - \vec{u}(t)) dt + \vec{i}(kT_s) \quad (4.12)$$

Since the discontinuous SVM uses three voltage vectors during a switching period, the behaviour of the ripple current component can be expressed as

$$\vec{i}_{\text{rip}}(t) = \frac{1}{L} \int_{kT_s}^{(k+1)T_s} (\vec{u}^* - \vec{u}(t)) dt \quad (4.13a)$$

$$= \frac{1}{L} \int_{kT_s}^{(k+1)T_s} \vec{u}^* dt - \frac{1}{L} \left(\int_{kT_s}^{kT_s+T_1} \vec{u}_1 dt + \int_{kT_s+T_1}^{kT_s+T_1+T_2} \vec{u}_2 dt + \int_{kT_s+T_1+T_2}^{(k+1)T_s} \vec{u}_3 dt \right) \quad (4.13b)$$

where T_1 , T_2 , and T_3 are the duty times of the nearest three voltage vectors \vec{u}_1 , \vec{u}_2 , and \vec{u}_3 , respectively, and they fulfil $T_1 + T_2 + T_3 = T_s$. When (4.13b) is normalised with base current $I_{\text{base}} = \frac{u_{\text{DC}} T_s}{\sqrt{3}L}$, and the integration variable is changed, the per unit current ripple can be expressed as

$$\begin{aligned} \vec{i}_{\text{rip,pu}}(\delta) = & \int_0^1 \vec{m} d\delta - \int_0^{d_1} s\vec{w}_1 \frac{\sqrt{3}}{2} d\delta \\ & - \int_{d_1}^{d_1+d_2} s\vec{w}_2 \frac{\sqrt{3}}{2} d\delta - \int_{d_1+d_2}^1 s\vec{w}_3 \frac{\sqrt{3}}{2} d\delta \end{aligned} \quad (4.14)$$

where \vec{m} is the normalised reference voltage¹ and d_1 to d_3 are the duty cycles of the switching vectors $s\vec{w}_1$ to $s\vec{w}_3$.

Fig. 4.5(a) illustrates the trajectory of \vec{m} and the harmonic voltage vectors resulting from the modulation of \vec{m}_A and \vec{m}_B during two adjacent switching periods. Let us assume that the switching sequence during the first period is pon – poo – ppo, and the switching sequence over $2T_s$ can be either (i) or (ii), as follows:

(i) pon – poo – ppo – onn – oon – pon

(ii) pon – poo – ppo – pon – oon – onn

The sequence (i) includes eight switched transitions. The sequence (ii) includes six switched transitions and would minimise the switching frequency and losses.

Figs. 4.5(b) and 4.5(c) illustrate the per unit ripple current trajectories generated by the sequences (i) and (ii), and calculated using (4.14). During $0 \leq t \leq T_s$ the trajectories are defined by the triangles a – b – c – a and during $T_s \leq t \leq 2T_s$ by the

¹The normalised reference voltage $\|\vec{m}\|$ equals the amplitude modulation ratio of SVM

triangles $d - e - f - d$. The average ripple currents $\langle \vec{i}_{\text{rip,pu}} \rangle_1$, $\langle \vec{i}_{\text{rip,pu}} \rangle_2$, and $\langle \vec{i}_{\text{rip,pu}} \rangle_{12}$ in Figs. 4.5(b) and 4.5(c) are defined as follows:

$$\langle \vec{i}_{\text{rip,pu}} \rangle_1 = \int_0^1 \vec{i}_{\text{rip,pu}}(\delta) d\delta \quad (4.15)$$

$$\langle \vec{i}_{\text{rip,pu}} \rangle_2 = \int_1^2 \vec{i}_{\text{rip,pu}}(\delta) d\delta \quad (4.16)$$

$$\langle \vec{i}_{\text{rip,pu}} \rangle_{12} = \frac{1}{2} \int_0^2 \vec{i}_{\text{rip,pu}}(\delta) d\delta \quad (4.17)$$

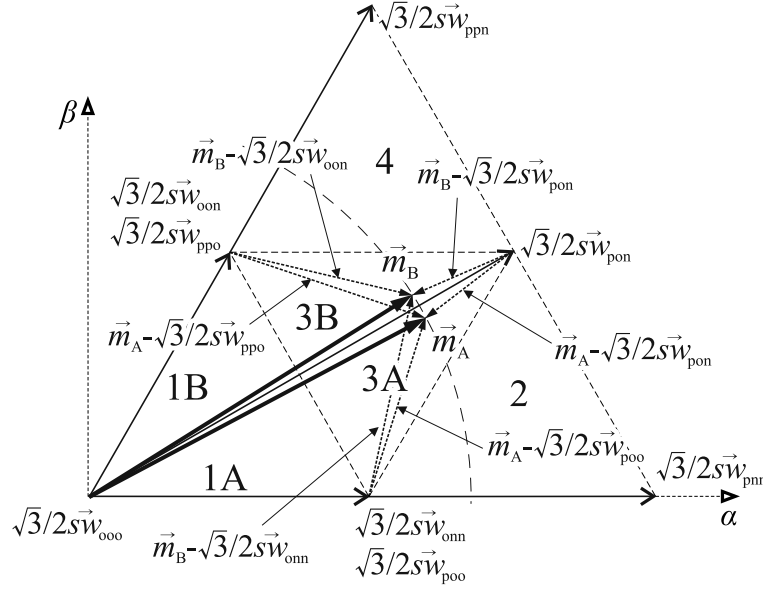
Based on Figs. 4.5(b) and 4.5(c), the sequences (i) and (ii) result in very different average ripple current over the two switching periods. In Fig. 4.5(b), $\langle \vec{i}_{\text{rip,pu}} \rangle_{12}$ is approximately zero, which implies that the ripple waveform is symmetrical. In Fig. 4.5(c), on the contrary, $\langle \vec{i}_{\text{rip,pu}} \rangle_{12}$ is nonzero because the PWM voltage waveform is not symmetrical between the two switching periods. It has been shown in [187] that discontinuities in the PWM voltage symmetry can cause grid current oscillations when an *LCL* filter is used. To prevent increasing the grid current distortion, the NTV combinations should be arranged and selected so that the waveform symmetry is retained.

4.5.2 Arrangement of adjacent switching sequences

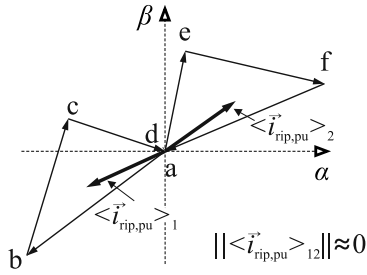
Fig. 4.5(a) shows that the subsectors 1, 2 and 4 of Sector 1 are defined by two voltage vectors longer and one shorter than the voltage reference. The subsector 3 is defined by two vectors shorter and one longer than the reference. The subsectors of Sector 2 to Sector 6 can be categorised in a similar manner. It can be deduced that, when the NTV sequence realised during a switching period involves two switched transitions, the applied vectors can appear in four different orders compared to the length of \vec{u}^* [187]:

- Shorter-longer-longer (for example $\vec{u}_{\text{onn}} - \vec{u}_{\text{pnn}} - \vec{u}_{\text{pon}}$)
- Shorter-shorter-longer (for example $\vec{u}_{\text{onn}} - \vec{u}_{\text{oon}} - \vec{u}_{\text{pon}}$)
- Longer-longer-shorter (for example $\vec{u}_{\text{pnn}} - \vec{u}_{\text{pon}} - \vec{u}_{\text{poo}}$)
- Longer-shorter-shorter (for example $\vec{u}_{\text{pon}} - \vec{u}_{\text{poo}} - \vec{u}_{\text{ppo}}$)

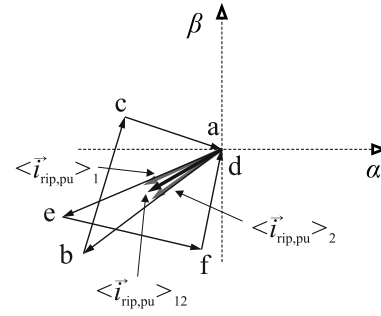
When the NTV combination remains unchanged during adjacent switching periods, it should be alternated in direct and inverse orders to minimise the switched transitions and achieve $\langle \vec{i}_{\text{rip,pu}} \rangle_{12} \approx 0$. The correct vector arrangement is achieved when the sequences are arranged according to the voltage vector lengths. It can be said, in terms of the voltage vector lengths, that if a switching period ends with a vector shorter (longer) than \vec{u}^* , also the next period should start with a shorter (longer) vector. As a result, the given NTV combination is alternated in direct and inverse orders.



(a)



(b)



(c)

Fig. 4.5: (a) Harmonic voltage vectors during the modulation of \vec{m}_A and \vec{m}_B . (b) The ripple current trajectory during the sequence (i): pon – poo – ppo – onn – oon – pon. (c) The ripple current trajectory during the sequence (ii): pon – poo – ppo – pon – oon – onn.

It is proposed in [187] that, to retain the waveform symmetry, the same arrangement criterion should be followed during the transitions between the subsectors and when the modulated NTV combination changes. Let us consider Figs. 4.5(a)-4.5(c) from the viewpoint of the proposed method. It is evident that the sequence (i) fulfils the

arrangement criterion and yields $\langle \vec{i}_{\text{rip,pu}} \rangle_{12} \approx 0$. On the other hand, the sequence (ii) minimises the switched transitions but it does not fulfil the arrangement criterion. As depicted in Fig. 4.5(c), the sequence (ii) generates an asymmetric ripple current trajectory. More similar examples can be found in [187].

The effects of the proposed arrangement criterion are exemplified by calculating the absolute value of $\langle \vec{i}_{\text{rip,pu}} \rangle_{12}$ in a moving two-sample window at different modulation indices for the DPWM0-DPWM3 patterns. In Figs. 4.6(a), 4.7(a), 4.8(a), and 4.9(a) the NTV combinations are arranged so that the switched transitions are minimised. Figs. 4.6(b), 4.7(b), 4.8(b), 4.9(b) are obtained by using the proposed switching sequence arrangement criterion.

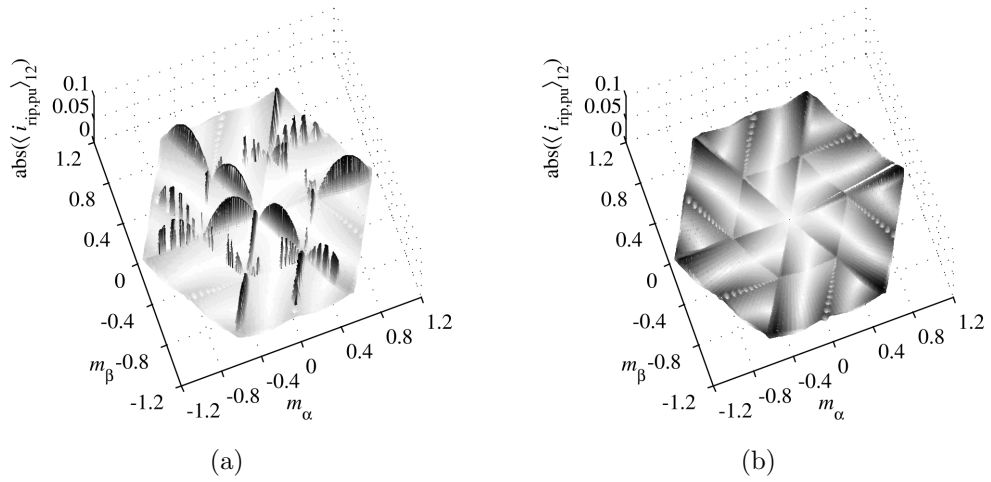


Fig. 4.6: Absolute value of $\langle \vec{i}_{\text{rip,pu}} \rangle_{12}$ for DPWM0 when (a) the switched transitions are minimised, (b) the proposed method is used.

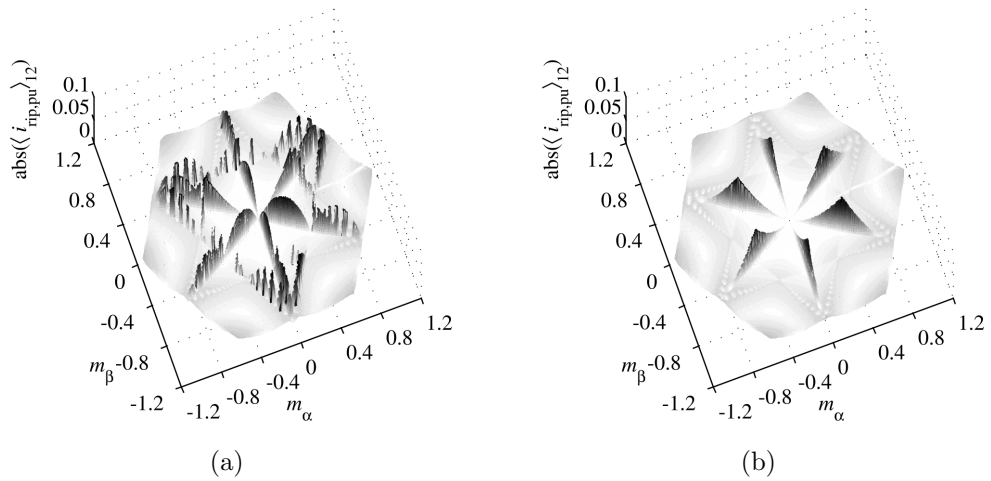


Fig. 4.7: Absolute value of $\langle \vec{i}_{\text{rip,pu}} \rangle_{12}$ for DPWM1 when (a) the switched transitions are minimised, (b) the proposed method is used.

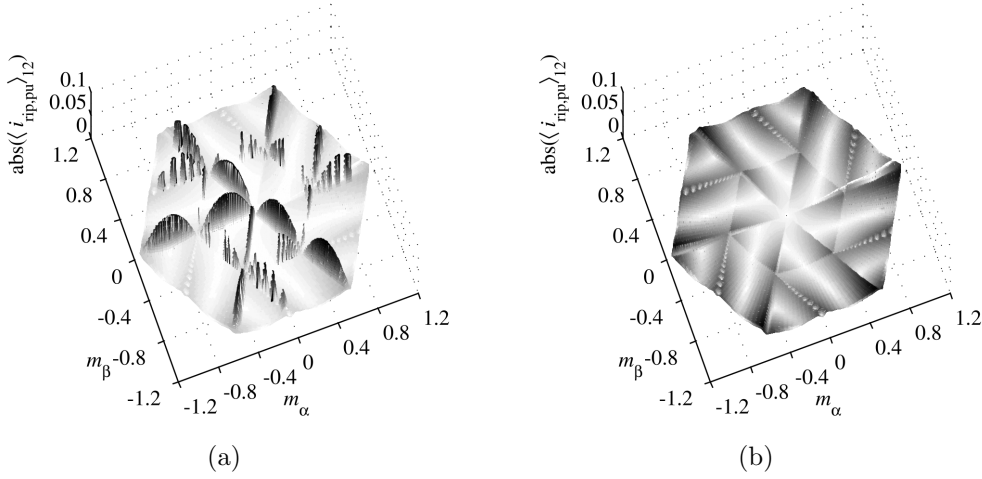


Fig. 4.8: Absolute value of $\langle \vec{i}_{rip,pu} \rangle_{12}$ for DPWM2 when (a) the switched transitions are minimised, (b) the proposed method is used.

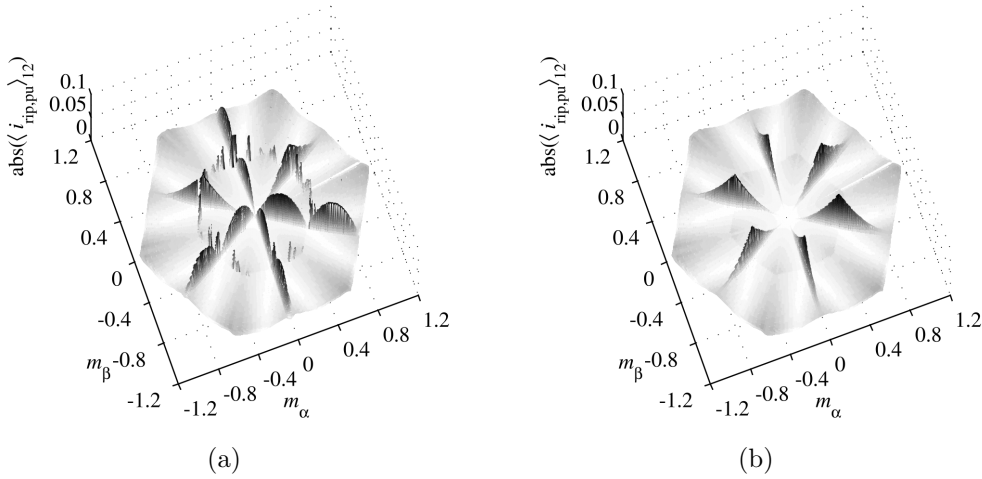


Fig. 4.9: Absolute value of $\langle \vec{i}_{rip,pu} \rangle_{12}$ for DPWM3 when (a) the switched transitions are minimised, (b) the proposed method is used.

The results indicate that, in the case of DPWM0 and DPWM2, the proposed method clearly decreases the $\langle \vec{i}_{rip,pu} \rangle_{12}$. Regarding the DPWM1 and DPWM3, $\langle \vec{i}_{rip,pu} \rangle_{12}$ is approximately zero elsewhere, but not during the transitions across the medium vectors. The phenomenon is caused by the placement of two short vectors within the NTV combinations, and their effect on the PWM waveforms. The value of $\langle \vec{i}_{rip,pu} \rangle_{12}$ reaches its maximum when the duty time of the third vector goes to zero. An additional arrangement criterion would be needed to solve the waveform problem. It should consider the harmonic voltage vectors created by the short vectors, and their placement within the sequence, when the transition across the medium vector occurs. Its effect can be deduced by comparing Figs. 4.7(a) and 4.7(b). The described criterion is not included in the implemented modulator and detailed investigation of it should be conducted during the future research.

The fact is that the proposed arrangement method causes additional switched transitions, which, however, can be avoided by slightly modifying the phase-leg discontinuity patterns. For example, in the case of DPWM1, a bus-to-bus switching occurs in the b-phase if the vector sequence $\vec{u}_{pon} - \vec{u}_{poo} - \vec{u}_{ppo} \rightarrow \vec{u}_{onn} - \vec{u}_{oon} - \vec{u}_{pon}$ is realised while the reference transitions between the subsectors 3A and 3B of Sector 1. Fig. 2.7 shows that in subsector 3A the DPWM1 clamps the a-phase to the DC+ bus. In subsector 3B, it clamps the c-phase to the DC- bus. As a result, the bus-to-bus transition is avoided if the a-phase clamping is continued until the transition to c-phase clamping can be carried out through the sequence $\vec{u}_{ppo} - \vec{u}_{poo} - \vec{u}_{pon} \rightarrow \vec{u}_{pon} - \vec{u}_{oon} - \vec{u}_{onn}$. The modification causes only a one switching period delay to the change of the clamped phase-leg. This type of modifications in the DPWM patterns have not been implemented in this thesis. The improvements should be studied during the future research.

4.6 Nonlinearity compensation algorithm

This section presents a method for the compensation of nonlinear voltage errors caused by the switching delays and the threshold voltage losses across the on-state power semiconductors. Firstly, the voltage errors are averaged over a switching period and described in terms of ideal voltage vectors and variables called 'error duty cycles'. After that, the error duty cycles are used to derive a closed-form expression for the duty cycles which compensate the average voltage errors. Finally, the solution of error voltage vectors and error duty cycles is described.

4.6.1 Compensation theory

Firstly, only the effects of the threshold voltage losses are considered. From here on, the actual converter voltage vectors are denoted as \vec{u}'_1 , \vec{u}'_2 , and \vec{u}'_3 . They can be expressed as ideal vectors \vec{u}_1 , \vec{u}_2 , and \vec{u}_3 superimposed by the error vectors \vec{u}_{e1} , \vec{u}_{e2} , and \vec{u}_{e3} . Consequently, the average converter voltage during a switching period T_s can be expressed in the $\alpha\beta$ coordinates as follows

$$\langle \vec{u} \rangle = d_1 \vec{u}'_1 + d_2 \vec{u}'_2 + d_3 \vec{u}'_3 \quad (4.18a)$$

$$= d_1(\vec{u}_1 + \vec{u}_{e1}) + d_2(\vec{u}_2 + \vec{u}_{e2}) + d_3(\vec{u}_3 + \vec{u}_{e3}) \quad (4.18b)$$

$$= \vec{u}^* + \overbrace{d_1 \vec{u}_{e1} + d_2 \vec{u}_{e2} + d_3 \vec{u}_{e3}}^{=\vec{u}_e} \quad (4.18c)$$

where \vec{u}_e is the difference between $\langle \vec{u} \rangle$ and \vec{u}^* , as depicted in Fig. 4.10.

Let us assume that the error \vec{u}_e does not shift $\langle \vec{u} \rangle$ to a different subsector compared with \vec{u}^* . The error vectors present in (4.18c) can be expressed as linear combinations

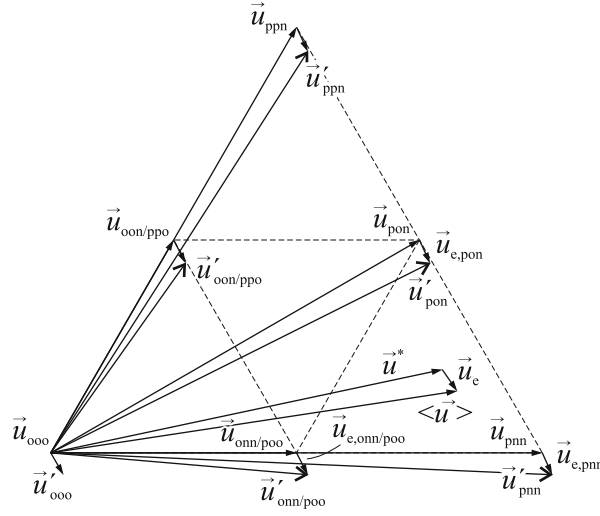


Fig. 4.10: Ideal voltage vectors superimposed by the error voltage vectors caused by the threshold voltage losses, and the resulting error \vec{u}_e in the average converter voltage $\langle \vec{u} \rangle$. The figure assumes $U_{F0,\text{fwd}} = U_{F0,\text{c}}$ and $i_a > 0$, $i_b < 0$, $i_c > 0$.

of \vec{u}_1 , \vec{u}_2 , and \vec{u}_3 , as follows

$$\begin{aligned} \langle \vec{u} \rangle = \vec{u}^* + d_1 \overbrace{(d_{e1,1}\vec{u}_1 + d_{e1,2}\vec{u}_2 + d_{e1,3}\vec{u}_3)}^{=\vec{u}_{e1}} + d_2 \overbrace{(d_{e2,1}\vec{u}_1 + d_{e2,2}\vec{u}_2 + d_{e2,3}\vec{u}_3)}^{=\vec{u}_{e2}} \\ + d_3 \overbrace{(d_{e3,1}\vec{u}_1 + d_{e3,2}\vec{u}_2 + d_{e3,3}\vec{u}_3)}^{=\vec{u}_{e3}} \end{aligned} \quad (4.19)$$

where $d_{e1,i}$, $d_{e2,i}$, and $d_{e3,i}$ with $i \in \{1, 2, 3\}$ denote the error duty cycles. By substituting $\vec{u}^* = d_1\vec{u}_1 + d_2\vec{u}_2 + d_3\vec{u}_3$ in (4.19), the generated average voltage can be expressed as

$$\begin{aligned} \langle \vec{u} \rangle = \vec{u}_1(d_1 + d_1d_{e1,1} + d_2d_{e2,1} + d_3d_{e3,1}) + \vec{u}_2(d_2 + d_1d_{e1,2} + d_2d_{e2,2} + d_3d_{e3,2}) \\ + \vec{u}_3(d_3 + d_1d_{e1,3} + d_2d_{e2,3} + d_3d_{e3,3}) \end{aligned} \quad (4.20)$$

To compensate the voltage error described in (4.19)-(4.20), a new set of duty cycles d'_1 , d'_2 , and d'_3 must be found which generate $\langle \vec{u} \rangle$ equal to \vec{u}^* so that the following condition is satisfied:

$$\langle \vec{u} \rangle = \vec{u}^* \quad (4.21)$$

$$\Leftrightarrow$$

$$d'_1\vec{u}'_1 + d'_2\vec{u}'_2 + d'_3\vec{u}'_3 = d_1\vec{u}_1 + d_2\vec{u}_2 + d_3\vec{u}_3 \quad (4.22)$$

The left-hand-side of (4.22) is the average voltage equal to \vec{u}^* in terms of the actual voltage vectors. The right-hand-side assumes ideal voltage vectors. When d_1 , d_2 , d_3

in (4.20) are replaced with d'_1 , d'_2 , d'_3 , it can be substituted to the left-hand-side of (4.22) which, after rearranging of the terms, yields the compensated average voltage:

$$\begin{aligned} \overbrace{d'_1 \vec{u}_1 + d'_2 \vec{u}_2 + d'_3 \vec{u}_3}^{\langle \vec{u} \rangle_{\text{comp}} = \vec{u}^* - \vec{u}_e} &= (d_1 - (d'_1 d_{e1,1} + d'_2 d_{e2,1} + d'_3 d_{e3,1})) \vec{u}_1 \\ &+ (d_2 - (d'_1 d_{e1,2} + d'_2 d_{e2,2} + d'_3 d_{e3,2})) \vec{u}_2 \\ &+ (d_3 - (d'_1 d_{e1,3} + d'_2 d_{e2,3} + d'_3 d_{e3,3})) \vec{u}_3 \end{aligned} \quad (4.23)$$

When the duty cycles of the respective voltage vectors on the both sides of (4.23) are equated, the equation group (4.24) can be developed. The solution of (4.24) yields (4.25), where d'_1 , d'_2 , and d'_3 are the duty cycles that compensate the average error caused by the semiconductor threshold voltage losses. In conclusion, the computation of d'_1 , d'_2 , and d'_3 requires the error duty cycles $d_{e1,i}$ to $d_{e3,i}$. Their solution is described in Sections 4.6.2-4.6.3.

$$\begin{cases} d'_1 = d_1 - (d'_1 d_{e1,1} + d'_2 d_{e2,1} + d'_3 d_{e3,1}) \\ d'_2 = d_2 - (d'_1 d_{e1,2} + d'_2 d_{e2,2} + d'_3 d_{e3,2}) \\ d'_3 = d_3 - (d'_1 d_{e1,3} + d'_2 d_{e2,3} + d'_3 d_{e3,3}) \\ d'_1 + d'_2 + d'_3 = 1 \end{cases} \quad (4.24)$$

$$\begin{cases} d'_1 = \frac{(d_{e2,2} - d_{e3,2} + 1)(d_1 - d_{e3,1}) + (d_{e2,1} - d_{e3,1})(d_{e3,2} - d_2)}{(d_{e1,1} - d_{e3,1} + 1)(d_{e2,2} - d_{e3,2} + 1) - (d_{e2,1} - d_{e3,1})(d_{e1,2} - d_{e3,2})} \\ d'_2 = \frac{(d_{e1,1} - d_{e3,1} + 1)(d_{e3,2} - d_2) + (d_1 - d_{e3,1})(d_{e1,2} - d_{e3,2})}{(d_{e2,1} - d_{e3,1})(d_{e1,2} - d_{e3,2}) - (d_{e1,1} - d_{e3,1} + 1)(d_{e2,2} - d_{e3,2} + 1)} \\ d'_3 = 1 - d'_1 - d'_2 \end{cases} \quad (4.25)$$

Next, the semiconductor voltage losses are neglected and only the voltage errors caused by the blanking times are considered. The average voltage during a switching period can be expressed as

$$\langle \vec{u} \rangle = \vec{u}^* + \vec{u}_{e1,\text{dt}} + \vec{u}_{e2,\text{dt}} + \vec{u}_{e3,\text{dt}} \quad (4.26)$$

where $\vec{u}_{e1,\text{dt}}$ denotes the voltage error caused by the delay in the transition from the last vector of the previous switching period to the first vector of the current switching period. The voltage errors $\vec{u}_{e2,\text{dt}}$ and $\vec{u}_{e3,\text{dt}}$ are caused by the transitions $\vec{u}_1 \rightarrow \vec{u}_2$ and $\vec{u}_2 \rightarrow \vec{u}_3$, respectively.

The error voltages $\vec{u}_{e1,\text{dt}}$, $\vec{u}_{e2,\text{dt}}$, $\vec{u}_{e3,\text{dt}}$ in (4.26) are assumed independent of the duty cycles d_1 , d_2 , and d_3 . The constraint is satisfied if the duty times of two adjacent vectors are longer than the switching delay between them. In that case, the cumulative error \vec{u}_{dt} can be expressed as the sum of \vec{u}_1 , \vec{u}_2 , and \vec{u}_3 weighted by the error duty cycles $d_{\text{dt}1}$, $d_{\text{dt}2}$, and $d_{\text{dt}3}$

$$\langle \vec{u} \rangle = \vec{u}^* + \overbrace{d_{\text{dt}1} \vec{u}_1 + d_{\text{dt}2} \vec{u}_2 + d_{\text{dt}3} \vec{u}_3}^{=\vec{u}_{\text{dt}} = \vec{u}_{e1,\text{dt}} + \vec{u}_{e2,\text{dt}} + \vec{u}_{e3,\text{dt}}} \quad (4.27a)$$

$$= \vec{u}_1(d_1 + d_{\text{dt}1}) + \vec{u}_2(d_2 + d_{\text{dt}2}) + \vec{u}_3(d_3 + d_{\text{dt}3}) \quad (4.27b)$$

where the error duty cycles are subject to $d_{dt1} + d_{dt2} + d_{dt3} = 0$, because $d_1 + d_2 + d_3 = 1$. As a result, (4.27b) shows that the blanking times can be compensated by subtracting d_{dt1} , d_{dt2} , d_{dt3} from d_1 , d_2 , and d_3 , respectively:

$$\langle \vec{u} \rangle_{\text{comp}} = \vec{u}^* = \vec{u}_1(d_1 - d_{dt1}) + \vec{u}_2(d_2 - d_{dt2}) + \vec{u}_3(d_3 - d_{dt3}) \quad (4.28)$$

Finally, (4.25) and (4.28) are combined to compensate the average voltage errors caused by the both phenomena. The compensation of the semiconductor voltage losses, described in (4.25), is performed first. Then, the obtained duty cycles are substituted in (4.28), which compensates the error caused by the switching delays. The resulting duty cycles are subject to $d'_1 \geq 0$, $d'_2 \geq 0$, $d'_3 \geq 0$, and $d'_1 + d'_2 + d'_3 = 1$. If the constraints are not fulfilled, the voltage errors cannot be fully compensated.

4.6.2 Estimation of the error voltage vectors

The information on phase current polarities is required to approximate the average error voltages caused by the blanking times and the semiconductor voltage losses. At low output currents, or during the zero crossings of the fundamental frequency current, the phase current polarity can change multiple times during a switching period because of the switching ripple current. In that case, the ripple current waveform can be approximated to estimate the error voltages.

Because of the sample-and-hold operation of the control, the voltage reference computed during $[kT_s, (k+1)T_s]$ is realised by the modulator during the interval $[(k+1)T_s, (k+2)T_s]$. To predict the converter currents in the beginning of interval $[(k+1)T_s, (k+2)T_s]$, the currents sampled at $t = kT_s$ are extrapolated assuming linear behaviour. After that, the inductor current at the instants $t_0 = 0$, $t_1 = T_1$, $t_2 = T_1 + T_2$, and $t_3 = T_1 + T_2 + T_3$ can be estimated as follows

$$\vec{i}(t_0) = \vec{i}(kT_s) + (\vec{i}(kT_s) - \vec{i}((k-1)T_s)) \quad (4.29)$$

$$\vec{i}(t_1) = \vec{i}(t_0) + \frac{1}{L_1} T_1 (\vec{u}^* - \vec{u}_1) \quad (4.30)$$

$$\vec{i}(t_2) = \vec{i}(t_1) + \frac{1}{L_1} T_2 (\vec{u}^* - \vec{u}_2) \quad (4.31)$$

$$\vec{i}(t_3) = \vec{i}(t_2) + \frac{1}{L_1} T_3 (\vec{u}^* - \vec{u}_3) \quad (4.32)$$

where L_1 is the inductance of the converter-side filter inductor and T_1 , T_2 , and T_3 are the duty times of the NTVs. The voltages on the source-side of the inductors have been assumed approximately constants over a sample period T_s .

The zero-crossing instants of the phase currents during T_s are needed to estimate the threshold voltage losses. Constant $\frac{di}{dt}$ is assumed between the intervals $t_0 \dots t_1$, $t_1 \dots t_2$, and $t_2 \dots t_3$. The zero-crossing instant between $[t_{i-1}, t_i]$, $i \in \{1, 2, 3\}$ can be

solved as follows

$$i(t_{i-1}) + \frac{i(t_i) - i(t_{i-1})}{T_i} t_{zc,i} = 0 \quad (4.33)$$

\Rightarrow

$$t_{zc,i} = \frac{-i(t_{i-1})T_i}{i(t_i) - i(t_{i-1})} \quad (4.34)$$

where $i(t_{i-1})$ and $i(t_i)$ denote the phase current at t_{i-1} and t_i , respectively. When (4.34) is normalised with T_i and limited between $t_{zc,i}/T_i = [0, 1]$, the average phase-voltage error during $[t_{i-1}, t_i]$ is

$$\langle u_e \rangle_i = d_{zc,i} u_e(t_{i-1}) + (1 - d_{zc,i}) u_e(t_i) \quad (4.35)$$

where $d_{zc,i}$ denotes the duty ratio and $u_e(t_{i-1})$ and $u_e(t_i)$ are the threshold voltage losses occurring at t_{i-1} and t_i , respectively. Voltage losses $u_e(t_{i-1})$ and $u_e(t_i)$ can be determined from Table 2.5 based on the current polarity and the applied switch combination. After the phase voltage errors during the application of the NTVs are solved, the error voltage vectors \vec{u}_{e1} , \vec{u}_{e2} , and \vec{u}_{e3} can be calculated.

The average voltage error caused by the blanking times can be estimated using Table 2.4. The phase current polarities at the switching instants can be solved from (4.29)-(4.32) and the switched transitions occurring during the sample period can be deduced from the applied NTV sequence. After that, the error voltage vectors $\vec{u}_{e1,dt}$, $\vec{u}_{e2,dt}$, and $\vec{u}_{e3,dt}$ can be solved.

4.6.3 Solution of the error duty cycles

The duty cycles of the error voltage vectors can be solved by applying the theory studied in Section 4.3. Fig. 4.11 depicts the reference \vec{u}^* which is superimposed by an arbitrary error \vec{u}_e . When the projections of error $(\vec{u}^* + \vec{u}_e) - \vec{u}^*$ on the Sector 1 boundaries are normalised with base voltage $\frac{1}{3}u_{DC}$, they can be expressed as

$$\Delta m_1 = m_{1e} - m_1 \quad (4.36)$$

$$\Delta m_2 = m_{2e} - m_2 \quad (4.37)$$

$$\begin{aligned} \Delta m_{12} &= (2 - m_{1e} - m_{2e}) - (2 - m_1 - m_2) \\ &= m_{12e} - m_{12} = -\Delta m_1 - \Delta m_2 \end{aligned} \quad (4.38)$$

where m_{1e} , m_{2e} , and m_{12e} denote the projections of $\vec{u}^* + \vec{u}_e$, and $\Delta m_1 + \Delta m_2 + \Delta m_{12} = 0$.

The error vector \vec{u}_e can be presented as a vector sum of the NTVs if both $(\vec{u}^* + \vec{u}_e)$ and \vec{u}^* are expressed in line with (2.12b). In fact, the difference $\vec{u}_e = (\vec{u}^* + \vec{u}_e) - \vec{u}^*$ can be expressed as

$$\vec{u}_e = \left(-\frac{\|\Delta \vec{p}_1\|}{\|\vec{l}_1\|} - \frac{\|\Delta \vec{p}_2\|}{\|\vec{l}_2\|} \right) \vec{u}_1 + \frac{\|\Delta \vec{p}_2\|}{\|\vec{l}_2\|} \vec{u}_2 + \frac{\|\Delta \vec{p}_1\|}{\|\vec{l}_1\|} \vec{u}_3 \quad (4.39a)$$

$$= d_{e1} \vec{u}_1 + d_{e2} \vec{u}_2 + d_{e3} \vec{u}_3 \quad (4.39b)$$

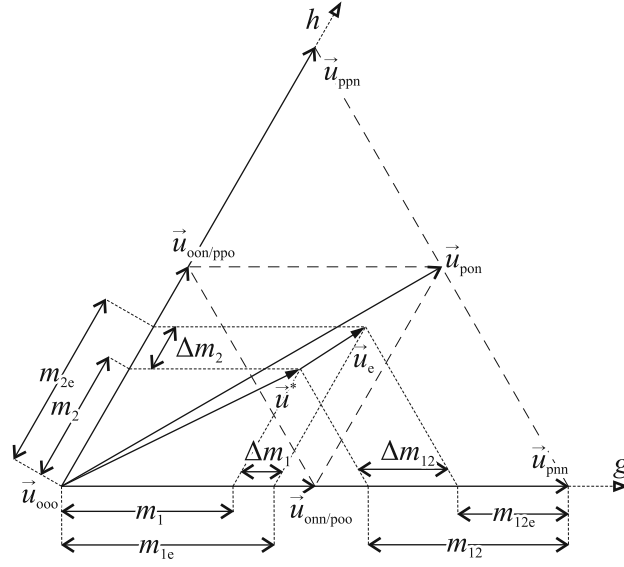


Fig. 4.11: Error vector projections Δm_1 , Δm_2 , and Δm_{12} .

where the projection lengths $\|\Delta \vec{p}_1\|$ and $\|\Delta \vec{p}_2\|$ can be described using Δm_1 , Δm_2 , and Δm_{12} . Consequently, in Sector 1 and Sector 2, the duty cycles of the error voltage vectors can be solved by following the theory presented in Section 4.3, and as summarised in Tables 4.5 and 4.6. In Sector 3 and Sector 5, the duty cycles of the error vectors are found by using the transformations reviewed in Appendix B on Table 4.5. In a similar manner, in Sector 4 and Sector 6, the error vector duty cycles can be solved by using the transformations of Appendix B on Table 4.6.

The relative alignment of \vec{u}_e with respect to \vec{u}^* must be maintained during the error duty cycles calculation to prevent incorrect compensation. In this thesis, Δm_1 and Δm_2 are solved by rotating \vec{u}_e to Sector 1, as described in Section 4.2. Before the solution of Δm_{12} and the error duty cycles, the projections Δm_1 and Δm_2 are transformed $(m - n)60^\circ$ counter-clockwise, where m denotes the original sector of \vec{u}_e and n denotes the original sector of \vec{u}^* . As a result, the relative alignment between \vec{u}_e and \vec{u}^* remains unchanged. The transformation of Δm_1 and Δm_2 between the sectors can be implemented by using the methods reviewed in Appendix A.

Table 4.5: Error duty cycles solution in Sector 1

NTV combinations based on negative short vectors			
Subsector	Error duty cycles		
1	$d_{e,onn} = \frac{\Delta m_1}{\gamma_n}$	$d_{e,oon} = \frac{\Delta m_2}{\gamma_n}$	$d_{e,ooo} = -d_{e,onn} - d_{e,oon}$
2	$d_{e,onn} = \frac{\Delta m_{12}}{\gamma_p}$	$d_{e,pon} = \frac{\Delta m_2}{\gamma_n}$	$d_{e,pnn} = -d_{e,onn} - d_{e,pon}$
3	$d_{e,onn} = \frac{-\Delta m_2}{\gamma_n}$	$d_{e,pon} = \frac{-\Delta m_{12}}{\gamma_p}$	$d_{e,oon} = -d_{e,onn} - d_{e,pon}$
4	$d_{e,oon} = \frac{\Delta m_{12}}{\gamma_p}$	$d_{e,pon} = \frac{\Delta m_1}{\gamma_p}$	$d_{e,ppn} = -d_{e,oon} - d_{e,pon}$
NTV combinations based on positive short vectors			
Subsector	Error duty cycles		
1	$d_{e,poo} = \frac{\Delta m_1}{\gamma_p}$	$d_{e,ppo} = \frac{\Delta m_2}{\gamma_p}$	$d_{e,ooo} = -d_{e,poo} - d_{e,ppo}$
2	$d_{e,poo} = \frac{\Delta m_{12}}{\gamma_n}$	$d_{e,pon} = \frac{\Delta m_2}{\gamma_n}$	$d_{e,pnn} = -d_{e,poo} - d_{e,pon}$
3	$d_{e,ppo} = \frac{-\Delta m_1}{\gamma_p}$	$d_{e,pon} = \frac{-\Delta m_{12}}{\gamma_n}$	$d_{e,poo} = -d_{e,ppo} - d_{e,pon}$
4	$d_{e,ppo} = \frac{\Delta m_{12}}{\gamma_n}$	$d_{e,pon} = \frac{\Delta m_1}{\gamma_p}$	$d_{e,ppn} = -d_{e,ppo} - d_{e,pon}$

Table 4.6: Error duty cycles solution in Sector 2

NTV combinations based on negative short vectors			
Subsector	Error duty cycles		
1	$d_{e,non} = \frac{\Delta m_2}{\gamma_n}$	$d_{e,oon} = \frac{\Delta m_1}{\gamma_n}$	$d_{e,ooo} = -d_{e,non} - d_{e,oon}$
2	$d_{e,oon} = \frac{\Delta m_{12}}{\gamma_p}$	$d_{e,opn} = \frac{\Delta m_2}{\gamma_p}$	$d_{e,ppn} = -d_{e,oon} - d_{e,opn}$
3	$d_{e,non} = \frac{-\Delta m_1}{\gamma_n}$	$d_{e,opn} = \frac{-\Delta m_{12}}{\gamma_p}$	$d_{e,oon} = -d_{e,non} - d_{e,opn}$
4	$d_{e,non} = \frac{\Delta m_{12}}{\gamma_p}$	$d_{e,opn} = \frac{\Delta m_1}{\gamma_n}$	$d_{e,npn} = -d_{e,non} - d_{e,opn}$
NTV combinations based on positive short vectors			
Subsector	Error duty cycles		
1	$d_{e,opo} = \frac{\Delta m_2}{\gamma_p}$	$d_{e,ppo} = \frac{\Delta m_1}{\gamma_p}$	$d_{e,ooo} = -d_{e,opo} - d_{e,ppo}$
2	$d_{e,ppo} = \frac{\Delta m_{12}}{\gamma_n}$	$d_{e,opn} = \frac{\Delta m_2}{\gamma_p}$	$d_{e,pnn} = -d_{e,ppo} - d_{e,opn}$
3	$d_{e,ppo} = \frac{-\Delta m_2}{\gamma_p}$	$d_{e,opn} = \frac{-\Delta m_{12}}{\gamma_n}$	$d_{e,poo} = -d_{e,ppo} - d_{e,opn}$
4	$d_{e,opo} = \frac{\Delta m_{12}}{\gamma_n}$	$d_{e,opn} = \frac{\Delta m_1}{\gamma_n}$	$d_{e,ppn} = -d_{e,opo} - d_{e,opn}$

4.7 Modulator program flow

Fig. 4.12 summarises the program flow of the modulation algorithm and the execution order of the modulator functions. The modulation algorithm is implemented on a microcontroller and is verified in a small-scale three-level STATCOM prototype. The experimental setup is described and the test results are provided in Chapter 6.

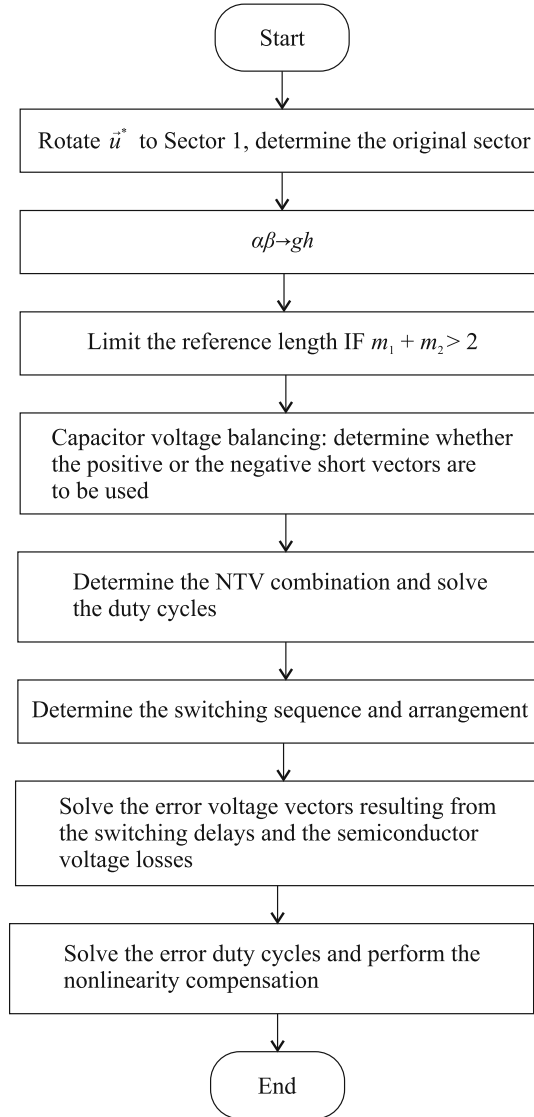


Fig. 4.12: Flowchart of the modulation algorithm.

4.8 Conclusions

This chapter presented the functions and the program flow of the implemented discontinuous space-vector modulation algorithm. Firstly, the solution of vector projections and duty cycles was presented. After that, the capacitor voltage balancing algorithm was described. It changes between the different DPWM patterns so that the voltage difference is driven towards zero. The balancing algorithm can not fully suppress the neutral-point voltage variation. However, the effect of capacitor voltage imbalance on the output voltage is compensated by the duty cycles solution algorithm. As a result, the modulator generates correct output voltages despite neutral-point oscillations.

Various scientific publications underline that the number of switched transitions should be minimised when moving from a switching period to the next. It was revealed that such operation generates discontinuities in the switching waveform symmetry which may deteriorate the grid current waveform, especially when an *LCL* filter is used. An arrangement method was proposed to decrease the waveform asymmetry, and its effect was studied. It was shown that the proposed method improves the waveform symmetry, but was not optimal. Possible improvements were proposed and further research is needed to optimise the switching sequence arrangement criteria.

A new algorithm was proposed for the compensation of the average voltage error caused by the blanking times and threshold voltage losses of the power semiconductors. A challenge of the compensation is the accuracy of phase current polarity detection. In the recent publications [131] and [132] the polarities are determined from the sampled currents at the start of each switching period. The solution is not optimal if the current ripple is large compared to the fundamental wave, because the polarity can change during the switching period and lead to over or undercompensation. In this thesis, the phase current polarities were determined by approximating the ripple current waveform, as described in Section 4.6.2.

Another problem may occur near the subsector boundaries. If the voltage error to be compensated is large, it may not be fully cancelled by manipulating the duty cycles of the given NTV combination, which is selected based on the location of the reference before the voltage error magnitude is known. Iteration could be used to find another NTV combination that enables full compensation, but is not desired because of the computational burden. An alternative solution could be to predict the error and use it to select an NTV combination that enables full error compensation. The prediction could be developed by assuming that the current polarities remain unchanged, the switching sequence of the previous switching period is executed in the opposite direction during the current one, and the semiconductor voltage losses remain unchanged. In conclusion, the issues with compensation accuracy need further research.

Chapter 5

Grid current control

5.1 Introduction

This chapter studies the characteristics of two grid current control strategies. The analyses are based on the average models presented in Chapter 3. The models are discretised and the closed-loop current control law, as well as the control computation delay, are included. The following assumptions and limitations apply to the analyses:

- The maximum frequency of the average models is half the control sampling frequency
- The losses of the rectifier bridge and the DC bus are omitted
- The modulation index is within the linear region
- The DC capacitor voltages are maintained in balance by the control
- The dynamics of DC bus voltage and the interaction between the AC and DC circuits is not considered

The outline of the chapter is following. In Section 5.2, the discrete-time model of the closed-loop current control is developed. Then the characteristics of the current controllers are studied in Section 5.3 and Section 5.4. The Smith predictor is derived and included in the current controllers in Section 5.5, and its effect is investigated. The effect of grid impedance on the current controllers' stability is revealed in Section 5.6. The conclusions are drawn in Section 5.7.

5.2 Discrete-time models

This section describes the development of discrete-time models of the closed-loop current control. The continuous-time models presented in Chapter 3 can be ex-

pressed as

$$\dot{\mathbf{x}}(t) = \mathbf{A}\mathbf{x}(t) + \mathbf{B}\mathbf{u}(t) + \mathbf{E}\mathbf{w}(t) \quad (5.1)$$

$$\mathbf{y}(t) = \mathbf{C}\mathbf{x}(t) + \mathbf{D}\mathbf{u}(t) + \mathbf{H}\mathbf{w}(t) \quad (5.2)$$

$$\mathbf{u}(t) = [u_{1d} \quad u_{1q}]^T \quad (5.3)$$

$$\mathbf{w}(t) = [u_{gd} \quad u_{gq}]^T \quad (5.4)$$

where \mathbf{E} and \mathbf{H} are the coefficient matrices of the stiff grid voltage which is considered as the disturbance $\mathbf{w}(t)$.

Let us assume that the modulator generates average rectifier voltages equal to the references during each switching period T_s . Then the continuous-time model can be discretised using the zero-order hold method [188], which yields

$$\mathbf{x}(k+1) = \mathbf{\Phi}\mathbf{x}(k) + \mathbf{\Gamma}_u\mathbf{u}(k) + \mathbf{\Gamma}_w\mathbf{w}(k) \quad (5.5)$$

$$\mathbf{y}(k) = \mathbf{C}\mathbf{x}(k) + \mathbf{D}\mathbf{u}(k) + \mathbf{H}\mathbf{w}(k) \quad (5.6)$$

$$\mathbf{\Phi} = e^{\mathbf{A}T_s} \quad (5.7)$$

$$\mathbf{\Gamma}_u = \left(\int_0^{T_s} e^{\mathbf{A}\tau} d\tau \right) \mathbf{B} \quad (5.8)$$

$$\mathbf{\Gamma}_w = \left(\int_0^{T_s} e^{\mathbf{A}\tau} d\tau \right) \mathbf{E} \quad (5.9)$$

The control delay is modelled by introducing a new state variable $\mathbf{u}(k-1)$ for the delayed modulator input (voltage reference) [184]. As a result, the state equation can be expressed as

$$\begin{bmatrix} \mathbf{x}(k+1) \\ \mathbf{u}(k) \end{bmatrix} = \begin{bmatrix} \mathbf{\Phi} & \mathbf{\Gamma}_u \\ \mathbf{0} & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{x}(k) \\ \mathbf{u}(k-1) \end{bmatrix} + \begin{bmatrix} \mathbf{0} \\ \mathbf{I} \end{bmatrix} \mathbf{u}(k) + \begin{bmatrix} \mathbf{\Gamma}_w \\ \mathbf{0} \end{bmatrix} \mathbf{w}(k) \quad (5.10)$$

$$\mathbf{y}(k) = [\mathbf{C} \quad \mathbf{D}] \begin{bmatrix} \mathbf{x}(k) \\ \mathbf{u}(k-1) \end{bmatrix} + [\mathbf{0}] \mathbf{u}(k) + [\mathbf{H}] \mathbf{w}(k) \quad (5.11)$$

The closed-loop control law is included in (5.10) as a linear combination of the state variables and the disturbances

$$\begin{bmatrix} \mathbf{x}(k+1) \\ \mathbf{u}(k) \end{bmatrix} = \begin{bmatrix} \mathbf{\Phi} & \mathbf{\Gamma}_u \\ \mathbf{L}_x & \mathbf{L}_u \end{bmatrix} \begin{bmatrix} \mathbf{x}(k) \\ \mathbf{u}(k-1) \end{bmatrix} + \begin{bmatrix} \mathbf{\Gamma}_w & \mathbf{0} \\ \mathbf{L}_w & \mathbf{L}_r \end{bmatrix} \begin{bmatrix} \mathbf{w}(k) \\ \mathbf{r}(k) \end{bmatrix} \quad (5.12)$$

$$\mathbf{y}(k) = [\mathbf{C} \quad \mathbf{D}] \begin{bmatrix} \mathbf{x}(k) \\ \mathbf{u}(k-1) \end{bmatrix} + [\mathbf{H} \quad \mathbf{0}] \begin{bmatrix} \mathbf{w}(k) \\ \mathbf{r}(k) \end{bmatrix} \quad (5.13)$$

where $\mathbf{r}(k)$ is the current reference and \mathbf{L}_x , \mathbf{L}_u , \mathbf{L}_w , and \mathbf{L}_r contain the control coefficients. Fig. 5.1 illustrates the block scheme of the closed-loop current control based on (5.12).

In this study, the rectifier current $\mathbf{i}_1(k) = [i_{1d} \quad i_{1q}]^T$ and the grid voltage $\mathbf{u}_2(k) = [u_{2d} \quad u_{2q}]^T$ at the coupling point are measured for current control purposes. They

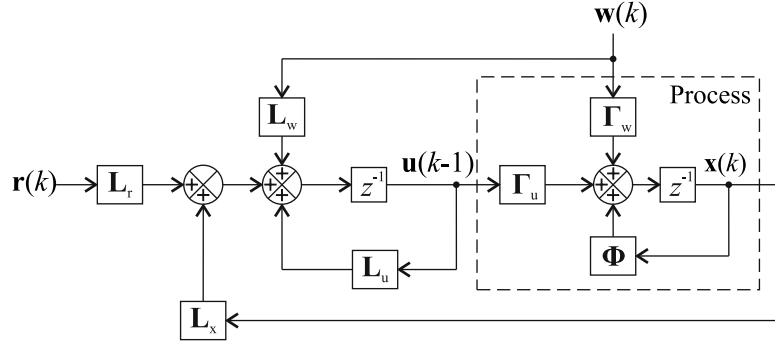


Fig. 5.1: General block scheme of the closed-loop current control.

are not found as state variables in all average models presented in Chapter 3 but can be solved as follows

$$\begin{bmatrix} \mathbf{i}_1(k) \\ \mathbf{u}_2(k) \end{bmatrix} = \begin{bmatrix} \mathbf{K}_{i1-x} & \mathbf{K}_{i1-u} \\ \mathbf{K}_{u2-x} & \mathbf{K}_{u2-u} \end{bmatrix} \begin{bmatrix} \mathbf{x}(k) \\ \mathbf{u}(k-1) \end{bmatrix} + \begin{bmatrix} \mathbf{K}_{i1-w} \\ \mathbf{K}_{u2-w} \end{bmatrix} \mathbf{w}(k) \quad (5.14)$$

where \mathbf{K}_{i1-x} , \mathbf{K}_{i1-u} , \mathbf{K}_{i1-w} and \mathbf{K}_{u2-x} , \mathbf{K}_{u2-u} , \mathbf{K}_{u2-w} are developed from (3.48), (3.63), (3.70), and (3.72) depending on the analysed model. If the model assumes an ideal grid, $\mathbf{K}_{u2-x} = \mathbf{K}_{u2-u} = \mathbf{0}$ and $\mathbf{K}_{u2-w} = \mathbf{I}$, which yields $\mathbf{w}(k) = \mathbf{u}_2(k)$. When $\mathbf{i}_1(k)$ is a state variable, $\mathbf{K}_{i1-u} = \mathbf{K}_{i1-w} = \mathbf{0}$, and \mathbf{K}_{i1-x} is defined as required. As a result, the coefficient matrices in (5.12) can be re-expressed as follows

$$\mathbf{L}_x = \mathbf{L}_{i1}\mathbf{K}_{i1-x} + \mathbf{L}_{u2}\mathbf{K}_{u2-x} \quad (5.15)$$

$$\mathbf{L}_u = \mathbf{L}_{u1} + \mathbf{L}_{i1}\mathbf{K}_{i1-u} + \mathbf{L}_{u2}\mathbf{K}_{u2-u} \quad (5.16)$$

$$\mathbf{L}_w = \mathbf{L}_{i1}\mathbf{K}_{i1-w} + \mathbf{L}_{u2}\mathbf{K}_{u2-w} \quad (5.17)$$

where \mathbf{L}_{i1} , \mathbf{L}_{u1} , and \mathbf{L}_{u2} include the control coefficients of $\vec{i}_1(k)$, $\vec{u}_1^*(k-1)$, and $\vec{u}_2(k)$, respectively. Fig. 5.2 illustrates the block scheme of the particular closed-loop model under study, including the effect of (5.15)-(5.17).

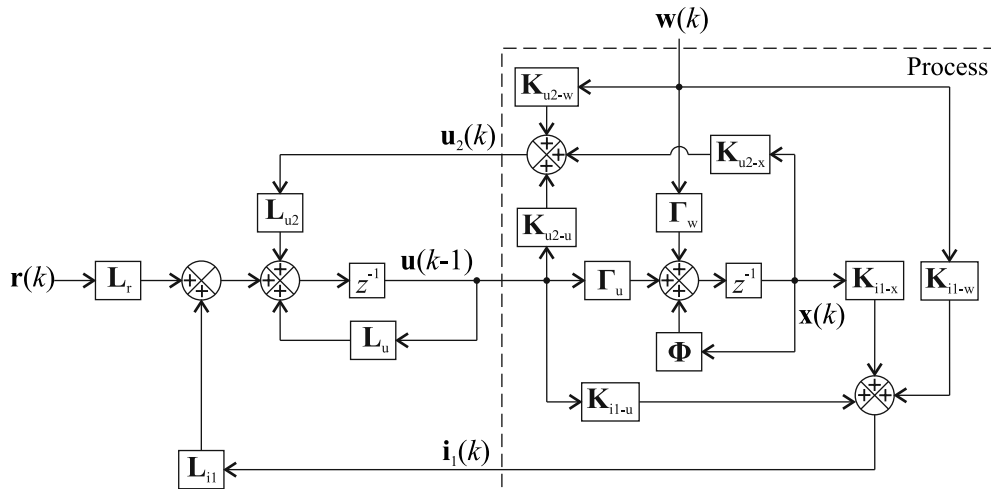


Fig. 5.2: Block scheme of the particular model of the closed-loop current control.

5.3 Synchronous reference frame PI current control

5.3.1 Closed-loop model

In this section, the closed-loop model is developed for the PI current control strategy. Based on the block scheme depicted in Fig. 2.14, the rectifier voltage references can be expressed as

$$u_{1d}^*(k) = u_{2d}(k) - (y_{PI d}(k) - \omega_r L_{tot} i_{1q}(k)) \quad (5.18)$$

$$u_{1q}^*(k) = u_{2q}(k) - (y_{PI q}(k) + \omega_r L_{tot} i_{1d}(k)) \quad (5.19)$$

The discrete-time PI controller outputs¹ are

$$y_{PI}(k) = K_p(1 + K_i T_s) e_{PI}(k) + y_{PI}(k-1) - K_p e_{PI}(k-1) \quad (5.20)$$

where $e_{PI}(k)$ is the error between the reference and the feedback, T_s is the sample time, K_p is the proportional gain, and K_i is the inverse of the integration time.

When (5.20) is substituted in (5.18) and (5.19), the control law can be written as follows

$$\begin{aligned} \begin{bmatrix} u_{1d}^*(k) \\ u_{1q}^*(k) \end{bmatrix} &= \mathbf{L}_{i1} \begin{bmatrix} i_{1d}(k) \\ i_{1q}(k) \end{bmatrix} + \mathbf{L}_{ePI} \begin{bmatrix} e_{PI d}(k-1) \\ e_{PI q}(k-1) \end{bmatrix} + \mathbf{L}_{yPI} \begin{bmatrix} y_{PI d}(k-1) \\ y_{PI q}(k-1) \end{bmatrix} \\ &+ \mathbf{L}_{u2} \begin{bmatrix} u_{2d}(k) \\ u_{2q}(k) \end{bmatrix} + \mathbf{L}_r \begin{bmatrix} i_{1d}^*(k) \\ i_{1q}^*(k) \end{bmatrix} \end{aligned} \quad (5.21)$$

where the coefficient matrices are

$$\begin{aligned} \mathbf{L}_{i1} &= \begin{bmatrix} K_p(1 + K_i T_s) & \omega_r L_{tot} \\ -\omega_r L_{tot} & K_p(1 + K_i T_s) \end{bmatrix}, \mathbf{L}_{ePI} = \begin{bmatrix} K_p & 0 \\ 0 & K_p \end{bmatrix}, \mathbf{L}_{yPI} = \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \\ \mathbf{L}_{u2} &= \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}, \mathbf{L}_r = \begin{bmatrix} -K_p(1 + K_i T_s) & 0 \\ 0 & -K_p(1 + K_i T_s) \end{bmatrix} \end{aligned}$$

Furthermore, the PI controllers are defined as follows:

$$\begin{bmatrix} e_{PI d}(k) \\ e_{PI q}(k) \end{bmatrix} = \overbrace{\begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix}}^{=\mathbf{M}_{i1}} \begin{bmatrix} i_{1d}(k) \\ i_{1q}(k) \end{bmatrix} + \overbrace{\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}}^{=\mathbf{M}_r} \begin{bmatrix} i_{1d}^*(k) \\ i_{1q}^*(k) \end{bmatrix} \quad (5.22)$$

$$\begin{aligned} \begin{bmatrix} y_{PI d}(k) \\ y_{PI q}(k) \end{bmatrix} &= \overbrace{\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}}^{=\mathbf{L}_r} \begin{bmatrix} i_{1d}(k) \\ i_{1q}(k) \end{bmatrix} + \overbrace{\begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix}}^{=-\mathbf{L}_{ePI}} \begin{bmatrix} e_{PI d}(k-1) \\ e_{PI q}(k-1) \end{bmatrix} \\ &+ \overbrace{\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}}^{=\mathbf{N}_{yPI}} \begin{bmatrix} y_{PI d}(k-1) \\ y_{PI q}(k-1) \end{bmatrix} + \overbrace{\begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix}}^{=-\mathbf{L}_r} \begin{bmatrix} i_{1d}^*(k) \\ i_{1q}^*(k) \end{bmatrix} \end{aligned} \quad (5.23)$$

¹In this study, standard form PI controllers $G_{PI}(s) = K_p \left(1 + \frac{1}{T_i} \frac{1}{s}\right)$ are used. The controllers are discretised using the Backward Euler method: $s \approx \frac{z-1}{T_s z}$.

The discrete-time closed-loop model is obtained by substituting (5.21)-(5.23) in (5.12)-(5.13), which yields

$$\begin{bmatrix} \mathbf{x}(k+1) \\ \mathbf{u}(k) \\ \mathbf{e}_{\text{PI}}(k) \\ \mathbf{y}_{\text{PI}}(k) \end{bmatrix} = \begin{bmatrix} \mathbf{\Phi} & \mathbf{\Gamma}_u & \mathbf{0} & \mathbf{0} \\ \mathbf{L}_x & \mathbf{L}_u & \mathbf{L}_{\text{ePI}} & \mathbf{L}_{\text{yPI}} \\ \mathbf{M}_x & \mathbf{M}_u & \mathbf{0} & \mathbf{0} \\ \mathbf{N}_x & \mathbf{N}_u & \mathbf{N}_{\text{ePI}} & \mathbf{N}_{\text{yPI}} \end{bmatrix} \begin{bmatrix} \mathbf{x}(k) \\ \mathbf{u}(k-1) \\ \mathbf{e}_{\text{PI}}(k-1) \\ \mathbf{y}_{\text{PI}}(k-1) \end{bmatrix} + \begin{bmatrix} \mathbf{\Gamma}_w & \mathbf{0} \\ \mathbf{L}_w & \mathbf{L}_r \\ \mathbf{M}_w & \mathbf{M}_r \\ \mathbf{N}_w & \mathbf{N}_r \end{bmatrix} \begin{bmatrix} \mathbf{w}(k) \\ \mathbf{r}(k) \end{bmatrix} \quad (5.24)$$

$$\mathbf{u}(k) = [u_{1d}^*(k) \quad u_{1q}^*(k)]^T \quad (5.25)$$

$$\mathbf{e}_{\text{PI}}(k) = [e_{\text{PI}d}(k) \quad e_{\text{PI}q}(k)]^T \quad (5.26)$$

$$\mathbf{y}_{\text{PI}}(k) = [y_{\text{PI}d}(k) \quad y_{\text{PI}q}(k)]^T \quad (5.27)$$

$$\mathbf{w}(k) = [u_{gd}(k) \quad u_{gq}(k)]^T \quad (5.28)$$

$$\mathbf{r}(k) = [i_{1d}^*(k) \quad i_{1q}^*(k)]^T \quad (5.29)$$

The coefficient matrices are developed in line with (5.15)-(5.17) and can be expressed as

$$\mathbf{L}_x = \mathbf{L}_{i1} \mathbf{K}_{i1-x} + \mathbf{L}_{u2} \mathbf{K}_{u2-x} \quad (5.30)$$

$$\mathbf{L}_u = \overbrace{\mathbf{L}_{u1}}^{=0} + \mathbf{L}_{i1} \mathbf{K}_{i1-u} + \mathbf{L}_{u2} \mathbf{K}_{u2-u} \quad (5.31)$$

$$\mathbf{L}_w = \mathbf{L}_{i1} \mathbf{K}_{i1-w} + \mathbf{L}_{u2} \mathbf{K}_{u2-w} \quad (5.32)$$

$$\mathbf{M}_x = \mathbf{M}_{i1} \mathbf{K}_{i1-x} + \overbrace{\mathbf{M}_{u2}}^{=0} \mathbf{K}_{u2-x} \quad (5.33)$$

$$\mathbf{M}_u = \overbrace{\mathbf{M}_{u1}}^{=0} + \mathbf{M}_{i1} \mathbf{K}_{i1-u} + \overbrace{\mathbf{M}_{u2}}^{=0} \mathbf{K}_{u2-u} \quad (5.34)$$

$$\mathbf{M}_w = \mathbf{M}_{i1} \mathbf{K}_{i1-w} + \overbrace{\mathbf{M}_{u2}}^{=0} \mathbf{K}_{u2-w} \quad (5.35)$$

$$\mathbf{N}_x = \mathbf{N}_{i1} \mathbf{K}_{i1-x} + \overbrace{\mathbf{N}_{u2}}^{=0} \mathbf{K}_{u2-x} \quad (5.36)$$

$$\mathbf{N}_u = \overbrace{\mathbf{N}_{u1}}^{=0} + \mathbf{N}_{i1} \mathbf{K}_{i1-u} + \overbrace{\mathbf{N}_{u2}}^{=0} \mathbf{K}_{u2-u} \quad (5.37)$$

$$\mathbf{N}_w = \mathbf{N}_{i1} \mathbf{K}_{i1-w} + \overbrace{\mathbf{N}_{u2}}^{=0} \mathbf{K}_{u2-w} \quad (5.38)$$

5.3.2 Stability and dynamic behaviour

The closed current control loop is studied using two system models. In the case of *RL model*, the filter inductors are modelled with *RL* series elements, as described in Section 3.2. In the case of *Foster model*, the filter inductors are modelled with third-order Foster equivalent circuits, as described in Section 3.3. The both models assume an ideal three-phase grid.

Fig. 5.3 illustrates the loci of the closed-loop poles when the proportional gains of the controllers are varied. The cross-coupling compensation is parametrised assuming nominal filter inductances, the integral gain is $K_i = 40$, and $T_s = 1/3600$ s. In Fig. 5.3(a), the resonant poles are close to the unit circle and, therefore, oscillatory responses can be expected. The damping of the resonant poles is higher in Fig. 5.3(b) because the resistances of the inductors' Foster equivalent circuits increase with frequency. The proportional gains $K_p = 3.25$ are selected for further investigation. The resulting pole locations are indicated with \times 's in Fig. 5.3.

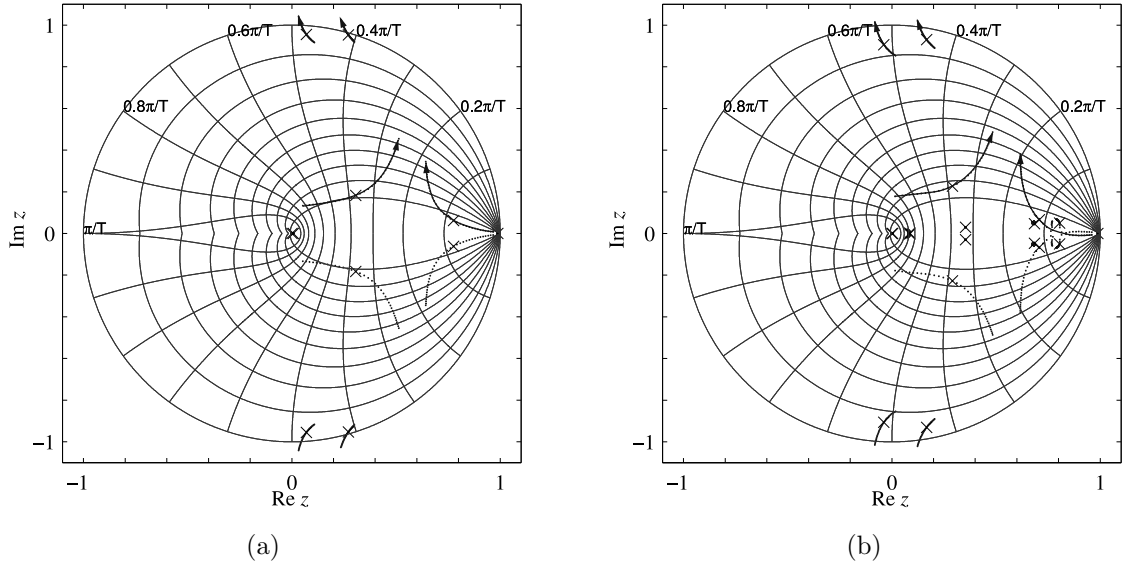


Fig. 5.3: Loci of the closed-loop poles when $K_p \in [0.72, 7.2]$. (a) *RL* model, (b) Foster model.

Fig. 5.4(a) depicts the responses $I_{1d}(e^{j\omega T_s})/I_{1d}^*(e^{j\omega T_s})$ and $I_{1q}(e^{j\omega T_s})/I_{1q}^*(e^{j\omega T_s})$ with the *RL* model. The magnitude responses peak at the *LCL* filter resonance. The control bandwidth read from the -3 dB point is approximately 155 Hz. The Foster model responses are shown in Fig. 5.4(b). The resistances of the filter inductors increase with frequency and they provide more damping at the *LCL* filter resonance. The control bandwidth is approximately 160 Hz.

Fig. 5.5 presents the admittances $I_{2d}(e^{j\omega T_s})/U_{2d}(e^{j\omega T_s})$ and $I_{2q}(e^{j\omega T_s})/U_{2q}(e^{j\omega T_s})$. The responses of the *RL* model peak around 700-900 Hz. Therefore, the voltage harmonics matching that frequency range would cause grid current oscillations. The magnitudes $|I_{2d}(e^{j\omega T_s})/U_{2d}(e^{j\omega T_s})|_{dB}$ of the both models reach -20 dB near 300 Hz which corresponds to the 5th and the 7th harmonics in the synchronous reference frame. As a result, the control can not generate purely sinusoidal currents if the grid voltage contains low order harmonics.

Finally, the step-change responses of the *q*-axis current are simulated using Simulink and SimPowerSystems toolbox. The average closed-loop model is simulated in parallel with the instantaneous STATCOM model described in Appendix D. Figs. 5.6(a) and 5.6(b) present the step responses of the *RL* model. The *LCL* filter resonance

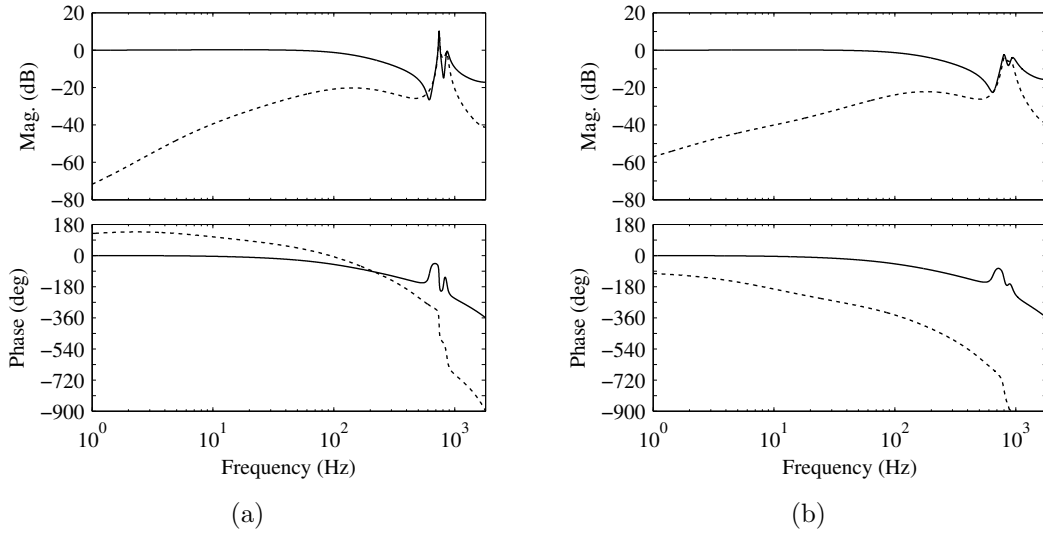


Fig. 5.4: (a) Responses of the RL model: $I_{1d}(e^{j\omega T_s})/I_{1d}^*(e^{j\omega T_s})$ (solid line), $I_{1d}(e^{j\omega T_s})/I_{1q}^*(e^{j\omega T_s})$ (dotted line). (b) Responses of the Foster model: $I_{1d}(e^{j\omega T_s})/I_{1d}^*(e^{j\omega T_s})$ (solid line), $I_{1d}(e^{j\omega T_s})/I_{1q}^*(e^{j\omega T_s})$ (dotted line).

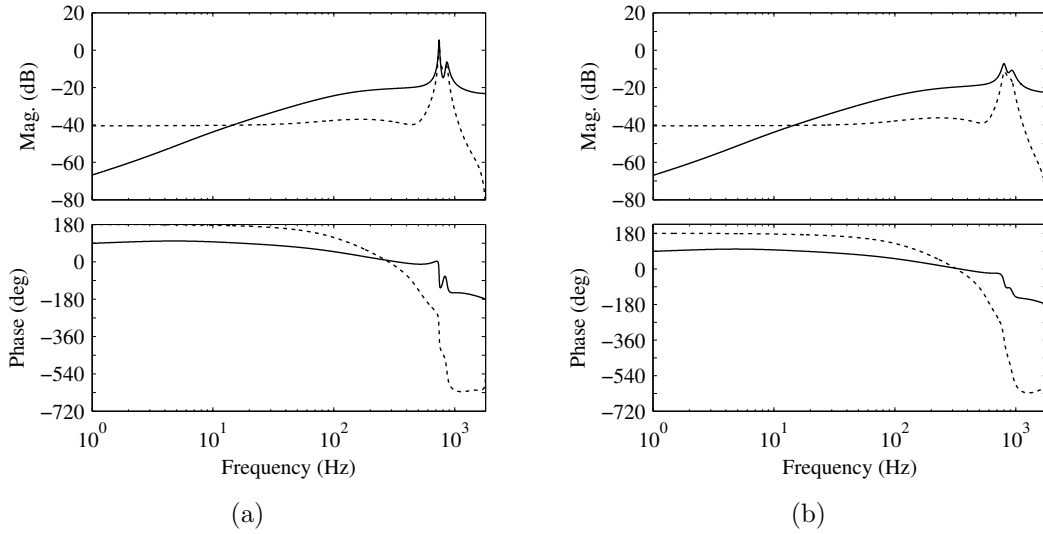


Fig. 5.5: (a) Responses of the RL model: $I_{2d}(e^{j\omega T_s})/U_{2d}(e^{j\omega T_s})$ (solid line), $I_{2d}(e^{j\omega T_s})/U_{2q}(e^{j\omega T_s})$ (dotted line). (b) Responses of the Foster model: $I_{2d}(e^{j\omega T_s})/U_{2d}(e^{j\omega T_s})$ (solid line), $I_{2d}(e^{j\omega T_s})/U_{2q}(e^{j\omega T_s})$ (dotted line).

causes oscillations as deduced based on the frequency responses. Figs. 5.6(c) and 5.6(d) show that the responses of the Foster model are more damped which is caused by the resistive characteristics of the third-order Foster models. The responses of the analytical models and the instantaneous model match with a good accuracy. Based on the results, if the control analysis was fully based on the RL model, the experimental STATCOM may show more stable behaviour than expected. In Fig. 5.6(c), the sampled rectifier currents in the Simulink simulation oscillate at half the sampling frequency. The sampling instants do not match with the exact zero-

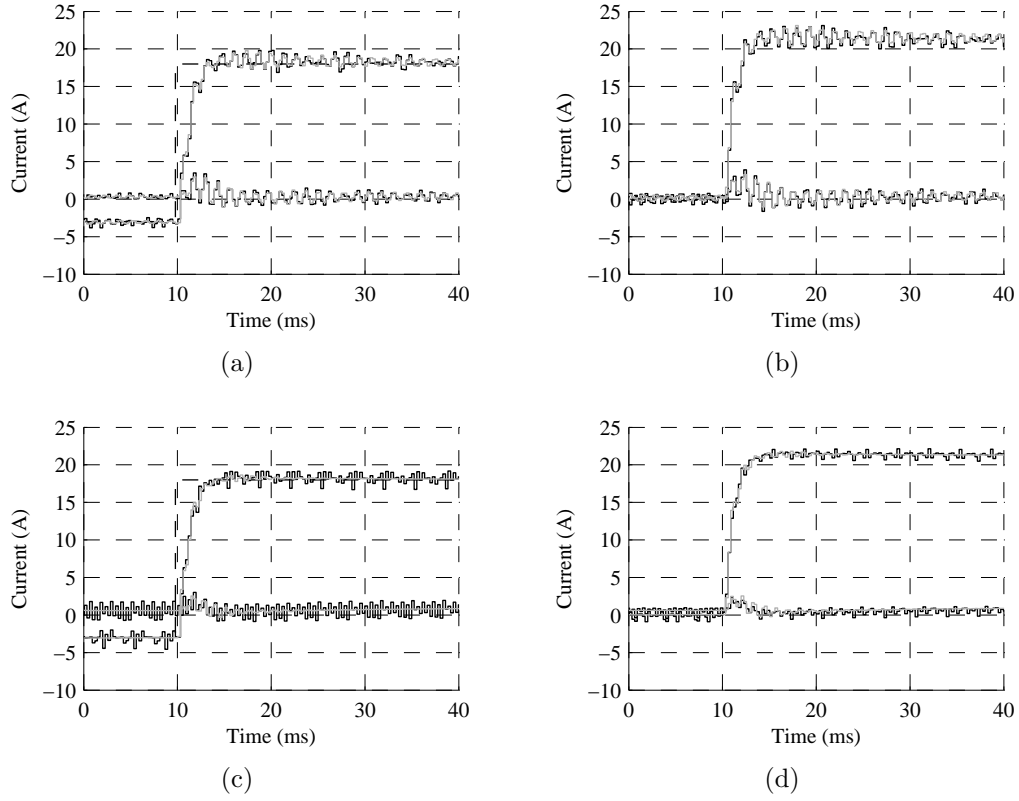


Fig. 5.6: Simulated q -axis current step responses. Gray solid line: response of the average model, Black solid line: response of the Simulink model, Dashed line: i_{1q}^* . (a) Rectifier current and (b) grid current when the inductors are modelled with series RL elements. (c) Rectifier current and (d) grid current when the inductors are modelled with Foster equivalent circuits.

crossings of the ripple current waveform and, therefore, a portion of the switching ripple is included in the sampled current.

5.4 Predictive vector current control

The block scheme of the studied predictive vector current controller is depicted in Fig. 5.7, where $Z_{L1} = R_1 + j\omega_r L_1$, $Z_{L2} = R_2 + j\omega_r L_2$, $Z_{L3} = R_3 + j\omega_r L_3$, and $Z_{C3} = 1/j\omega_r C_3$. Similarly as in [189], the controller has a cascade structure and a PI controller is included in the outermost loop to compensate the steady-state grid current error. Only the grid voltages and the rectifier currents are measured. The remaining unknown state variables are estimated to prevent increasing the number of required sensor hardware.

The controller is derived by approximating the differential circuit equations of the LCL filter circuit by using the Forward Euler method

$$\dot{x}(t) \approx \frac{x(t + T_s) - x(t)}{T_s} \quad (5.39)$$

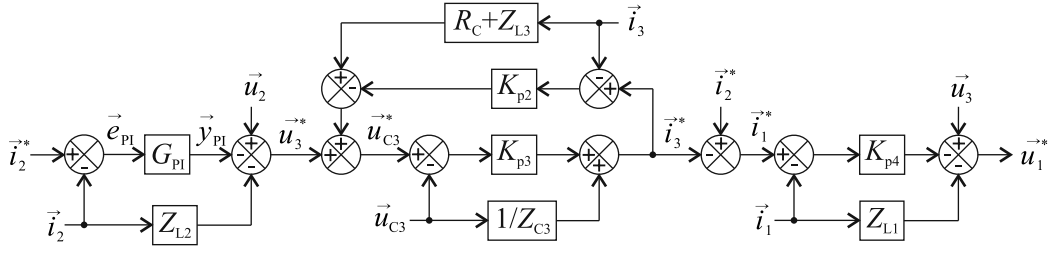


Fig. 5.7: Block scheme of the predictive vector current controller.

For sake of simplicity, the damping resistors R_d are neglected, because their effect below the LCL filter resonance and within the control bandwidth is small. Hence, it is assumed that $i_{31k} \approx i_{3k}$. When the Forward Euler method is applied to (3.6)-(3.10), the following difference equations are obtained:

$$\vec{u}_2(k) - \vec{u}_3(k) = \frac{L_2}{T_s} \left(\vec{i}_2(k+1) - \vec{i}_2(k) \right) + (R_2 + j\omega_r L_2) \vec{i}_2(k) \quad (5.40)$$

$$\vec{u}_3(k) - \vec{u}_{C3}(k) = \frac{L_3}{T_s} \left(\vec{i}_3(k+1) - \vec{i}_3(k) \right) + (R_3 + R_C + j\omega_r L_3) \vec{i}_3(k) \quad (5.41)$$

$$\vec{i}_3(k) = \frac{C_3}{T_s} (\vec{u}_{C3}(k+1) - \vec{u}_{C3}(k)) + j\omega_r C_3 \vec{u}_{C3}(k) \quad (5.42)$$

$$\vec{u}_3(k) - \vec{u}_1(k) = \frac{L_1}{T_s} \left(\vec{i}_1(k+1) - \vec{i}_1(k) \right) + (R_1 + j\omega_r L_1) \vec{i}_1(k) \quad (5.43)$$

$$\begin{aligned} \vec{u}_3(k) = & c \left(\frac{L_3}{L_1} R_1 - R_C - R_3 \right) \vec{i}_1(k) + c \left(R_C + R_3 - \frac{L_3}{L_2} R_2 \right) \vec{i}_2(k) \\ & + c \vec{u}_{C3}(k) + c \frac{L_3}{L_1} \vec{u}_1(k) + c \frac{L_3}{L_2} \vec{u}_2(k) \end{aligned} \quad (5.44)$$

$$c = \frac{L_1 L_2}{L_1 L_2 + L_2 L_3 + L_1 L_3} \quad (5.45)$$

Next, the voltages and the currents of sampling instant $t = (k + 1)T_s$ are considered as references. The grid current error $\vec{i}_2^*(k) - \vec{i}_2(k)$ is compensated with standard form PI controllers that are discretised using the Backward Euler method. As a result, the following equations are obtained

$$\vec{y}_{\text{PI}}(k) = K_{\text{pI}}(1 + K_{\text{i}}T_{\text{s}}) \overbrace{\left(\vec{i}_2^*(k) - \vec{i}_2(k) \right)}^{=\vec{e}_{\text{PI}}(k)} + \vec{y}_{\text{PI}}(k-1) - K_{\text{pI}}\vec{e}_{\text{PI}}(k-1) \quad (5.46)$$

$$\vec{u}_3^*(k) = \vec{u}_2(k) - (R_2 + j\omega_r L_2) \vec{i}_2(k) - \vec{y}_{\text{PI}}(k) \quad (5.47)$$

$$\vec{u}_{C3}^*(k) = \vec{u}_3^*(k) - K_{p2} \left(\vec{i}_3^*(k) - \vec{i}_3(k) \right) + (R_3 + R_C + j\omega_r L_3) \vec{i}_3(k) \quad (5.48)$$

$$\vec{i}_3^*(k) = K_{p3} (\vec{u}_{C3}^*(k) - \vec{u}_{C3}(k)) + j\omega_r C_3 \vec{u}_{C3}(k) \quad (5.49)$$

$$\vec{u}_1^*(k) = \vec{u}_3(k) - K_{\text{p4}} \left(\vec{i}_1^*(k) - \vec{i}_1(k) \right) - (R_1 + \text{j}\omega_{\text{r}}L_1) \vec{i}_1(k) \quad (5.50)$$

where the proportional gains K_{p1} , K_{p2} , K_{p3} , and K_{p4} are defined as follows

$$K_{p1} = K_{i2} \frac{L_2}{T_s}, K_{p2} = K_{i3} \frac{L_3}{T_s}, K_{p3} = K_{u3} \frac{C_3}{T_s}, K_{p4} = K_{i1} \frac{L_1}{T_s} \quad (5.51)$$

where K_{i2} , K_{i3} , K_{uC3} , and K_{i1} are the tuning coefficients.

Finally, the voltage reference $\vec{u}_1^*(k)$ can be solved by combining (5.46)-(5.50). The current reference present in (5.50) can be solved by taking into account that $\vec{i}_3(k) = \vec{i}_2(k) - \vec{i}_1(k)$. Furthermore, the voltage $\vec{u}_3(k)$ present in (5.50) can be solved from (5.44) by substituting $\vec{u}_1(k) = \vec{u}_1^*(k-1)$. The voltage reference $\vec{u}_1^*(k)$ can be expressed as

$$\begin{aligned}
\vec{u}_1^*(k) = & \overbrace{\left[K_{p4} - R_1 - c(R_C + R_3 - \frac{L_3}{L_1}R_1) - j\omega_r L_1 \right]}^{=L_{i1}} \vec{i}_1(k) \\
& + \overbrace{\left[c(R_C + R_3 - \frac{L_3}{L_2}R_2) - \frac{K_{p3}K_{p4}}{K_{p2}K_{p3} + 1}(R_2 - K_{p1}(1 + K_i T_s) + j\omega_r L_2) \right]}^{=L_{i2}} \vec{i}_2(k) \\
& + \overbrace{\left[\frac{K_{p3}K_{p4}}{K_{p2}K_{p3} + 1}(K_{p2} - R_C - R_3 - j\omega_r L_3) \right]}^{=L_{i3}} \vec{i}_3(k) \\
& + \overbrace{\left[c + \frac{K_{p3}K_{p4}}{K_{p2}K_{p3} + 1}(-1 + j\omega_r \frac{C_3}{K_{p3}}) \right]}^{=L_{uC3}} \vec{u}_{C3}(k) + \overbrace{\left[c \frac{L_3}{L_1} \right]}^{=L_{u1}} \vec{u}_1^*(k-1) \\
& + \overbrace{\left[\frac{K_{p3}K_{p4}}{K_{p2}K_{p3} + 1}K_{p1} \right]}^{=L_{ePI}} \vec{e}_{PI}(k-1) + \overbrace{\left[\frac{-K_{p3}K_{p4}}{K_{p2}K_{p3} + 1} \right]}^{=L_{yPI}} \vec{y}_{PI}(k-1) \\
& + \overbrace{\left[\frac{K_{p3}K_{p4}}{K_{p2}K_{p3} + 1} + c \frac{L_3}{L_2} \right]}^{=L_{u2}} \vec{u}_2(k) + \overbrace{\left[-\frac{K_{p3}K_{p4}}{K_{p2}K_{p3} + 1}K_{p1}(1 + K_i T_s) - K_{p4} \right]}^{=L_r} \vec{i}_2^*(k)
\end{aligned} \tag{5.52}$$

To develop the closed-loop model, the control law (5.52) is separated into d and q axis components and expressed in the following form

$$\begin{aligned}
\begin{bmatrix} u_{1d}^*(k) \\ u_{1q}^*(k) \end{bmatrix} = & \mathbf{L}_{i1} \begin{bmatrix} i_{1d}(k) \\ i_{1q}(k) \end{bmatrix} + \mathbf{L}_{i2} \begin{bmatrix} i_{2d}(k) \\ i_{2q}(k) \end{bmatrix} + \mathbf{L}_{i3} \begin{bmatrix} i_{3d}(k) \\ i_{3q}(k) \end{bmatrix} + \mathbf{L}_{uC3} \begin{bmatrix} u_{C3d}(k) \\ u_{C3q}(k) \end{bmatrix} \\
& + \mathbf{L}_{u1} \begin{bmatrix} u_{1d}^*(k-1) \\ u_{1q}^*(k-1) \end{bmatrix} + \mathbf{L}_{ePI} \begin{bmatrix} e_{PI d}(k-1) \\ e_{PI q}(k-1) \end{bmatrix} + \mathbf{L}_{yPI} \begin{bmatrix} y_{PI d}(k-1) \\ y_{PI q}(k-1) \end{bmatrix} \\
& + \mathbf{L}_{u2} \begin{bmatrix} u_{2d}(k) \\ u_{2q}(k) \end{bmatrix} + \mathbf{L}_r \begin{bmatrix} i_{2d}^*(k) \\ i_{2q}^*(k) \end{bmatrix}
\end{aligned} \tag{5.53}$$

where \mathbf{L}_{i1} , \mathbf{L}_{i2} , \mathbf{L}_{i3} , \mathbf{L}_{uC3} , \mathbf{L}_{u1} , \mathbf{L}_{ePI} , \mathbf{L}_{yPI} , \mathbf{L}_{u2} , and \mathbf{L}_r denote the control coefficient matrices. For example, \mathbf{L}_{i1} is defined as follows:

$$\mathbf{L}_{i1} = \begin{bmatrix} \text{Re}\{L_{i1}\} & -\text{Im}\{L_{i1}\} \\ \text{Im}\{L_{i1}\} & \text{Re}\{L_{i1}\} \end{bmatrix} \tag{5.54}$$

Furthermore, the PI controllers are defined as follows:

$$\begin{bmatrix} e_{PI_d}(k) \\ e_{PI_q}(k) \end{bmatrix} = \overbrace{\begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix}}^{=M_{i2}} \begin{bmatrix} i_{2d}(k) \\ i_{2q}(k) \end{bmatrix} + \overbrace{\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}}^{=M_r} \begin{bmatrix} i_{2d}^*(k) \\ i_{2q}^*(k) \end{bmatrix} \quad (5.55)$$

$$\begin{aligned} \begin{bmatrix} y_{PI_d}(k) \\ y_{PI_q}(k) \end{bmatrix} &= \overbrace{\begin{bmatrix} -K_{p1}(1 + K_i T_s) & 0 \\ 0 & -K_{p1}(1 + K_i T_s) \end{bmatrix}}^{=N_{i2}} \begin{bmatrix} i_{2d}(k) \\ i_{2q}(k) \end{bmatrix} \\ &+ \overbrace{\begin{bmatrix} -K_{p1} & 0 \\ 0 & -K_{p1} \end{bmatrix}}^{=N_{ePI}} \begin{bmatrix} e_{PI_d}(k-1) \\ e_{PI_q}(k-1) \end{bmatrix} + \overbrace{\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}}^{=N_{yPI}} \begin{bmatrix} y_{PI_d}(k-1) \\ y_{PI_q}(k-1) \end{bmatrix} + \overbrace{\begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}}^{=-N_{i2}} \begin{bmatrix} i_{2d}^*(k) \\ i_{2q}^*(k) \end{bmatrix} \end{aligned} \quad (5.56)$$

5.4.1 State observer

The studied predictive controller requires the information on all system states. However, only the grid voltages and the rectifier currents are measured. The unmeasured states are estimated using the reduced-order observer depicted in Fig. 5.8.

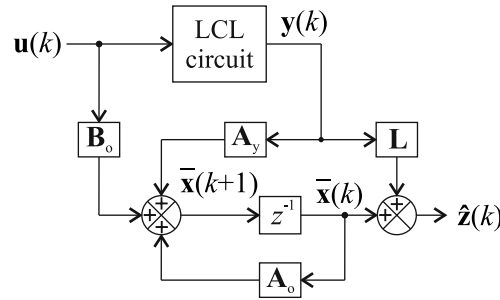


Fig. 5.8: Block scheme of the reduced-order observer.

To develop the observer, the coefficient matrices Φ and $\Gamma = [\Gamma_u \quad \Gamma_w]$ of the process model are separated for the available measurements $\mathbf{y}(k)$ and the unknown states $\mathbf{z}(k)$ that are to be estimated, yielding

$$\begin{bmatrix} \mathbf{y}(k+1) \\ \mathbf{z}(k+1) \end{bmatrix} = \begin{bmatrix} \Phi_{11} & \Phi_{12} \\ \Phi_{21} & \Phi_{22} \end{bmatrix} \begin{bmatrix} \mathbf{y}(k) \\ \mathbf{z}(k) \end{bmatrix} + \begin{bmatrix} \Gamma_1 \\ \Gamma_2 \end{bmatrix} \mathbf{u}(k) \quad (5.57)$$

$$\mathbf{y}(k) = [i_{1d}(k) \quad i_{1q}(k)]^T \quad (5.58)$$

$$\mathbf{z}(k) = [i_{2d}(k) \quad i_{2q}(k) \quad i_{31d}(k) \quad i_{31q}(k) \quad u_{C3d}(k) \quad u_{C3q}(k)]^T \quad (5.59)$$

$$\mathbf{u}(k) = [u_{1d}^*(k-1) \quad u_{1q}^*(k-1) \quad u_{2d}(k) \quad u_{2q}(k)]^T \quad (5.60)$$

Based on (5.57), the portion of the known states that is affected by the unknown states $\mathbf{z}(k)$ is

$$\mathbf{y}_z(k) = \mathbf{y}(k+1) - \Phi_{11}\mathbf{y}(k) - \Gamma_1\mathbf{u}(k) = \Phi_{12}\mathbf{z}(k) \quad (5.61)$$

The estimate of the unknown partial state vector $\mathbf{z}(k)$ can be expressed as

$$\hat{\mathbf{z}}(k+1) = \Phi_{21}\mathbf{y}(k) + \Phi_{22}\hat{\mathbf{z}}(k) + \Gamma_2\mathbf{u}(k) + \mathbf{L}(\mathbf{y}_z(k) - \Phi_{12}\hat{\mathbf{z}}(k)) \quad (5.62)$$

which includes the feedback from the error in the computation of $\mathbf{y}_z(k)$. \mathbf{L} is the observer gain matrix. Substitution of (5.61) in (5.62) yields the term $\mathbf{L}\mathbf{y}(k+1)$ which is not available when $\mathbf{y}(k)$ is sampled. Therefore, a variable change is made to estimate $\bar{\mathbf{x}}(k) = \hat{\mathbf{z}}(k) - \mathbf{L}\mathbf{y}(k)$ instead of $\hat{\mathbf{z}}(k)$. The resulting reduced-order observer corresponds to the block scheme depicted in Fig. 5.8 and can be expressed as follows:

$$\bar{\mathbf{x}}(k+1) = \hat{\mathbf{z}}(k+1) - \mathbf{L}\mathbf{y}(k+1) \quad (5.63a)$$

$$= \underbrace{(\Phi_{22} - \mathbf{L}\Phi_{12})}_{\mathbf{A}_o} \bar{\mathbf{x}}(k) + \underbrace{(\Gamma_2 - \mathbf{L}\Gamma_1)}_{\mathbf{B}_o} \mathbf{u}(k) + \underbrace{(\Phi_{21} - \mathbf{L}\Phi_{11} + \Phi_{22}\mathbf{L} - \mathbf{L}\Phi_{12}\mathbf{L})}_{\mathbf{A}_y} \mathbf{y}(k) \quad (5.63b)$$

$$= \mathbf{A}_o \bar{\mathbf{x}}(k) + [\mathbf{B}_o^u \quad \mathbf{B}_o^w] \mathbf{u}(k) + \mathbf{A}_y \mathbf{y}(k) \quad (5.63c)$$

Finally, the state vector including both the measured and the estimated variables is

$$\begin{bmatrix} \mathbf{y}(k) \\ \hat{\mathbf{z}}(k) \end{bmatrix} = \begin{bmatrix} \mathbf{y}(k) \\ \mathbf{L}\mathbf{y}(k) + \bar{\mathbf{x}}(k) \end{bmatrix} \quad (5.64)$$

The process model of the observer is obtained by discretising (3.15)-(3.19) as described in Section 5.2. The observer gain matrix \mathbf{L} determines the poles of \mathbf{A}_o which govern the observer's dynamic behaviour. As a rule of thumb, the poles should be 4 to 10 times faster than the controller poles [188]. In this thesis, the poles are placed on the real axis at $p_{1,2} = 0.2$, $p_{3,4} = 0.21$, and $p_{5,6} = 0.22$ based on the behaviour of Simulink simulations and preliminary laboratory tests. The gain matrix is solved numerically using the *place* command provided in Matlab Control System Toolbox. The observer is developed using the nominal values of the *LCL* circuit. The inductors' equivalent series resistances are parametrised according to the impedance measurements presented in Appendix C.

5.4.2 Closed-loop model

The closed-loop model of the predictive vector current control is developed in line with Section 5.2, and can be expressed as follows

$$\begin{bmatrix} \mathbf{x}(k+1) \\ \bar{\mathbf{x}}(k+1) \\ \mathbf{u}(k) \\ \mathbf{e}_{\text{PI}}(k) \\ \mathbf{y}_{\text{PI}}(k) \end{bmatrix} = \begin{bmatrix} \Phi & \mathbf{0} & \Gamma_u & \mathbf{0} & \mathbf{0} \\ \mathbf{A}_x & \mathbf{A}_o & \mathbf{B}_u & \mathbf{0} & \mathbf{0} \\ \mathbf{L}_x & \mathbf{L}_o & \mathbf{L}_u & \mathbf{L}_{\text{ePI}} & \mathbf{L}_{\text{yPI}} \\ \mathbf{M}_x & \mathbf{M}_o & \mathbf{M}_u & \mathbf{0} & \mathbf{0} \\ \mathbf{N}_x & \mathbf{N}_o & \mathbf{N}_u & \mathbf{N}_{\text{ePI}} & \mathbf{N}_{\text{yPI}} \end{bmatrix} \begin{bmatrix} \mathbf{x}(k) \\ \bar{\mathbf{x}}(k) \\ \mathbf{u}(k-1) \\ \mathbf{e}_{\text{PI}}(k-1) \\ \mathbf{y}_{\text{PI}}(k-1) \end{bmatrix} + \begin{bmatrix} \Gamma_w & \mathbf{0} \\ \mathbf{B}_w & \mathbf{0} \\ \mathbf{L}_w & \mathbf{L}_r \\ \mathbf{M}_w & \mathbf{M}_r \\ \mathbf{N}_w & \mathbf{N}_r \end{bmatrix} \begin{bmatrix} \mathbf{w}(k) \\ \mathbf{r}(k) \end{bmatrix} \quad (5.65)$$

$$\mathbf{u}(k) = [u_{1d}^*(k) \quad u_{1q}^*(k)]^T \quad (5.66)$$

$$\mathbf{e}_{\text{PI}}(k) = [e_{\text{PI}d}(k) \quad e_{\text{PI}q}(k)]^T \quad (5.67)$$

$$\mathbf{y}_{\text{PI}}(k) = [y_{\text{PI}d}(k) \quad y_{\text{PI}q}(k)]^T \quad (5.68)$$

$$\mathbf{w}(k) = [u_{gd}(k) \quad u_{gq}(k)]^T \quad (5.69)$$

$$\mathbf{r}(k) = [i_{2d}^*(k) \quad i_{2q}^*(k)]^T \quad (5.70)$$

The estimate $\hat{\mathbf{z}}(k)$ of the unknown states is not readily available in the state vector of (5.65) because of the variable change performed in (5.63c). In line with (5.64), the estimated state variables are

$$\hat{\mathbf{z}}(k) = \mathbf{L}\mathbf{y}(k) + \bar{\mathbf{x}}(k) \quad (5.71)$$

$$\hat{\mathbf{z}}(k) = [\hat{i}_{2d}(k) \quad \hat{i}_{2q}(k) \quad \hat{i}_{31d}(k) \quad \hat{i}_{31q}(k) \quad \hat{u}_{\text{C3}d}(k) \quad \hat{u}_{\text{C3}q}(k)]^T \quad (5.72)$$

$$\mathbf{y}(k) = [i_{1d}(k) \quad i_{1q}(k)]^T \quad (5.73)$$

When (5.71) is considered, the coefficient matrices of the observer can be expressed as

$$\mathbf{A}_x = \mathbf{A}_y \mathbf{K}_{i1-x} + \mathbf{B}_o^w \mathbf{K}_{u2-x} \quad (5.74)$$

$$\mathbf{B}_u = \mathbf{B}_o^u + \mathbf{A}_y \mathbf{K}_{i1-u} + \mathbf{B}_o^w \mathbf{K}_{u2-u} \quad (5.75)$$

$$\mathbf{B}_w = \mathbf{A}_y \mathbf{K}_{i1-w} + \mathbf{B}_o^w \mathbf{K}_{u2-w} \quad (5.76)$$

the coefficient matrices of the control law can be expressed as

$$\mathbf{L}_x = (\mathbf{L}_{i1} + \mathbf{L}_o \mathbf{L}) \mathbf{K}_{i1-x} + \mathbf{L}_{u2} \mathbf{K}_{u2-x} \quad (5.77)$$

$$\mathbf{L}_o = [\mathbf{L}_{i2} \quad \mathbf{L}_{i3} \quad \mathbf{L}_{u\text{C3}}] \quad (5.78)$$

$$\mathbf{L}_u = \mathbf{L}_{u1} + (\mathbf{L}_{i1} + \mathbf{L}_o \mathbf{L}) \mathbf{K}_{i1-u} + \mathbf{L}_{u2} \mathbf{K}_{u2-u} \quad (5.79)$$

$$\mathbf{L}_w = (\mathbf{L}_{i1} + \mathbf{L}_o \mathbf{L}) \mathbf{K}_{i1-w} + \mathbf{L}_{u2} \mathbf{K}_{u2-w} \quad (5.80)$$

and the coefficient matrices of the PI controller can be expressed as

$$\mathbf{M}_x = (\overbrace{\mathbf{M}_{i1}}^{=0} + \mathbf{M}_o \mathbf{L}) \mathbf{K}_{i1-x} + \overbrace{\mathbf{M}_{u2}}^{=0} \mathbf{K}_{u2-x} \quad (5.81)$$

$$\mathbf{M}_o = [\mathbf{M}_{i2} \quad \mathbf{0} \quad \mathbf{0}] \quad (5.82)$$

$$\mathbf{M}_u = \overbrace{\mathbf{M}_{u1}}^{=0} + (\overbrace{\mathbf{M}_{i1}}^{=0} + \mathbf{M}_o \mathbf{L}) \mathbf{K}_{i1-u} + \overbrace{\mathbf{M}_{u2}}^{=0} \mathbf{K}_{u2-u} \quad (5.83)$$

$$\mathbf{M}_w = (\overbrace{\mathbf{M}_{i1}}^{=0} + \mathbf{M}_o \mathbf{L}) \mathbf{K}_{i1-w} + \overbrace{\mathbf{M}_{u2}}^{=0} \mathbf{K}_{u2-w} \quad (5.84)$$

$$\mathbf{N}_x = (\overbrace{\mathbf{N}_{i1}}^{=0} + \mathbf{N}_o \mathbf{L}) \mathbf{K}_{i1-x} + \overbrace{\mathbf{N}_{u2}}^{=0} \mathbf{K}_{u2-x} \quad (5.85)$$

$$\mathbf{N}_o = [\mathbf{N}_{i2} \quad \mathbf{0} \quad \mathbf{0}] \quad (5.86)$$

$$\mathbf{N}_u = \overbrace{\mathbf{N}_{u1}}^{=0} + (\overbrace{\mathbf{N}_{i1}}^{=0} + \mathbf{N}_o \mathbf{L}) \mathbf{K}_{i1-u} + \overbrace{\mathbf{N}_{u2}}^{=0} \mathbf{K}_{u2-u} \quad (5.87)$$

$$\mathbf{N}_w = (\overbrace{\mathbf{N}_{i1}}^{=0} + \mathbf{N}_o \mathbf{L}) \mathbf{K}_{i1-w} + \overbrace{\mathbf{N}_{u2}}^{=0} \mathbf{K}_{u2-w} \quad (5.88)$$

5.4.3 Stability and dynamic behaviour

The characteristics of the closed current control loop are studied by means of pole analysis and frequency response analysis. The dynamic behaviour is shown by means of step-response simulations. The analyses have been carried out using the two system models presented in Chapter 3 which assume zero network impedance. In the case of *RL model*, the filter inductors are modelled with *RL* series elements. Regarding the *Foster model*, the filter inductors are modelled with Foster equivalent circuits.

Figs. 5.9(a)-5.9(d) illustrate the pole loci when the proportional gains are varied. Nominal filter component values are assumed, the integral gains of the PI controllers are $K_i = 40$, and the sampling frequency is 3600 Hz. It can be seen that K_{i1} should be selected significantly lower than unity, or otherwise the poles move too close to the unstable region. The parameters K_{i3} and K_{uC3} have a minor effect on the slowest poles. As a result, the controller parameters $K_{i1} = 0.3$, $K_{i3} = K_{uC3} = 1$, and $K_{i2} = 0.2$ are selected for further investigation. The resulting pole locations are indicated with \times 's. It is important to notice that in Figs. 5.9(b) and 5.9(d) the observer poles have displaced from their designed locations and move when the controller parameters are varied.

The observer's sensitivity to parametric uncertainties compromises the controller feasibility if the dynamics can vary considerably or if it can even become unstable. Fig. 5.10 illustrates the loci of closed-loop poles of the *RL* model when the filter inductances are varied. The observer and the controller are parametrised by assuming the nominal filter component values. Based on the results, the mismatch of L_1 and L_2 have a strong effect on the observer poles while the effect of L_3 is minor. The overestimation of L_1 moves the resonance poles towards the unit circle and,

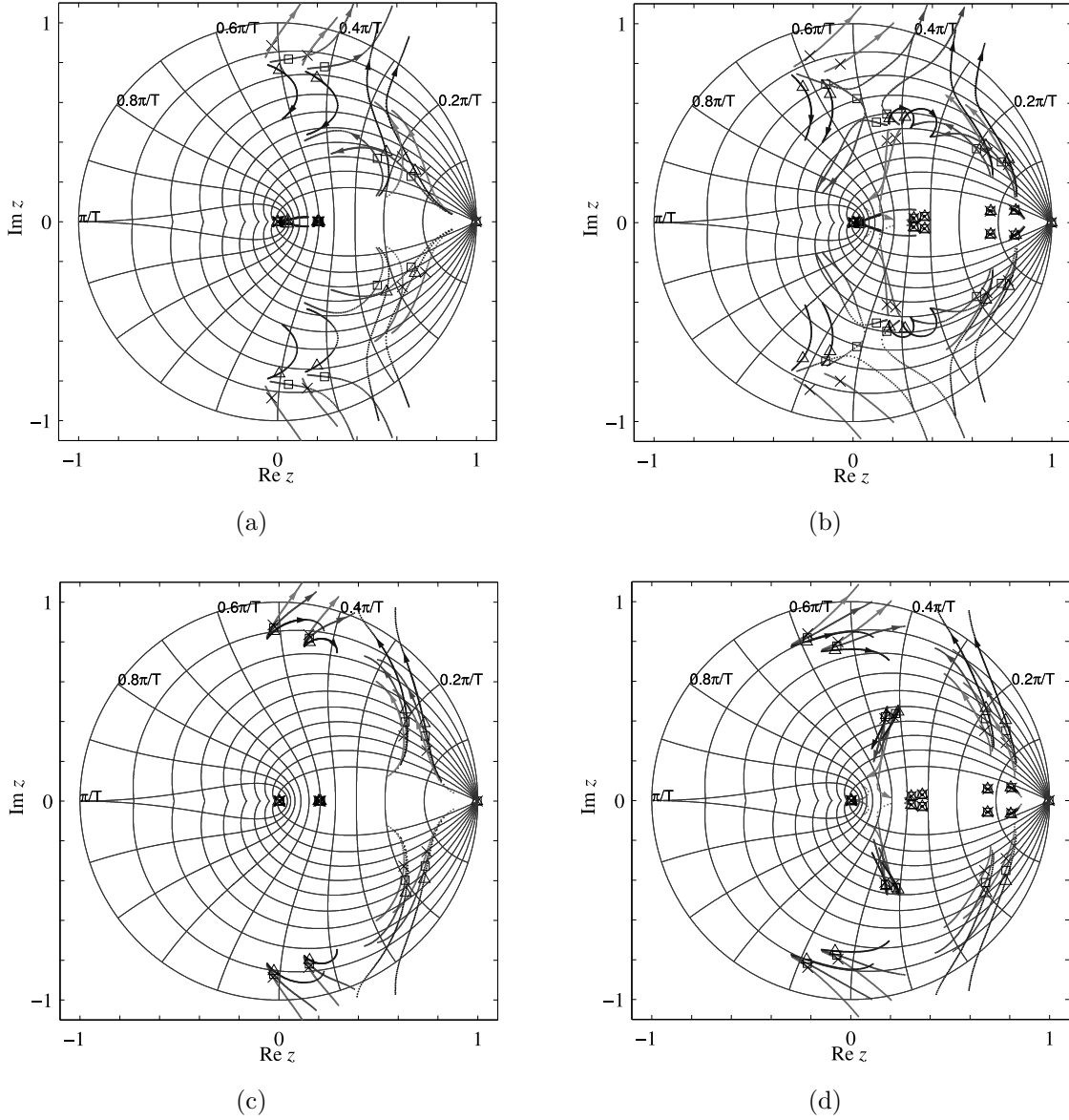


Fig. 5.9: Loci of the closed-loop poles when the proportional gains are varied. (a) RL model and (b) Foster model when $K_{i3} = K_{uc3} \in \{1, 4, 8\}$, $K_{i2} = 0.2$, and $K_{i1} \in [0.1, 1]$. (c) RL model and (d) Foster model when $K_{i2} \in \{0.2, 0.6, 1\}$, $K_{i3} = K_{uc3} = 1$, and $K_{i1} \in [0.1, 1]$. In (a) and (b), the poles at $K_{i1} = 0.3$ have been marked with crosses (\times) for $K_{i3} = K_{uc3} = 1$, with squares (\square) for $K_{i3} = K_{uc3} = 4$ and with triangles (\triangle) for $K_{i3} = K_{uc3} = 8$. In (c) and (d), the poles at $K_{i1} = 0.3$ have been marked with crosses (\times) for $K_{i2} = 0.2$, with squares (\square) for $K_{i2} = 0.6$ and with triangles (\triangle) for $K_{i2} = 1$.

eventually, to the unstable region. On the other hand, strong underestimation of L_1 and L_2 move two observer poles along the real axis towards point $(1,0)$, which implies that the settling time of the observer increases.

Fig. 5.11 illustrates the $I_{2d}(e^{j\omega T_s})/I_{2d}^*(e^{j\omega T_s})$ and $I_{2d}(e^{j\omega T_s})/I_{2q}^*(e^{j\omega T_s})$ responses of the two closed-loop models. The control bandwidth of the RL model is 350 Hz. In Fig. 5.11(b) the DC gain of $|I_{2d}(e^{j\omega T_s})/I_{2d}^*(e^{j\omega T_s})|_{dB}$ is -0.08 dB which leads to

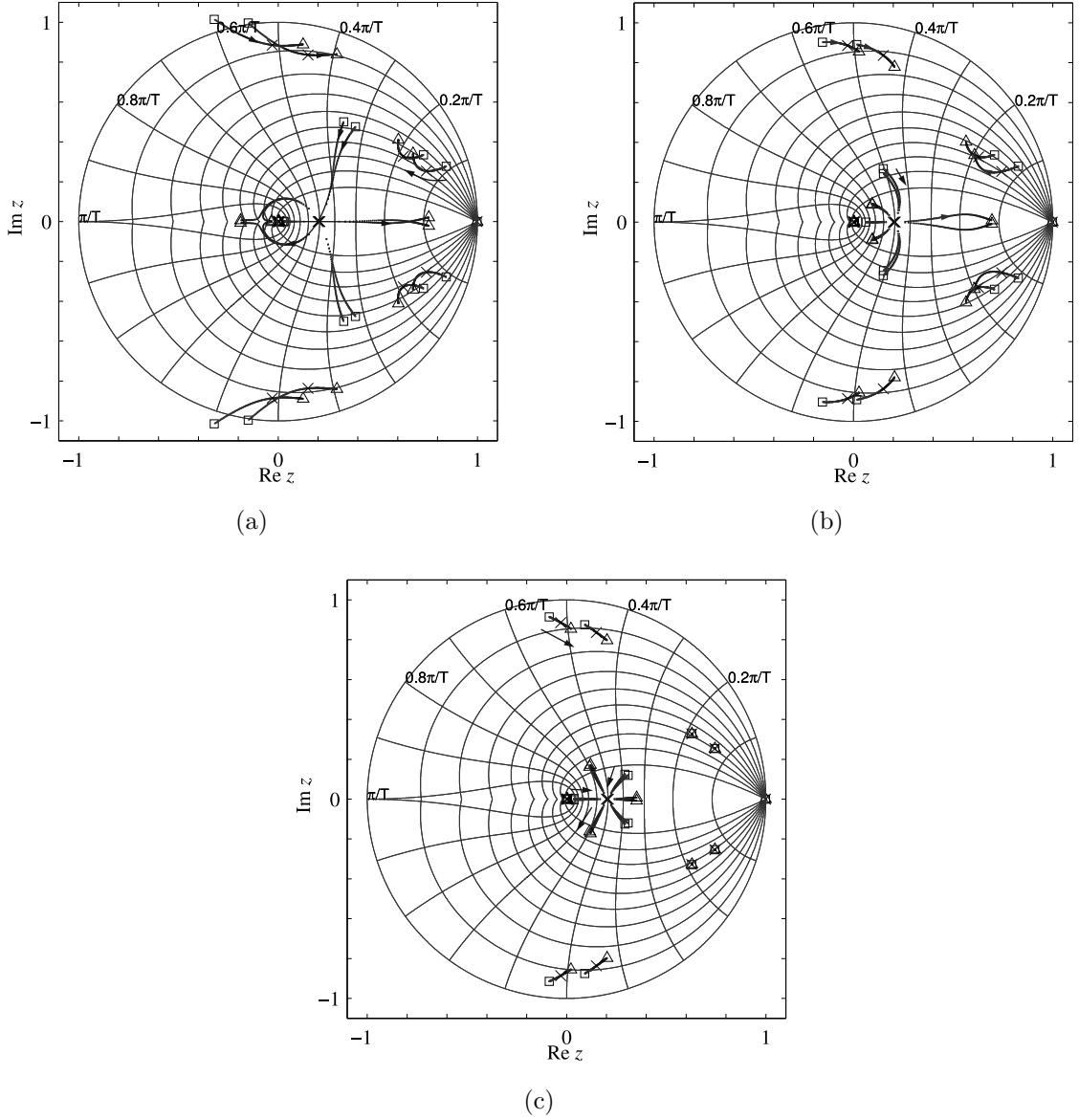


Fig. 5.10: The effect of filter inductor parameter mismatches on the closed-loop poles. (a) $L_1 \in [0.6L_{1,\text{nom}}, 1.4L_{1,\text{nom}}]$, (b) $L_2 \in [0.6L_{2,\text{nom}}, 1.4L_{2,\text{nom}}]$, (c) $L_3 \in [0.6L_{3,\text{nom}}, 1.4L_{3,\text{nom}}]$. The pole locations with -40% inductance are marked with squares (\square), with +40% with triangles (\triangle), and with nominal inductance with crosses (\times). The controllers are parametrised as follows: $K_{i1} = 0.3$, $K_{i2} = 0.2$, $K_{u\text{C}3} = K_{i3} = 1$.

ca. 1% steady-state error in the grid current. The control bandwidth of the Foster model is 360 Hz. Fig. 5.12 depicts the admittances $I_{2d}(e^{j\omega T_s})/U_{2d}(e^{j\omega T_s})$ and $I_{2q}(e^{j\omega T_s})/U_{2q}(e^{j\omega T_s})$. The magnitudes $|I_{2d}(e^{j\omega T_s})/U_{2d}(e^{j\omega T_s})|_{\text{dB}}$ near the 5th and the 7th harmonics are higher compared with the PI control strategy (see Fig. 5.5) which implies poorer capability to reject the background grid voltage distortion.

Fig. 5.13 presents the simulated responses to the step-change of the q -axis current reference. The average model is simulated in parallel with the instantaneous model. The responses correlate very well. The overshoot of the both models is ca. 14%. The

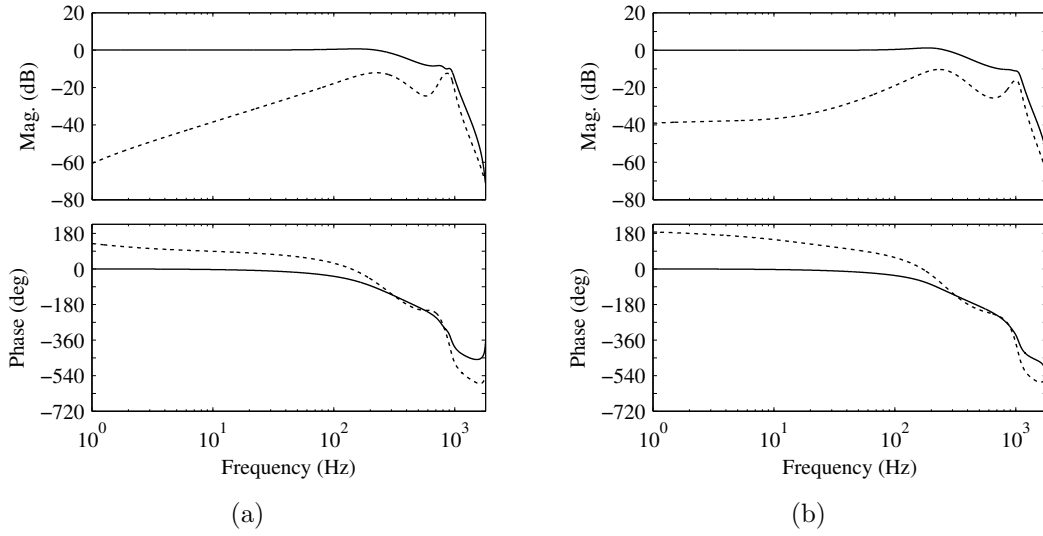


Fig. 5.11: (a) Responses of the RL model: $I_{2d}(e^{j\omega T_s})/I_{2d}^*(e^{j\omega T_s})$ (solid line), $I_{2d}(e^{j\omega T_s})/I_{2q}^*(e^{j\omega T_s})$ (dotted line). (b) Responses of the Foster model: $I_{2d}(e^{j\omega T_s})/I_{2d}^*(e^{j\omega T_s})$ (solid line), $I_{2d}(e^{j\omega T_s})/I_{2q}^*(e^{j\omega T_s})$ (dotted line).

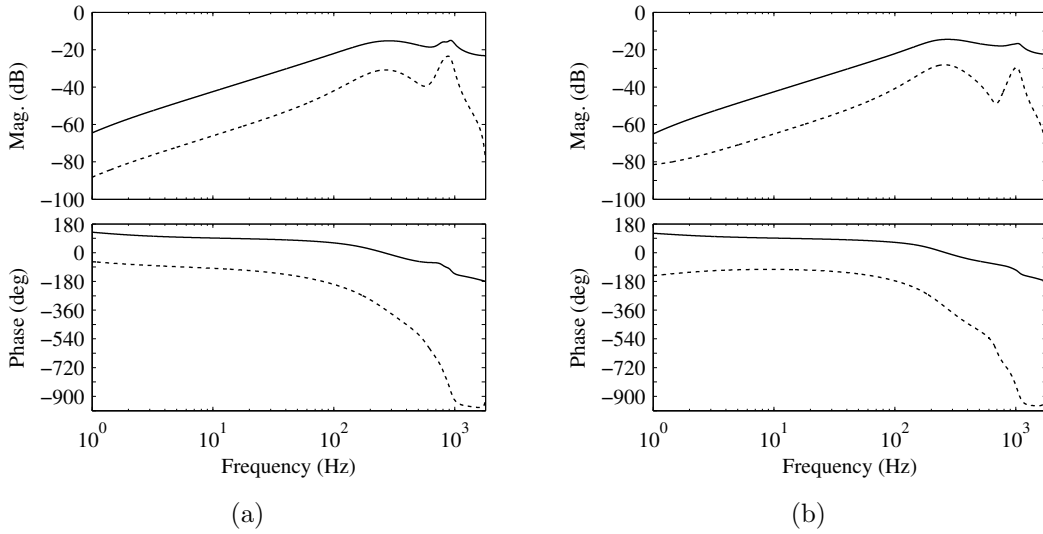


Fig. 5.12: (a) Responses of the RL model: $I_{2d}(e^{j\omega T_s})/U_{2d}(e^{j\omega T_s})$ (solid line), $I_{2d}(e^{j\omega T_s})/U_{2q}(e^{j\omega T_s})$ (dotted line). (b) Responses of the Foster model: $I_{2d}(e^{j\omega T_s})/U_{2d}(e^{j\omega T_s})$ (solid line), $I_{2d}(e^{j\omega T_s})/U_{2q}(e^{j\omega T_s})$ (dotted line).

current waveforms show that the d and the q channel controllers are not perfectly decoupled. The Foster model shows a small steady-state error in the grid current as it was approximated based on the frequency responses.

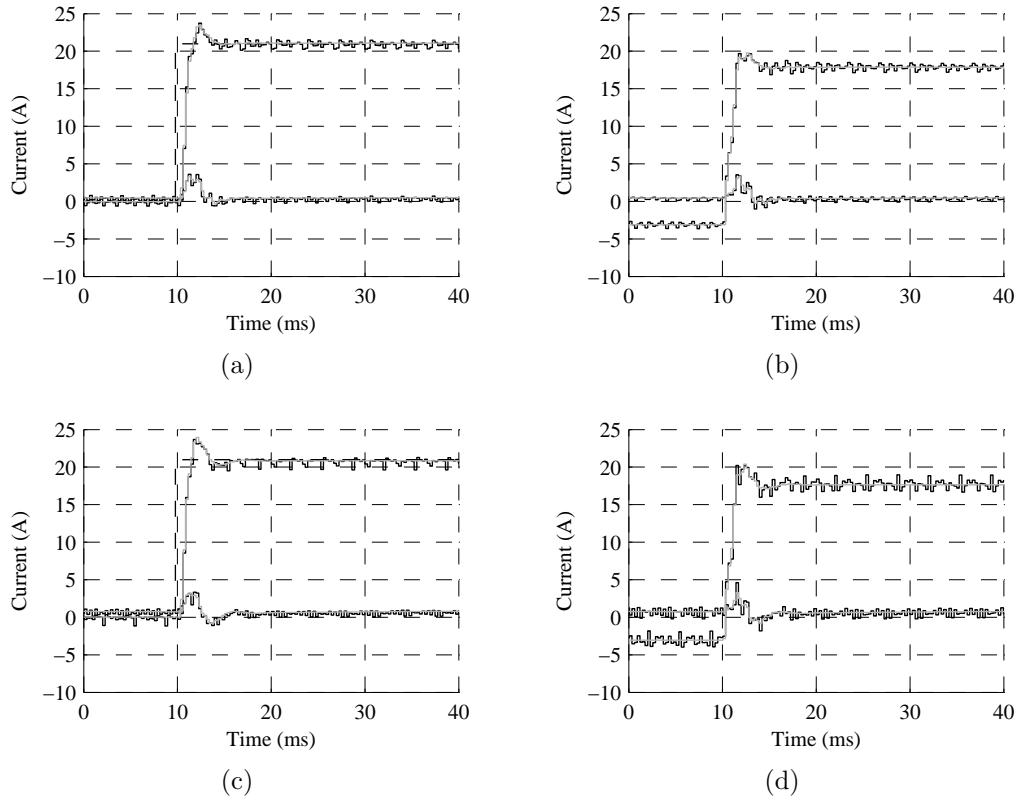


Fig. 5.13: Simulated step responses of the q -axis current. Gray solid line: response of the average model, Black solid line: response of the instantaneous STATCOM model, Dashed line: i_{2q}^* . (a) Grid current and (b) rectifier current when the inductors are modelled with series RL elements. (c) Grid current and (d) rectifier current when the inductors are modelled with Foster equivalent circuits.

5.5 Smith predictor

In this section, the Smith predictor is derived and included in the current control schemes studied in Sections 5.3 and 5.4. Firstly, the rectifier current in the beginning of sampling interval $[(k+1)T_s, (k+2)T_s]$ is approximated using the Forward Euler method:

$$\vec{u}_3(k) - \vec{u}_1^*(k-1) = \frac{L_1}{T_s} \left(\hat{i}_1(k+1) - \vec{i}_1(k) \right) + (R_1 + j\omega_r L_1) \vec{i}_1(k) \quad (5.89)$$

Then (5.89) is solved for $\hat{i}_1(k+1)$ and the feedback from the error $\vec{i}_1(k) - \hat{i}_1(k)$ is included. The predicted rectifier current can be expressed as

$$\begin{aligned} \hat{i}_1(k+1) = & \frac{T_s}{L_1} (\vec{u}_3(k) - \vec{u}_1^*(k-1)) + \left(1 - \frac{T_s R_1}{L_1} - j\omega_r T_s \right) \hat{i}_1(k) + \\ & K_{sp} \left(\vec{i}_1(k) - \hat{i}_1(k) \right) \end{aligned} \quad (5.90)$$

where K_{sp} is the feedback gain. The voltage \vec{u}_3 present in (5.90) can be solved by expressing (5.44) as follows

$$\begin{aligned} \vec{u}_3(k) = & c \left(\frac{L_3}{L_1} R_1 - R_C - R_3 \right) \vec{i}_1(k) + c \left(R_C + R_3 - \frac{L_3}{L_2} R_2 \right) \hat{i}_2(k) \\ & + c \hat{u}_{C3}(k) + c \frac{L_3}{L_1} \vec{u}_1^*(k-1) + c \frac{L_3}{L_2} \vec{u}_2(k) \end{aligned} \quad (5.91)$$

where $\hat{i}_2(k)$ and $\hat{u}_{C3}(k)$ can be estimated by using the observer presented in Section 5.4.1. When (5.91) is substituted in (5.90), the predictor can be expressed as follows

$$\begin{aligned} \hat{i}_1(k+1) = & \overbrace{c \frac{T_s}{L_1} \left(\frac{L_3}{L_1} R_1 - R_C - R_3 + \frac{L_1}{c T_s} K_{sp} \right)}^{=S_{i1}} \vec{i}_1(k) \\ & + \overbrace{c \frac{T_s}{L_1} \left(R_C + R_3 - \frac{L_3}{L_2} R_2 \right)}^{=S_{i2}} \hat{i}_2(k) + \overbrace{c \frac{T_s}{L_1} \hat{u}_{C3}(k)}^{=S_{uC3}} \\ & + \overbrace{\frac{T_s}{L_1} \left(c \frac{L_3}{L_1} - 1 \right)}^{=S_{u1}} \vec{u}_1^*(k-1) \\ & + \overbrace{\left(1 - \frac{T_s R_1}{L_1} - K_{sp} - j\omega_r T_s \right)}^{=S_{i1sp}} \hat{i}_1(k) + \overbrace{c \frac{T_s}{L_1} \frac{L_3}{L_2} \vec{u}_2(k)}^{=S_{u2}} \end{aligned} \quad (5.92)$$

and it can be separated into direct and quadrature components to obtain

$$\begin{aligned} \begin{bmatrix} \hat{i}_{1d}(k+1) \\ \hat{i}_{1q}(k+1) \end{bmatrix} = & \mathbf{S}_{i1} \begin{bmatrix} i_{1d}(k) \\ i_{1q}(k) \end{bmatrix} + \mathbf{S}_{i2} \begin{bmatrix} \hat{i}_{2d}(k) \\ \hat{i}_{2q}(k) \end{bmatrix} + \mathbf{S}_{uC3} \begin{bmatrix} \hat{u}_{C3d}(k) \\ \hat{u}_{C3q}(k) \end{bmatrix} + \mathbf{S}_{u1} \begin{bmatrix} u_{1d}^*(k-1) \\ u_{1q}^*(k-1) \end{bmatrix} \\ & + \mathbf{S}_{i1sp} \begin{bmatrix} \hat{i}_{1d}(k) \\ \hat{i}_{1q}(k) \end{bmatrix} + \mathbf{S}_{u2} \begin{bmatrix} u_{2d}(k) \\ u_{2q}(k) \end{bmatrix} \end{aligned} \quad (5.93)$$

Finally, the predictor output is included in the rectifier current error in line with Fig. 2.16:

$$\bar{e}(k) = \bar{i}_1^*(k) - \left(\bar{i}_1(k) - \hat{i}_1(k) \right) - \hat{i}_1(k+1) \quad (5.94)$$

5.5.1 Closed-loop model

The closed-loop model including the Smith predictor can be expressed as follows

$$\begin{bmatrix} \mathbf{x}(k+1) \\ \bar{\mathbf{x}}(k+1) \\ \mathbf{u}(k) \\ \mathbf{e}_{PI}(k) \\ \mathbf{y}_{PI}(k) \\ \hat{\mathbf{i}}_1(k+1) \end{bmatrix} = \begin{bmatrix} \Phi & \mathbf{0} & \Gamma_u & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{A}_x & \mathbf{A}_o & \mathbf{B}_u & \mathbf{0} & \mathbf{0} & \mathbf{0} \\ \mathbf{L}_x & \mathbf{L}_o & \mathbf{L}_u & \mathbf{L}_{ePI} & \mathbf{L}_{yPI} & \mathbf{L}_{i1sp} \\ \mathbf{M}_x & \mathbf{M}_o & \mathbf{M}_u & \mathbf{0} & \mathbf{0} & \mathbf{M}_{i1sp} \\ \mathbf{N}_x & \mathbf{N}_o & \mathbf{N}_u & \mathbf{N}_{ePI} & \mathbf{N}_{yPI} & \mathbf{N}_{i1sp} \\ \mathbf{S}_x & \mathbf{S}_o & \mathbf{S}_u & \mathbf{0} & \mathbf{0} & \mathbf{S}_{i1sp} \end{bmatrix} \begin{bmatrix} \mathbf{x}(k) \\ \bar{\mathbf{x}}(k) \\ \mathbf{u}(k-1) \\ \mathbf{e}_{PI}(k-1) \\ \mathbf{y}_{PI}(k-1) \\ \hat{\mathbf{i}}_1(k) \end{bmatrix} + \begin{bmatrix} \Gamma_w & \mathbf{0} \\ \mathbf{B}_w & \mathbf{0} \\ \mathbf{L}_w & \mathbf{L}_r \\ \mathbf{M}_w & \mathbf{M}_r \\ \mathbf{N}_w & \mathbf{N}_r \\ \mathbf{S}_w & \mathbf{0} \end{bmatrix} \begin{bmatrix} \mathbf{w}(k) \\ \mathbf{r}(k) \end{bmatrix} \quad (5.95)$$

where the new state variable $\hat{\mathbf{i}}_1(k) = [\hat{i}_{1d}(k) \ \hat{i}_{1q}(k)]^T$ is the predicted rectifier current. The coefficients matrices \mathbf{L}_x , \mathbf{L}_o , \mathbf{L}_u , \mathbf{L}_{ePI} , \mathbf{L}_{yPI} , \mathbf{L}_{i1sp} are developed by substituting the rectifier current error of the controllers studied in Sections 5.3 and 5.4 with (5.94). The coefficient matrices of the Smith predictor are developed using (5.93) and (5.14)-(5.17), and they can be expressed as follows:

$$\mathbf{S}_x = (\mathbf{S}_{i1} + \mathbf{S}_o \mathbf{L}) \mathbf{K}_{i1-x} + \mathbf{S}_{u2} \mathbf{K}_{u2-x} \quad (5.96)$$

$$\mathbf{S}_o = [\mathbf{S}_{i2} \ \mathbf{0} \ \mathbf{S}_{uC3}] \quad (5.97)$$

$$\mathbf{S}_u = \mathbf{S}_{u1} + (\mathbf{S}_{i1} + \mathbf{S}_o \mathbf{L}) \mathbf{K}_{i1-u} + \mathbf{S}_{u2} \mathbf{K}_{u2-u} \quad (5.98)$$

$$\mathbf{S}_w = (\mathbf{S}_{i1} + \mathbf{S}_o \mathbf{L}) \mathbf{K}_{i1-w} + \mathbf{S}_{u2} \mathbf{K}_{u2-w} \quad (5.99)$$

5.5.2 Effect on the grid current controller characteristics

PI current control strategy

Firstly, the predictor's effect on the PI current control strategy is studied. Fig. 5.14 illustrates the loci of the closed-loop poles when the proportional gains are varied. The controller and the observer are parametrised using the nominal filter component values. Compared with the original PI control strategy, the inclusion of the predictor increases the damping of the poles located nearest to the unit circle. Fig. 5.14(b) shows that in the case of Foster model the observer poles depart from their designed locations and move towards the unit circle when K_{sp} and K_p increase. Because of

the sensitivity of controller and observer poles to modelling errors, the controller gains $K_p = 3.25$ and $K_{sp} = 0.39$ are selected for further investigation.

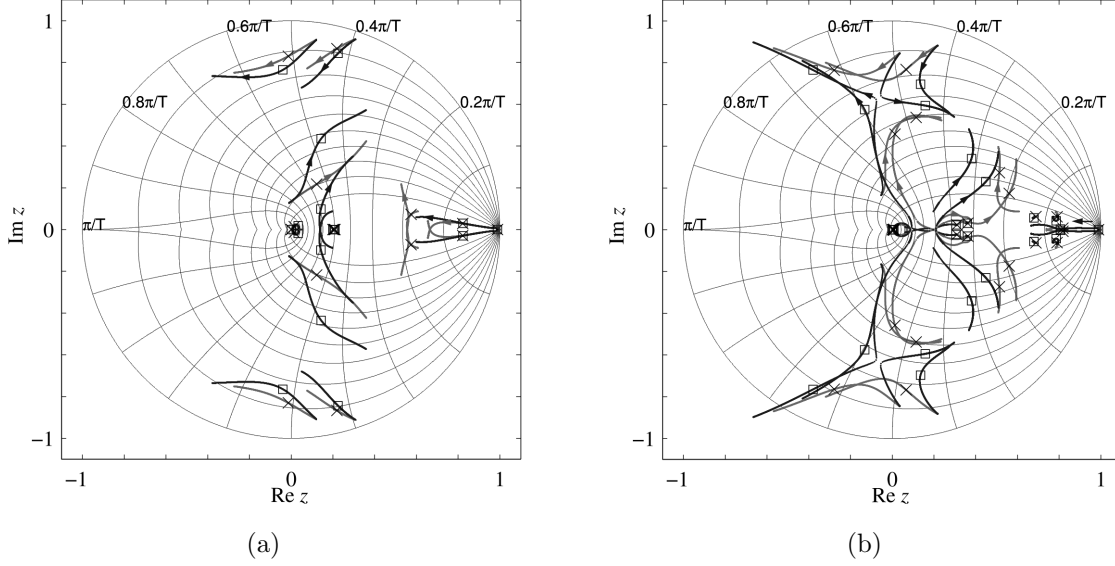


Fig. 5.14: Loci of the closed-loop poles when the predictor is included in the PI current control strategy: (a) *RL* model, (b) Foster model. The controller parameters are varied as follows: $K_p \in [0, 7.2]$, $K_{sp} \in \{0.39, 0.8\}$, $K_i = 40$. The pole locations with $K_p = 3.25$ are marked with crosses (\times) for $K_{sp} = 0.39$ and with squares (\square) for $K_{sp} = 0.8$.

The responses $I_{1d}(e^{j\omega T_s})/I_{1d}^*(e^{j\omega T_s})$ and $I_{1d}(e^{j\omega T_s})/I_{1q}^*(e^{j\omega T_s})$ are depicted in Fig. 5.15. The control bandwidth of both the *RL* model and the Foster model is ca. 121 Hz. Compared with the behaviour of the original PI control strategy, depicted in Fig. 5.4, the predictor has increased the damping of the *LCL* filter's resonant peak. The same effect can be seen in the $I_{2d}(e^{j\omega T_s})/U_{2d}(e^{j\omega T_s})$ and $I_{2d}(e^{j\omega T_s})/U_{2q}(e^{j\omega T_s})$ responses illustrated in Fig. 5.16. Otherwise the capability to reject grid voltage harmonics is similar to the original controller.

Fig. 5.17 compares the STATCOM current responses to the step-change of *q*-axis current reference with and without the predictor. The inclusion of the predictor reduces the oscillations but the narrower control bandwidth increases the rise-time. In the case of *RL* model, the controller gains could be increased to improve the dynamic behaviour. However, the analysis of the Foster model showed that the controller is sensitive to modelling errors when the predictor is included. Therefore, the controller gains were selected based on the behaviour of the Foster model.

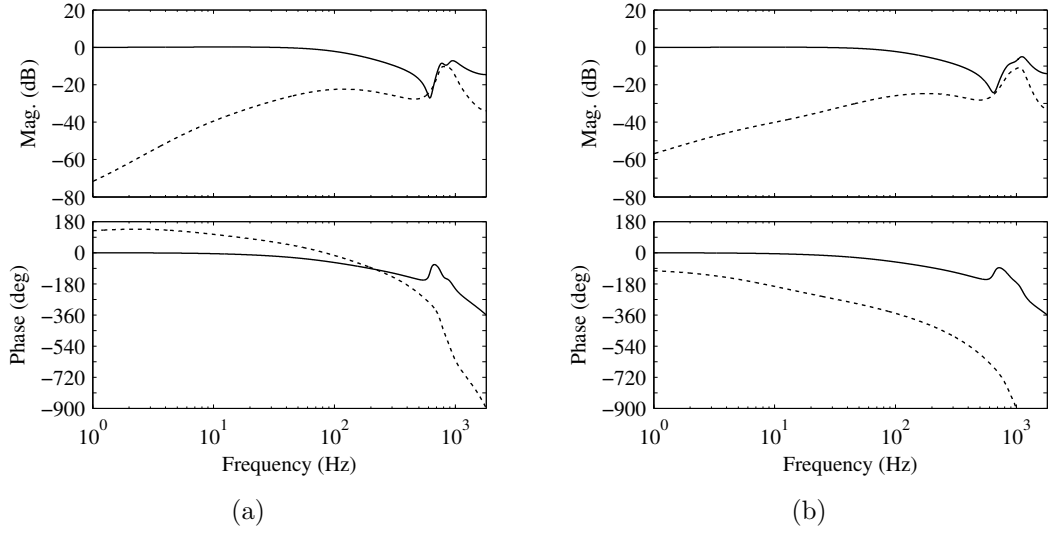


Fig. 5.15: Responses $I_{1d}(e^{j\omega T_s})/I_{1d}^*(e^{j\omega T_s})$ and $I_{1d}(e^{j\omega T_s})/I_{1q}^*(e^{j\omega T_s})$ when the predictor is included in the PI current control strategy. (a) *RL* model: $I_{1d}(e^{j\omega T_s})/I_{1d}^*(e^{j\omega T_s})$ (solid line), $I_{1d}(e^{j\omega T_s})/I_{1q}^*(e^{j\omega T_s})$ (dotted line). (b) Foster model: $I_{1d}(e^{j\omega T_s})/I_{1d}^*(e^{j\omega T_s})$ (solid line), $I_{1d}(e^{j\omega T_s})/I_{1q}^*(e^{j\omega T_s})$ (dotted line).

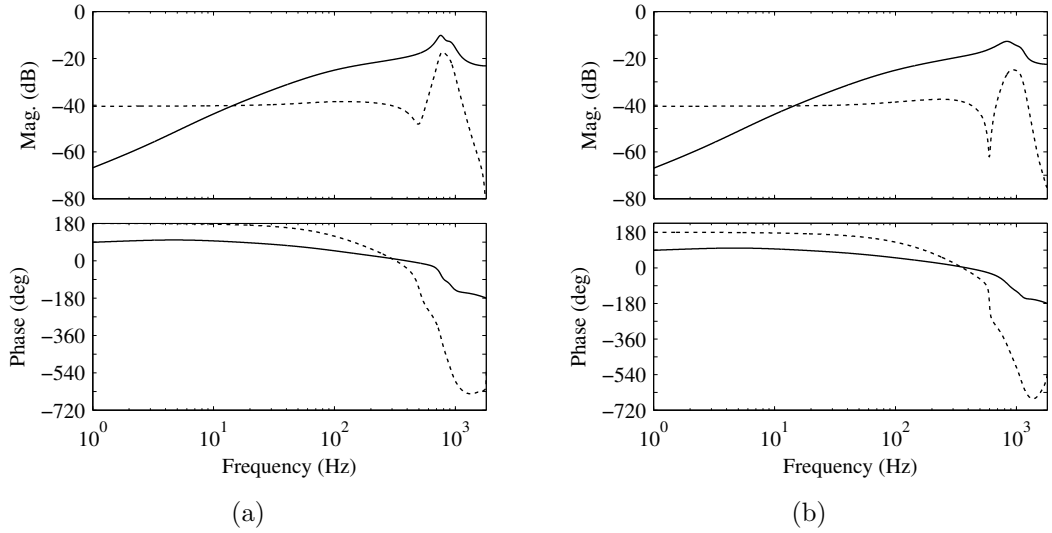


Fig. 5.16: Responses $I_{2d}(e^{j\omega T_s})/U_{2d}(e^{j\omega T_s})$ and $I_{2d}(e^{j\omega T_s})/U_{2q}(e^{j\omega T_s})$ when the predictor is included in the PI current control strategy. (a) *RL* model: $I_{2d}(e^{j\omega T_s})/U_{2d}(e^{j\omega T_s})$ (solid line), $I_{2d}(e^{j\omega T_s})/U_{2q}(e^{j\omega T_s})$ (dotted line). (b) Foster model: $I_{2d}(e^{j\omega T_s})/U_{2d}(e^{j\omega T_s})$ (solid line), $I_{2d}(e^{j\omega T_s})/U_{2q}(e^{j\omega T_s})$ (dotted line).

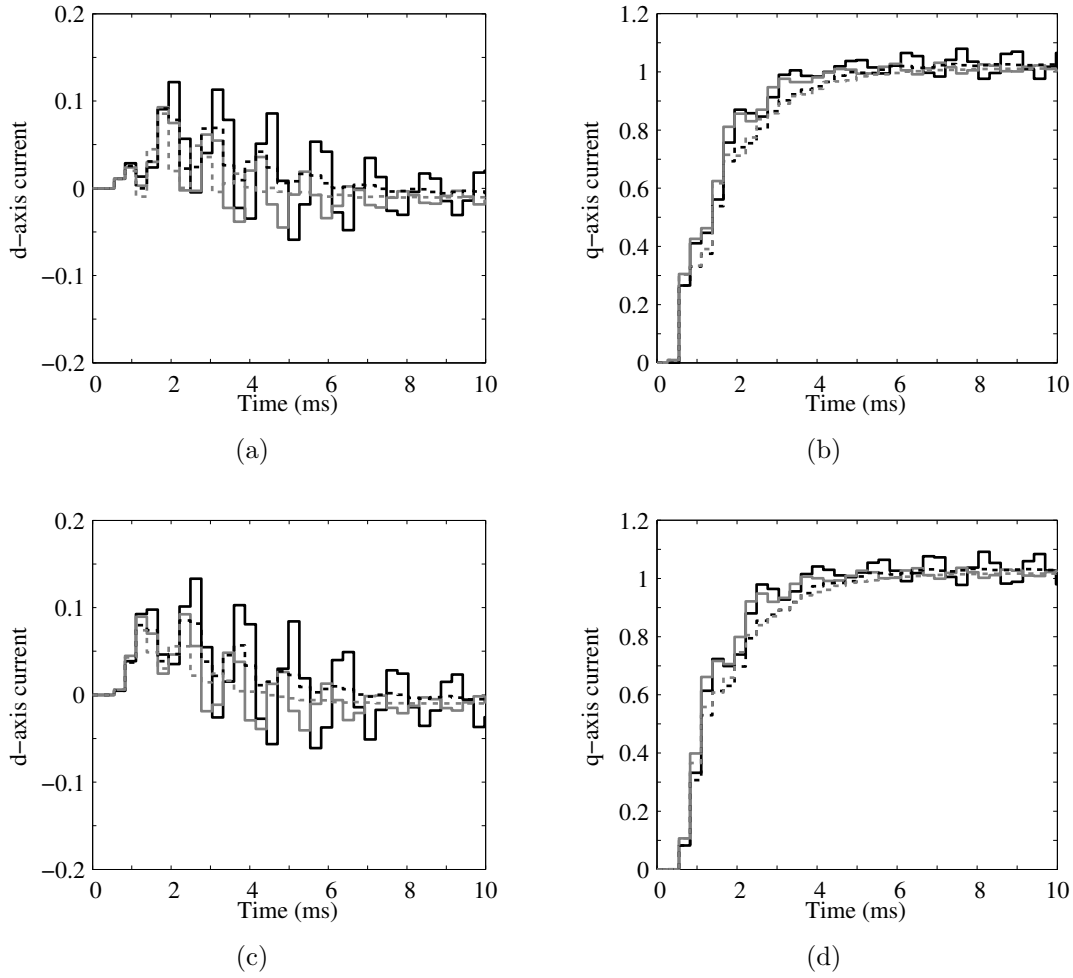


Fig. 5.17: Responses of the average models to the step-change of q -axis rectifier current reference. (a) d -axis rectifier current, (b) q -axis rectifier current, (c) d -axis grid current, (d) q -axis grid current. Black solid line: RL model without the predictor. Gray solid line: Foster model without the predictor. Black dotted line: RL model with the predictor. Gray dotted line: Foster model with the predictor.

Predictive vector current control strategy

Fig. 5.18 illustrates the closed-loop pole loci when the Smith predictor is included in the predictive vector current control strategy, and the proportional gains are varied. In the case of RL model, the predictor increases the damping of the resonant poles located near the unit circle compared with the original controller, the behaviour of which is depicted in Fig. 5.9. Based on the RL model, the controller gains could be increased to improve the response time. However, the parameters $K_{i1} = 0.3$ and $K_{sp} = 0.39$ are selected for further investigation, because in the case of Foster model the control is very sensitive to parameter variations.

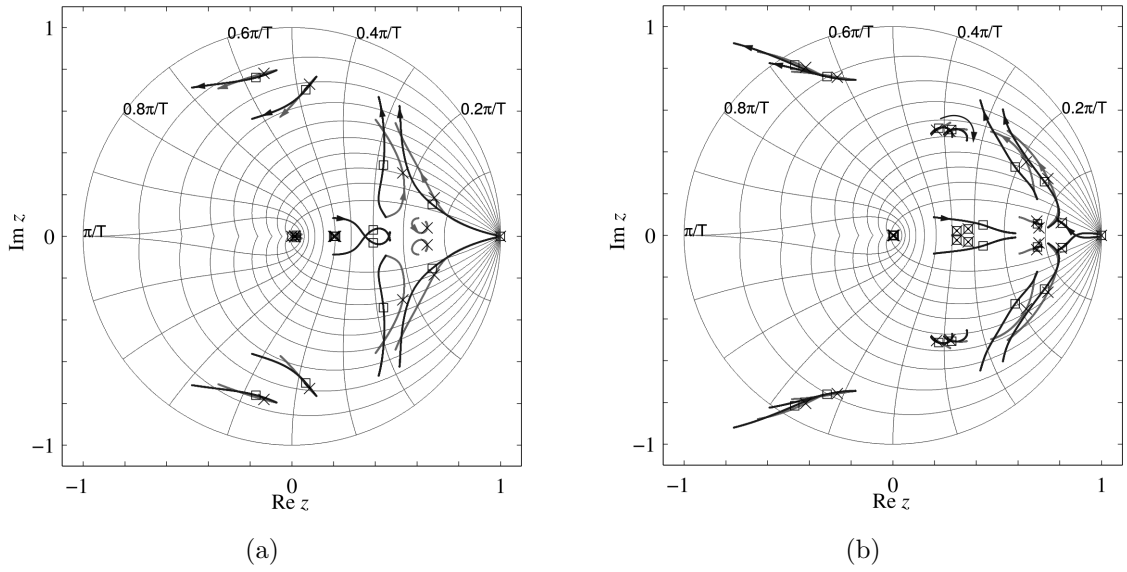


Fig. 5.18: Loci of the closed-loop poles when the Smith predictor is included in the predictive vector current control strategy. (a) RL model, (b) Foster model. The controller parameters are varied as follows: $K_{i1} \in [0, 1]$, $K_i = 40$, $K_{i2} = 0.2$, $K_{i3} = K_{uC3} = 1$, $K_{sp} \in \{0.39, 0.8\}$. The pole locations with $K_{i1} = 0.3$ have been marked with crosses (\times) for $K_{sp} = 0.39$ and with squares (\square) for $K_{sp} = 0.8$.

Fig. 5.19 illustrates the responses $I_{2d}(e^{j\omega T_s})/I_{2d}^*(e^{j\omega T_s})$ and $I_{2d}(e^{j\omega T_s})/I_{2q}^*(e^{j\omega T_s})$. The control bandwidth is ca. 266 Hz with the RL model and ca. 298 Hz with the Foster model. Compared with Fig. 5.11, the predictor has slightly reduced the cross-coupling above 100 Hz. The DC gain of $I_{2d}(e^{j\omega T_s})/I_{2d}^*(e^{j\omega T_s})$ in the case of Foster model is ca. -0.077 dB which yields ca. 1% steady state error. Based on Fig. 5.20, the capability to reject grid voltage harmonics is comparable to the original controller without the Smith predictor, the behaviour of which is depicted in Fig. 5.12.

Fig. 5.21 presents the responses to the step-change of q -axis current reference with and without the Smith predictor. The controller and the observer are parametrised using the nominal component values. The predictor reduces the oscillations and mitigates the overshoot but the rise-times are faster without the predictor because of the wider control bandwidths. In terms of rise-time, the responses of the predictive

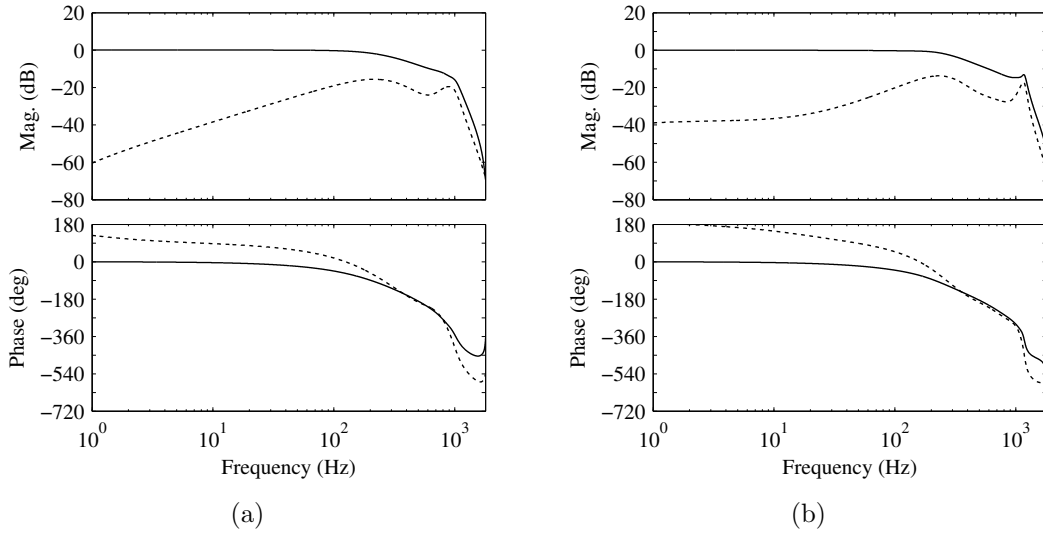


Fig. 5.19: Responses $I_{2d}(e^{j\omega T_s})/I_{2d}^*(e^{j\omega T_s})$ and $I_{2d}(e^{j\omega T_s})/I_{2q}^*(e^{j\omega T_s})$ when the Smith predictor is included in the predictive vector current controller. (a) *RL* model: $I_{2d}(e^{j\omega T_s})/I_{2d}^*(e^{j\omega T_s})$ (solid line), $I_{2d}(e^{j\omega T_s})/I_{2q}^*(e^{j\omega T_s})$ (dotted line). (b) Foster model: $I_{2d}(e^{j\omega T_s})/I_{2d}^*(e^{j\omega T_s})$ (solid line), $I_{2d}(e^{j\omega T_s})/I_{2q}^*(e^{j\omega T_s})$ (dotted line).

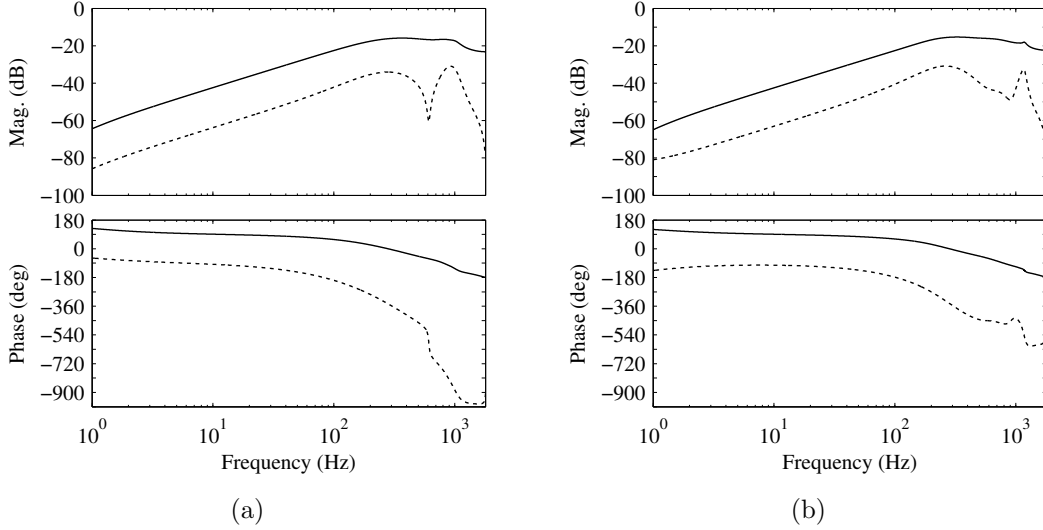


Fig. 5.20: Responses $I_{2d}(e^{j\omega T_s})/U_{2d}(e^{j\omega T_s})$ and $I_{2d}(e^{j\omega T_s})/U_{2q}(e^{j\omega T_s})$ when the Smith predictor is included in the predictive vector current controller. (a) *RL* model: $I_{2d}(e^{j\omega T_s})/U_{2d}(e^{j\omega T_s})$ (solid line), $I_{2d}(e^{j\omega T_s})/U_{2q}(e^{j\omega T_s})$ (dotted line). (b) Foster model: $I_{2d}(e^{j\omega T_s})/U_{2d}(e^{j\omega T_s})$ (solid line), $I_{2d}(e^{j\omega T_s})/U_{2q}(e^{j\omega T_s})$ (dotted line).

vector current controllers are faster compared with the PI current controllers (see Fig. 5.17).

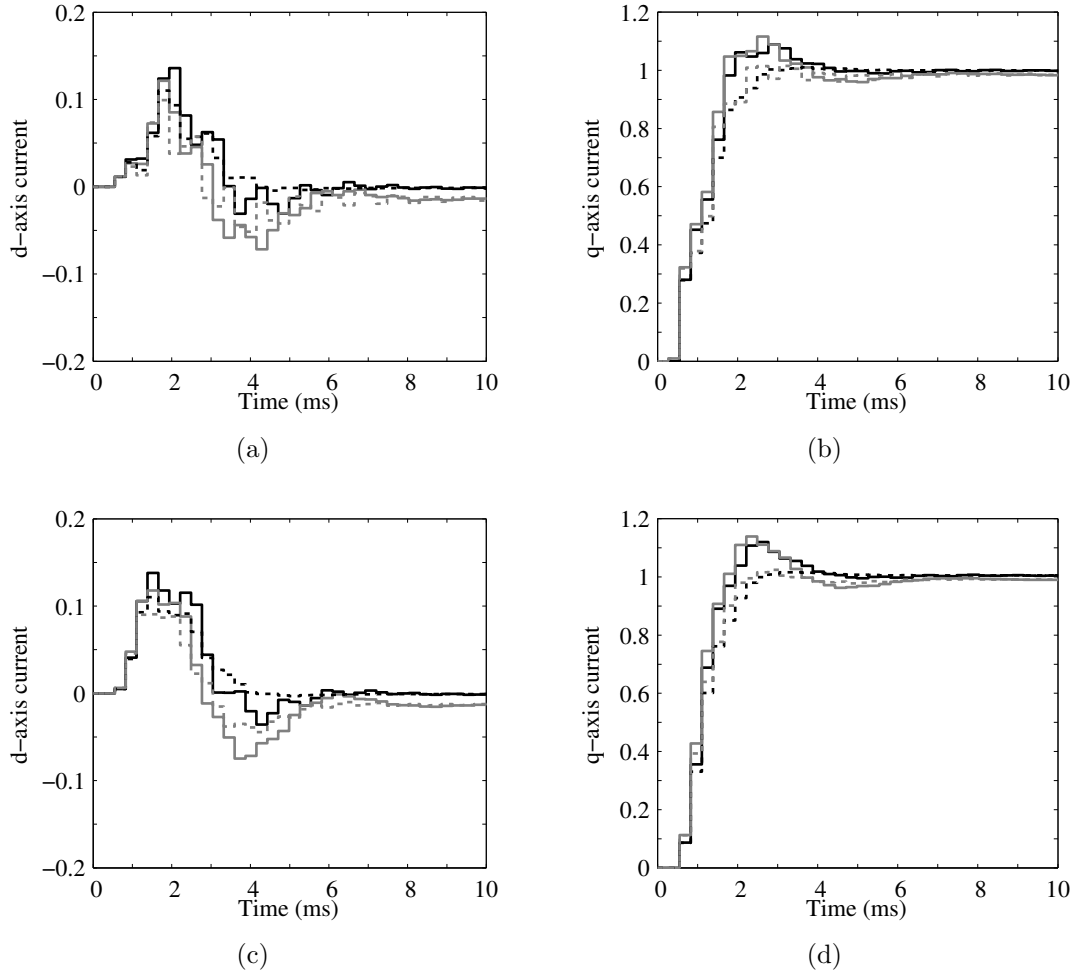


Fig. 5.21: Responses of the average models to the step-change of q -axis grid current reference. (a) d -axis rectifier current, (b) q -axis rectifier current, (c) d -axis grid current, (d) q -axis grid current. Black solid line: RL model with the predictive vector current controller, Gray solid line: Foster model with the predictive vector current controller. Black dotted line: RL model with the predictive vector current controller and the Smith predictor. Gray dotted line: Foster model with the predictive vector current controller and the Smith predictor.

Step-response simulations

Fig. 5.22 depicts the step responses of the average models and the Simulink model of the STATCOM. The responses are in a good agreement. The predictor mitigates the oscillation from the response of the PI control strategy. In the case of predictive vector current control, the inclusion of the Smith predictor eliminates the overshoot. The Simulink simulation including the Foster equivalent circuits of the filter inductors' shows that a portion of the switching frequency ripple is included in the sampled rectifier current.

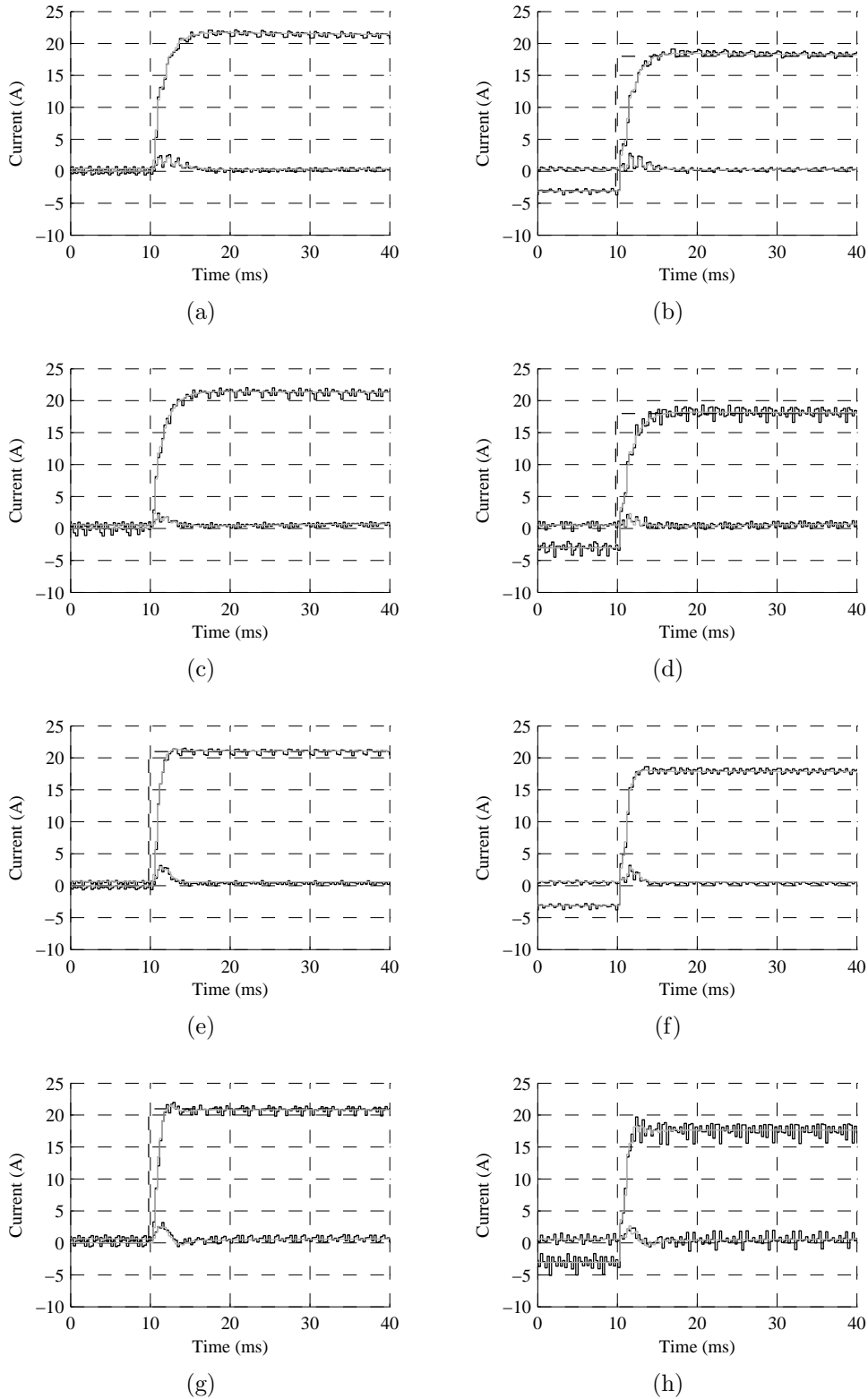


Fig. 5.22: Simulated step responses. (a)-(d) PI control with the Smith predictor: (a) Grid current and (b) rectifier current of the RL model. (c) Grid current and (d) rectifier current of the Foster model. (e)-(h) Predictive vector current controller with the Smith predictor: (e) Grid current and (f) rectifier current of the RL model. (g) Grid current and (h) rectifier current of the Foster model.

5.6 Influence of grid impedance on the control stability

Next the effect of grid impedance on the stability of the closed-loop current control is studied. The grid impedance Z_g is defined using the short circuit ratio (SCR)

$$\text{SCR} = \frac{S_g}{S_n} = \frac{U_g^2}{Z_g S_n} \quad (5.100)$$

where S_g denotes the short-circuit capacity of the grid at the STATCOM's connection point, S_n denotes the nominal apparent power of the STATCOM, and U_g denotes the grid voltage. The PLL is not included in the average closed-loop models and, therefore, they operate as if the synchronisation was ideal. During the simulations it was observed that at very low SCR values the dynamic behaviour of the average models starts to differ from the instantaneous STATCOM simulation model. The responses were in a good agreement with SCRs down to 5 which is the lower limit in the presented results.

Figs. 5.23-5.26 illustrate the loci of the closed-loop poles when $\text{SCR} \in (\infty, 5]$. The ratio between the grid reactance and resistance is five. The grid is considered stiff when $\text{SCR} > 20$ and weak when $\text{SCR} < 10$. The controllers and the observer are parametrised using the nominal filter component values. The pole locations at $\text{SCR} \approx \infty$ are highlighted with crosses (\times), at $\text{SCR} = 20$ with triangles (\triangle), and at $\text{SCR} = 10$ with squares (\square). The controllers remain stable within the studied range of SCR. When the SCR decreases, the poles move towards the point (1, 0) which implies that the settling time increases and the damping reduces.

Figs. 5.24(a), 5.25(a), and 5.26(a) show that in the case of RL model, when the observer is an accurate copy of the LCL filter circuit, the grid impedance variation has a strong effect on the observer poles. Regarding the Foster models, in Figs. 5.24(b), 5.25(b), and 5.26(b), the grid impedance variation has less effect on the observer poles. However, the poles have displaced from the designed locations because of the parametric uncertainty of the observer.

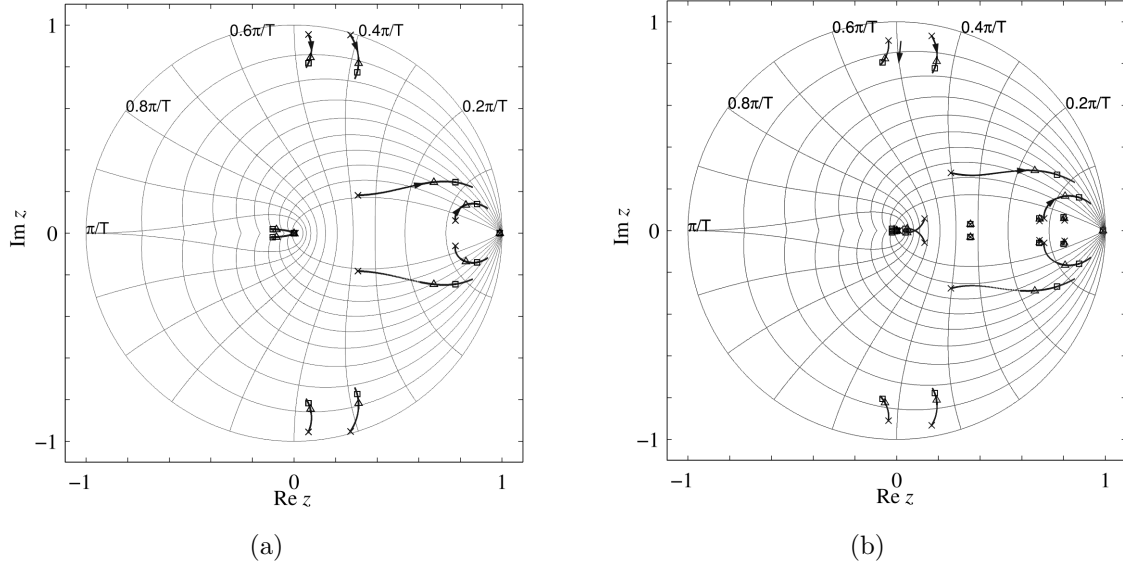


Fig. 5.23: Pole loci of the PI current control strategy. (a) RL model, (b) Foster model.

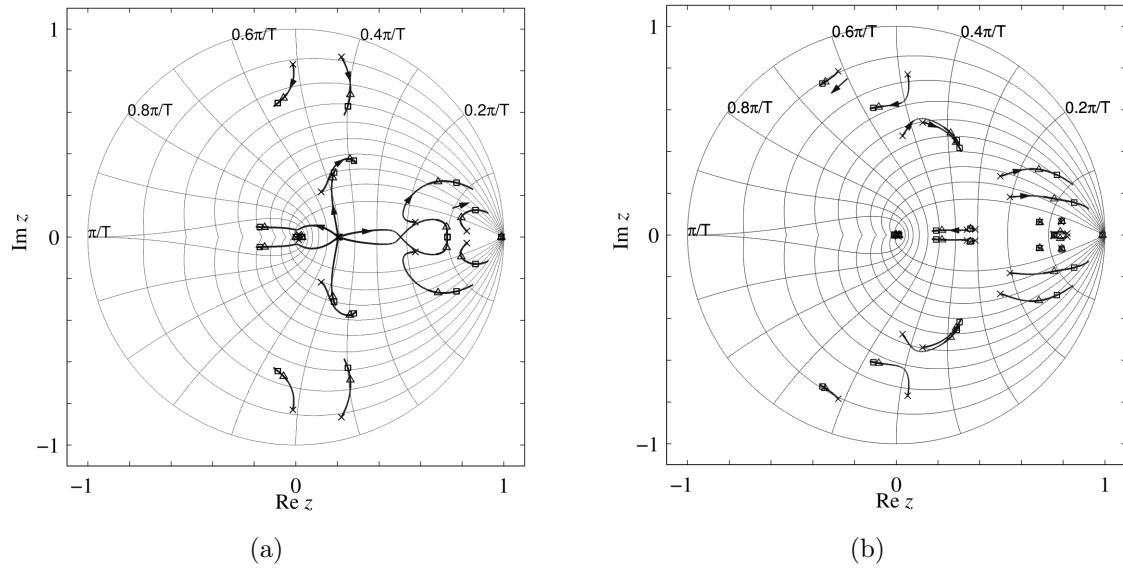


Fig. 5.24: Pole loci of the PI current control strategy with the Smith predictor. (a) RL model, (b) Foster model.

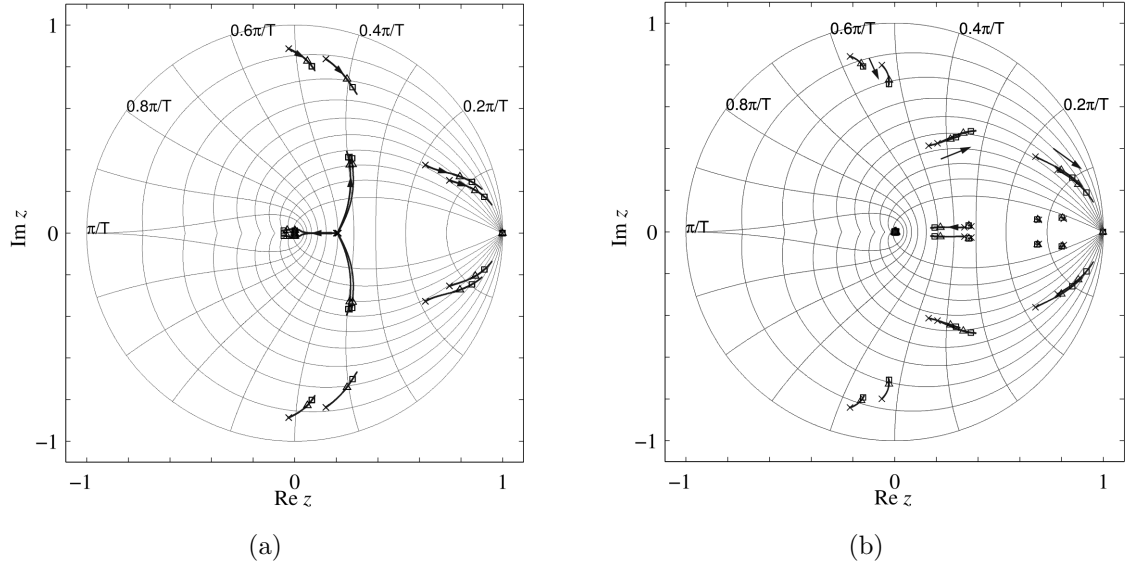


Fig. 5.25: Pole loci of the predictive vector current control strategy. (a) *RL* model, (b) Foster model.

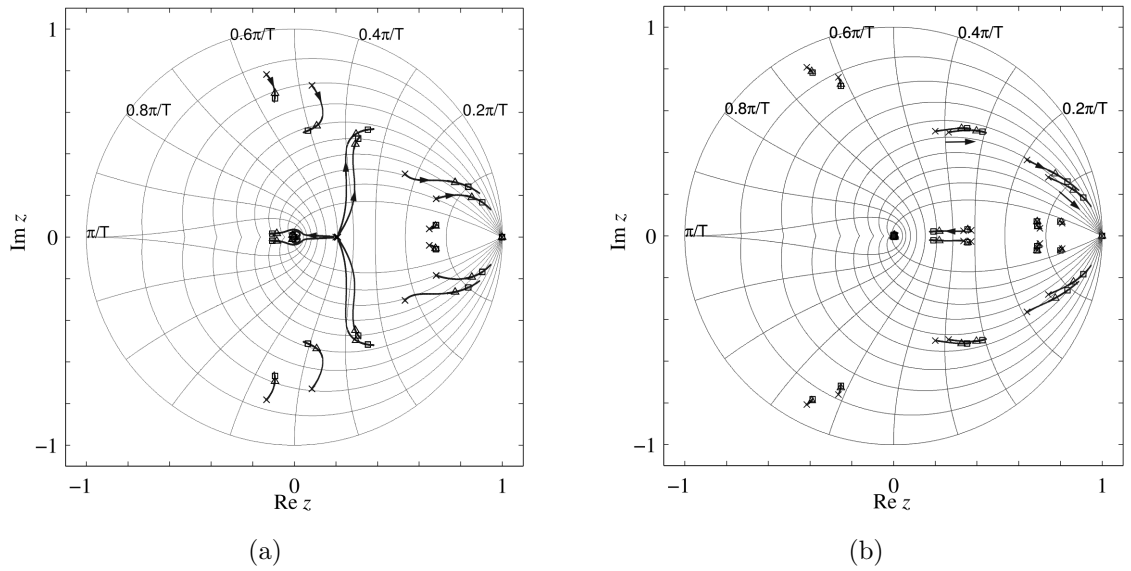


Fig. 5.26: Pole loci of the predictive vector current control strategy with the Smith predictor. (a) *RL* model, (b) Foster model.

5.7 Conclusions

The results of this chapter show that frequency independent filter component models may be insufficient to characterise the experimental system with the required accuracy. In the case of PI current control strategy, the *LCL* filter resonance was underdamped when the filter inductors were modelled with series *RL* elements. The inclusion of inductors' Foster equivalent circuits increased the natural damping of the filter and mitigated the oscillating behaviour. However, the resonant poles were located near the unit circle which limited the selection of the controller gain and the reachable bandwidth. Regarding the predictive vector current control scheme, a major problem was the observer's sensitivity to parametric uncertainties. The same problem was associated with the Smith predictor.

The average models were verified by comparing their step-change responses to the instantaneous Simulink model of the STATCOM. The responses were in a good agreement which proves the validity of the models.

Based on the frequency response analyses, the both controllers are incapable to properly reject the background grid voltage distortion. The fifth and the seventh voltage harmonic can be a problem, especially in the case of predictive vector current controller. The performance did not change when the Smith predictor was included in the controllers. An additional harmonic controller could be inserted in parallel with the main current controller, as proposed in [165, 108], to mitigate the effects of background grid voltage harmonics on the grid current waveform.

In the case of *RL* models, the Smith predictor increased the damping of the resonant poles located nearest to the unit circle. However, the Foster models showed that the combination of the predictor and the observer is sensitive to modelling errors. Therefore, the controller gains and the control bandwidths could not be increased compared with the original controllers. The step response simulations showed that the predictor mitigated the oscillatory behaviour of the PI current control strategy. In the case of predictive vector current controller, the overshoot was eliminated. As a result, the predictor can potentially improve the dynamic behaviour of the controllers, but in this study, the benefits were hindered by its sensitivity to parametric uncertainty. Furthermore, the predictor increases the required control computation effort.

Finally, the effects of grid impedance variation on the control dynamics were revealed. Based on the results, the changes in the network condition can yield unexpected performance, even instability, if the dynamic behaviour is optimised at a single operating point. It was also shown that the observer poles are sensitive to grid impedance variation which is a potential problem in practical applications. In conclusion, to guarantee satisfactory dynamic behaviour and robustness of the control, the grid current controller and the observer should adapt to the network impedance variation or tolerate the impedance variation within a required range.

Chapter 6

Simulation and experimental verification

6.1 Introduction

In this chapter, the theoretical considerations presented are validated by means of computer simulations and laboratory experiments. Firstly, the 10 kVA STATCOM prototype based on the three-level NPC rectifier is presented. After that, the laboratory test results are presented and compared with Simulink simulations. The main objectives are to prove the operation of the switching control strategy and the modulator functions presented in Chapter 4, and to verify that the dynamic behaviour of the grid current controllers agrees with the analyses presented in Chapter 5.

6.2 Laboratory prototype

Fig. 6.1 depicts the laboratory prototype of the 10 kVA STATCOM. The hardware is based on the three-level back-to-back PWM converter investigated in [190] which was modified for the purposes of this study. The circuit schematic of the STATCOM is illustrated in Fig. 6.2 and its nominal parameters are summarised in Table 6.1.

The STATCOM is connected to the three-phase 400 V 50 Hz grid through an *LCL* filter circuit. The three-phase inductors L_1 , L_2 , and L_3 are each made of three laminated iron cores with individual windings. The filter shunt branch consists of the inductors L_3 in series with film capacitors C_3 . The series resonant frequency of the shunt branch is designed at 1800 Hz. The resonant frequency of the *LCL* filter is designed at 610 Hz and the resonant peak is damped with resistors R_d and R_C .

The rectifier bridge consists of three 600 V 75 A Semikron SK75MLI066T modules [191], each of which includes a three-level NPC bridge-leg. The turn-off voltage overshoots across the IGBTs are suppressed with six Vishay's 850 V 680 nF MKP

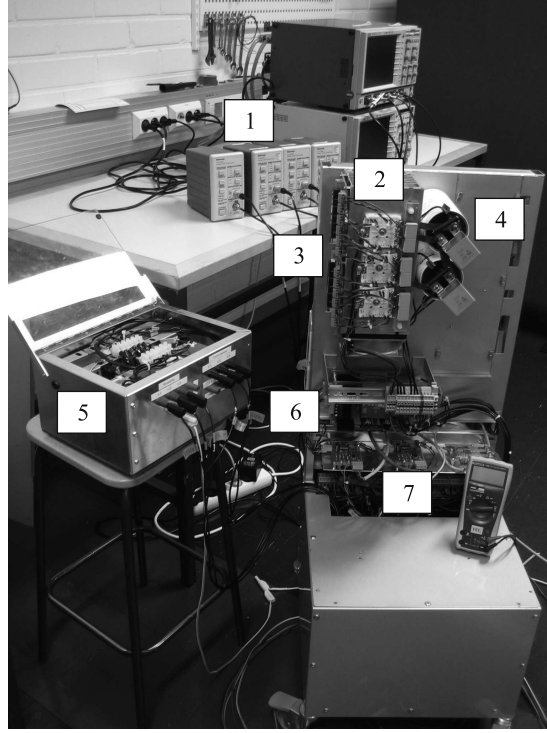


Fig. 6.1: Laboratory prototype of 10 kVA three-level STATCOM. 1: Measurement equipment, 2: snubber capacitors and SK75MLI066T modules mounted on a heat sink, 3: IGBT drivers, 4: DC bus capacitors, 5: *LCL* filter, 6: Auxiliary power supply, 7: AC and DC voltage measurement circuits.

snubber capacitors (C_{s1}). They are connected between the nodes p-o and o-n at the IGBT modules' DC terminals. The IGBTs are driven with two six-channel Concept SCALE 6SD106EI drivers. The blanking times are generated using resistor-capacitor delay circuits and inverting Schmitt-triggers 74HC14. For the outer switches S_{1k} and S_{4k} , the *RC* time constants are ca. $\tau_{on} = 3\mu s$ and $\tau_{off} = 22ns$. For the inner switches S_{2k} and S_{3k} , the time constants are ca. $\tau_{on} = \tau_{off} = 1.5\mu s$. The total turn-on and turn-off delays are $T_{d(on),S1/S4} \approx 3\mu s$, $T_{d(off),S1/S4} \approx 1\mu s$, $T_{d(on),S2/S3} \approx 1.7\mu s$, and $T_{d(off),S2/S3} \approx 2.6\mu s$ when the sum effect of blanking times, drive circuit delays, and semiconductor switching characteristics is considered.

The DC voltage bus consists of two 3300 μF 450 V_{DC} electrolytic capacitors from

Table 6.1: Nominal prototype parameters

S_n	10 kVA	U_n	400 V_{AC}
u_{DC}	680 V	f_s	3600 Hz
L_1	2.8 mH (5.5 %)	C_1	3300 μF (164 %)
L_2	2.0 mH (4 %)	C_2	3300 μF (164 %)
L_3	0.26 mH (0.5 %)	C_3	30 μF (15 %)
R_d	10 Ω	R_C	0.39 Ω
C_{s1}	680 nF	R_{dis}	47 $k\Omega$
C_{s2}	1.8 μF		

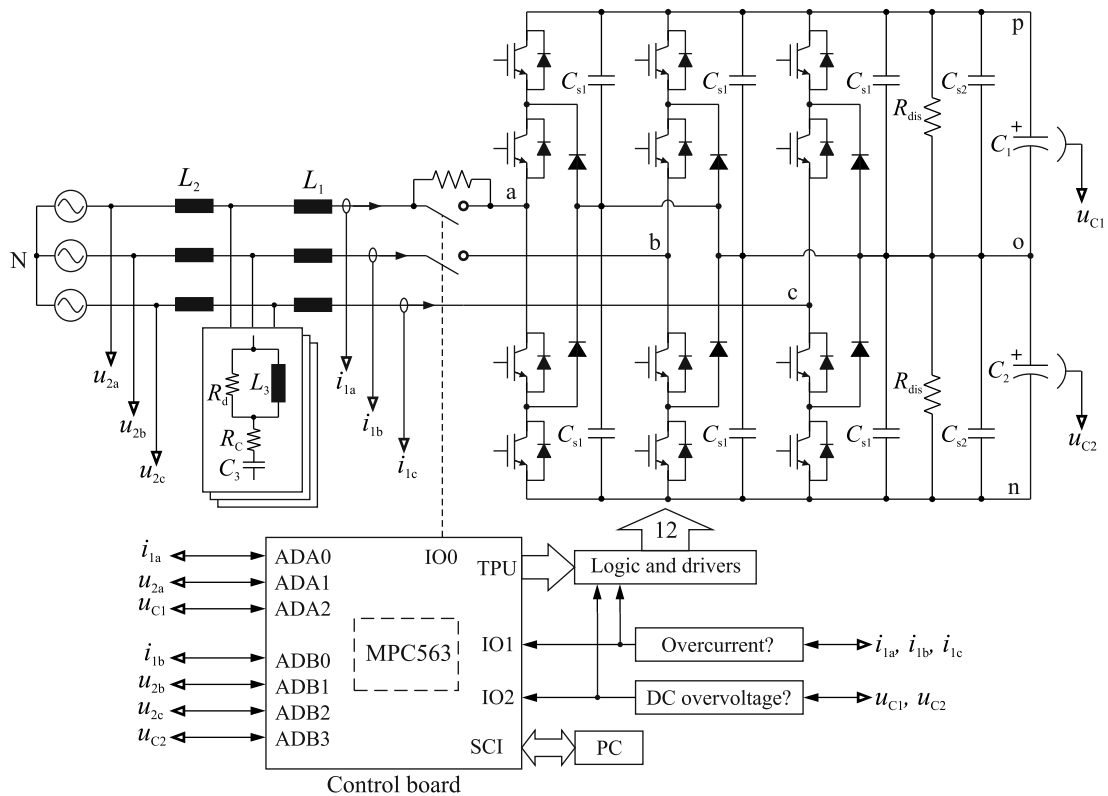


Fig. 6.2: Schematic of the laboratory prototype showing the main circuit diagram, measurement signals, and the basis of the control electronics.

Kemet's PEH200 series. Two 47 k Ω resistors (R_{dis}) are connected across the bus nodes p-o and o-n to discharge the capacitors after power-off and to ensure balanced voltage sharing during stand-by. Vishay's 850 V 1.8 μF MKP film capacitors (C_{s2}) are connected in parallel with the electrolytic capacitors to reduce the effects of stray inductance. The wiring between the DC capacitors and the power semiconductor modules is implemented with three stacked copper bus bars and polycarbonate insulations.

The rectifier currents are measured with compensated Hall-effect LEM LA55-P current transducers with 1:1000 conversion ratios. The currents are converted into voltage signals between ± 5 V which yields the measurement range between ± 50 A. The grid voltages are measured using resistive voltage scaling and the measurement range is between ± 355 V. Before the analogue-to-digital (AD) conversions the measured AC signals are scaled to the range of ± 2.5 V, and a $+2.5$ V offset is added because the input voltage range of the AD converters is 0...5 V. The three DC bus node voltages are measured against ground by using resistive voltage scaling and the DC capacitor voltages are obtained using differential-mode measurement. The capacitor voltage measurement range is 0...450 V_{DC}, which is scaled to 0...5 V.

The STATCOM control is implemented on Freescale's 32-bit MPC563MZIP66 microcontroller. It includes two queued AD converters with 10-bit resolution and two programmable 16-channel time processing units (TPU) for the generation of PWM signals. The IGBT driver control signals are generated with two generic array logic

(GAL26V12) circuits based on the TPU outputs. In addition, the control board includes auxiliary circuits for measurement signal processing, and overcurrent and overvoltage detection and protection.

The control software is programmed using C code but some arithmetic operations are written as assembly macros. The interrupt service routine is executed every 277 μs , which corresponds to the sampling frequency $f_s \approx 3600$ Hz. The AD converters operate independently, and therefore, two signals can be sampled simultaneously. The conversion time of one sample is approximately 7 μs , which is a drawback in the time-critical application, because various signals are sampled and synchronised sampling is desired. The scans of AD conversion queues ADA0-ADA1-ADA2 and ADB0-ADB1-ADB2-ADB3 (see Fig. 6.2) are started in the beginning of each interrupt period, and the program execution waits until the conversions are ready. The rectifier currents are sampled first to match the sampling instant with the zero-crossing of the ripple current waveforms. The human interface to the control software is implemented using RS-232 serial bus. Reading and writing of the serial bus data is performed using Matlab.

The measurement data are collected using LeCroy LT354M and LeCroy LC334AM oscilloscopes. The voltages, both AC and DC, are measured using Tektronix P5200 differential voltage probes. The AC currents are measured using Tektronix TCP312 probes and TCPA300 AC/DC current probe amplifiers.

Prior to the laboratory experiments, the STATCOM control has been tested by means of hardware-in-the-loop (HIL) simulations [187, 189]. The HIL simulation setup is presented in Appendix E. It was used as an intermediate test platform between the Simulink simulations and laboratory experiments to verify the operation of the SVM algorithm, the PLL, and the current controllers.

6.3 Verification of the modulation algorithm

This section demonstrates the operation of the modulation strategy presented in Chapter 4. The experimental results obtained with the STATCOM prototype are presented and compared to the simulated waveforms. Both the simulations and the laboratory experiments are performed using the controller parameters selected in Chapter 5. The principle of the Simulink model is presented in Appendix D.

6.3.1 Steady-state waveforms

Firstly, the steady-state current and voltage waveforms are studied. Both the experimental tests and the simulations are performed using the PI current control strategy and with all modulator functions enabled. In the simulations, the filter inductors are modelled with Foster equivalent circuits described in Appendix C, the grid voltages are purely sinusoidal and the grid impedance is zero.

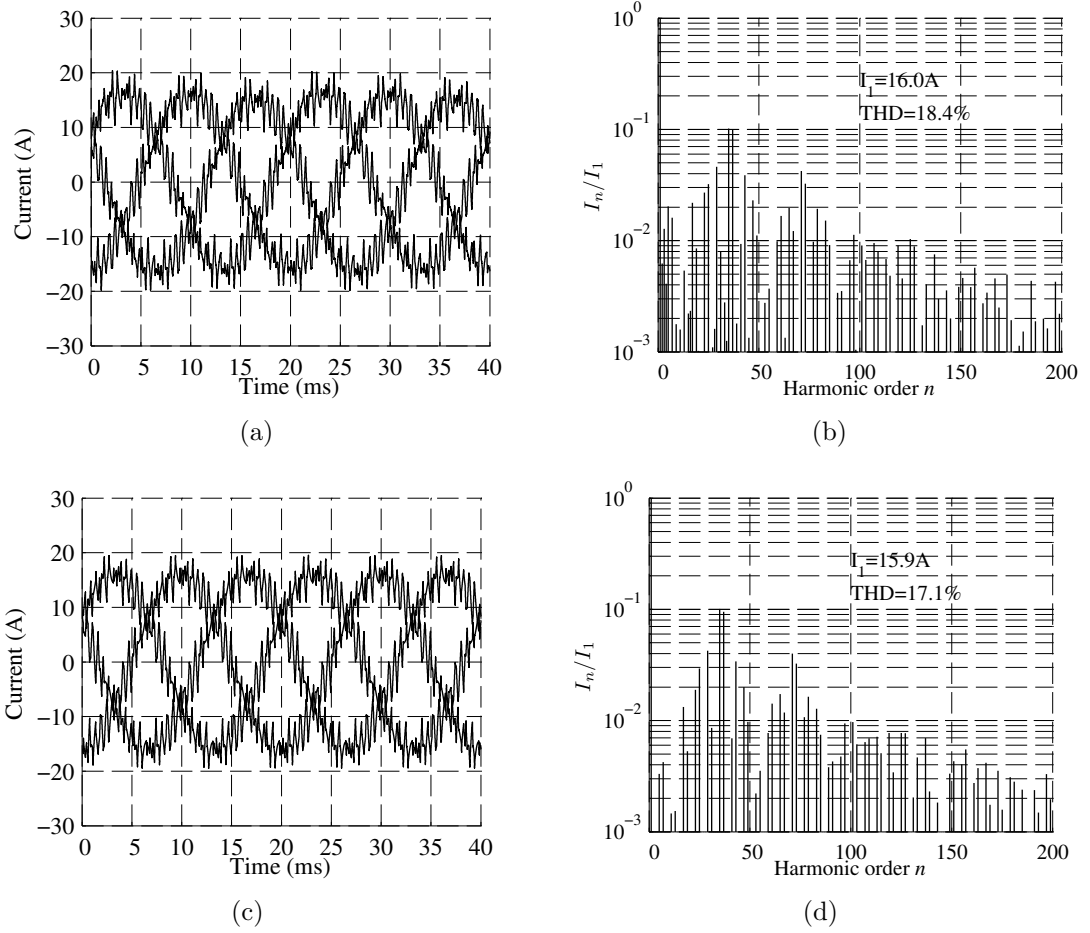


Fig. 6.3: (a)-(b) Experimental STATCOM currents and i_{1a} spectrum up to 10 kHz, (c)-(d) simulated waveforms and spectrum.

Figs. 6.3-6.4 present the rectifier and the grid current waveforms and the spectra of i_{1a} and i_{2a} when the rectifier is controlled to generate 19 A (peak) of capacitive reactive current. The experimental current waveforms are filtered with first-order discrete-time low-pass filters (DLPFs) to remove the measurement noise. The filter corner frequencies are set to $f_c = 100 \text{ kHz}$. The results show that the switching ripple current is effectively filtered by the LCL circuit and the grid currents are quite sinusoidal. The simulated current waveforms and spectra match with the experimental ones with a good accuracy. The spectra of experimental currents include some low frequency harmonics that are not present in the simulated waveforms. Those harmonics are caused by the background grid voltage harmonics.

Fig. 6.5 presents the waveforms of phase to DC bus midpoint voltages u_{ao} , u_{bo} , and u_{co} , and DC bus capacitor voltages. The experimental capacitor voltages have been filtered with first-order DLPFs ($f_c = 50 \text{ kHz}$). The PWM voltage waveforms reveal that the modulation is based on DPWM patterns. The DPWM pattern is selected based on the capacitor voltage difference, which causes the difference between the experimental and simulated PWM voltage waveforms. In both the simulations and experiments, the capacitor voltages are balanced on the average-basis but the low-frequency variation of the neutral-point voltage is not suppressed. Figs. 6.6 and 6.7 present the phase-to-neutral u_{aN} and line-to-line u_{ab} PWM voltage waveforms and

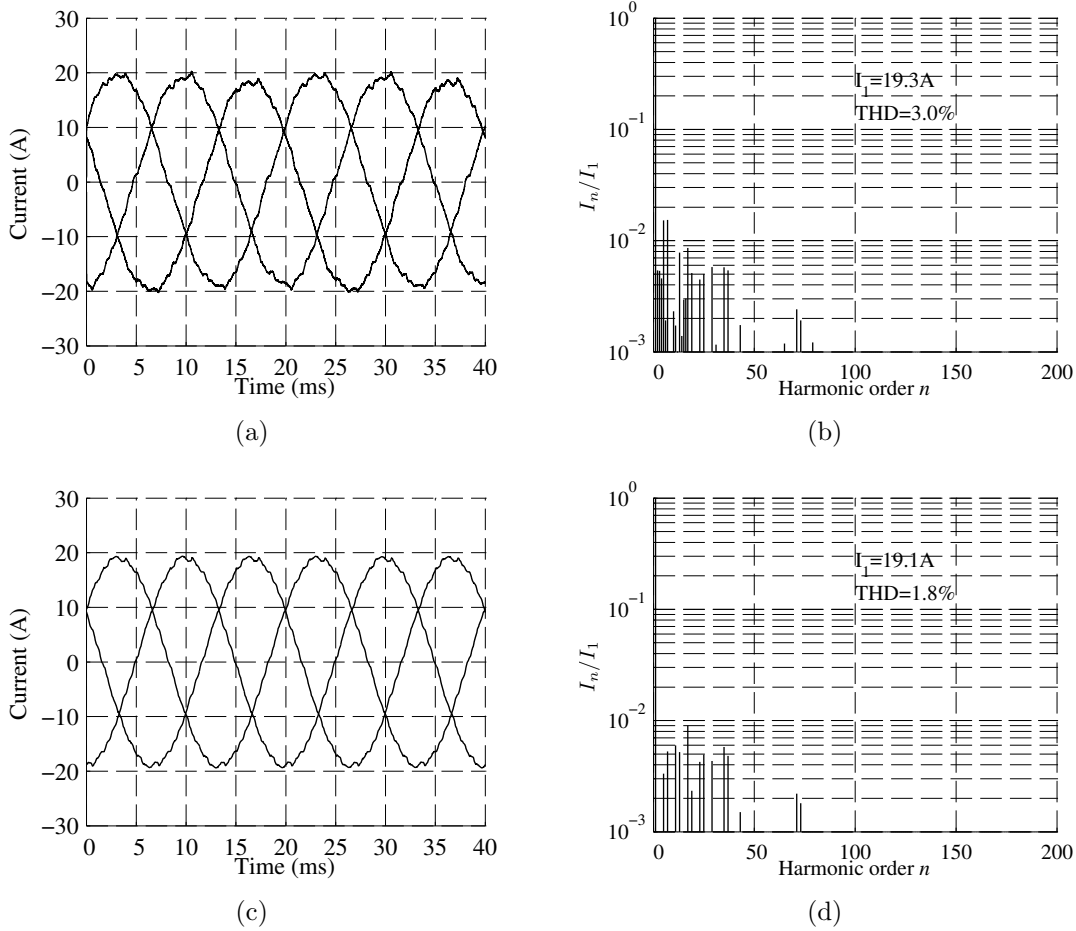


Fig. 6.4: (a)-(b) Experimental grid currents and i_{2a} spectrum up to 10 kHz, (c)-(d) simulated waveforms and spectrum.

the frequency spectra up to 10 kHz. The simulations and experimental results are in a good agreement.

Figs. 6.3-6.7 show that the experimental and simulated waveforms match with a good accuracy. Therefore, it can be said that the modulation strategy operates as it is designed to. During the measurements, it was observed that the grid voltages include the 5th and the 7th harmonics. Their effect can be seen in the frequency spectra of the experimental waveforms. Furthermore, the Simulink model does not consider the nonidealities of the power circuit, the component tolerances, or the asymmetry of impedances between the phases, which may cause differences compared with the experimental results. Other nonidealities that are potential to cause differences between the experimental and simulated waveforms are (i) accuracies of the current and voltage measurements, (ii) measurement delays and resolution, (iii) numerical rounding inaccuracies in the microcontroller code, and (iv) queued operation of the AD conversions. For example, the rated current of the prototype is far below the nominal 50 A primary current of the LA 55-P current transducers. Based on the manufacturer's datasheet, the worst-case offset error is nearly 4.5 % of the nominal rectifier current amplitude. During the laboratory tests, it was observed that current measurements included a nonlinear error which could not be completely compensated by adjusting the measurement signal scaling and offset removal. The

magnitude of the measurement error was 2.7 % with 15 A and 3.7 % with 30 A test current.

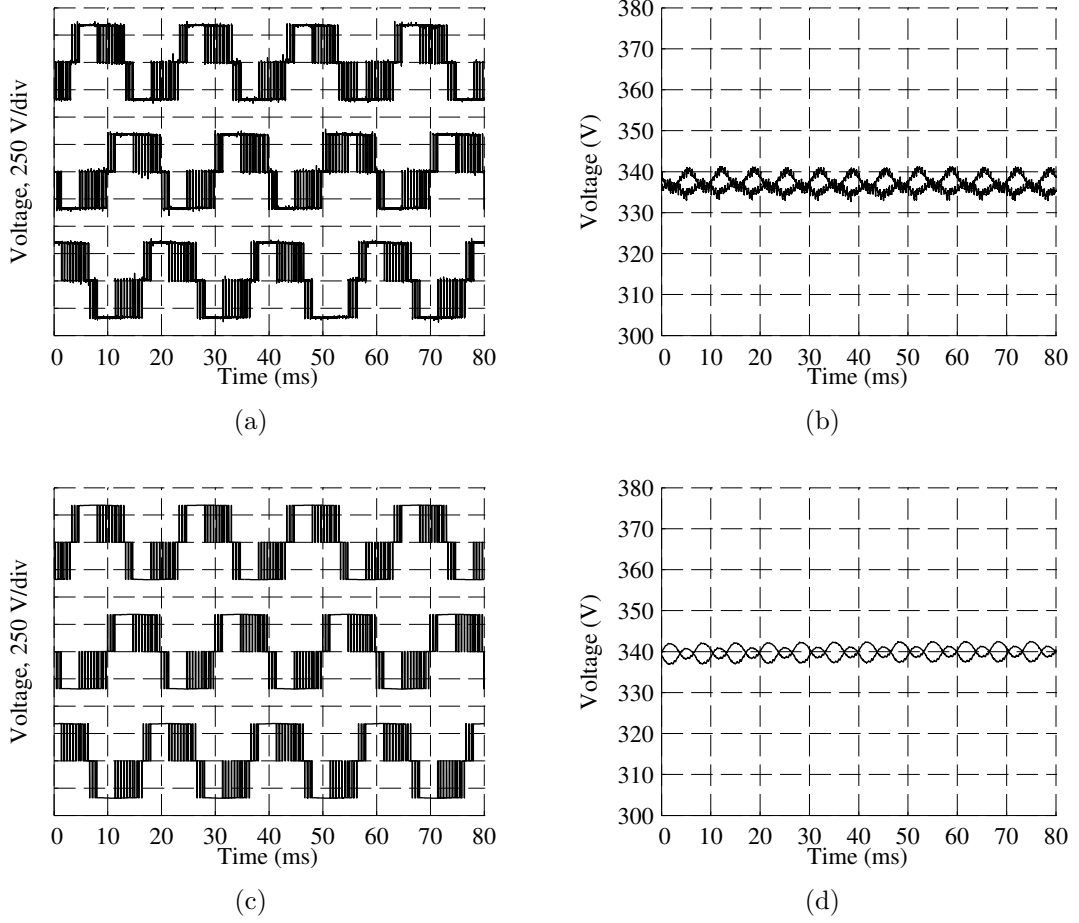


Fig. 6.5: (a) Experimental phase to DC bus midpoint voltages from top to bottom: u_{ao} , u_{bo} , u_{co} , (b) experimental DC capacitor voltages, (c)-(d) simulated waveforms.

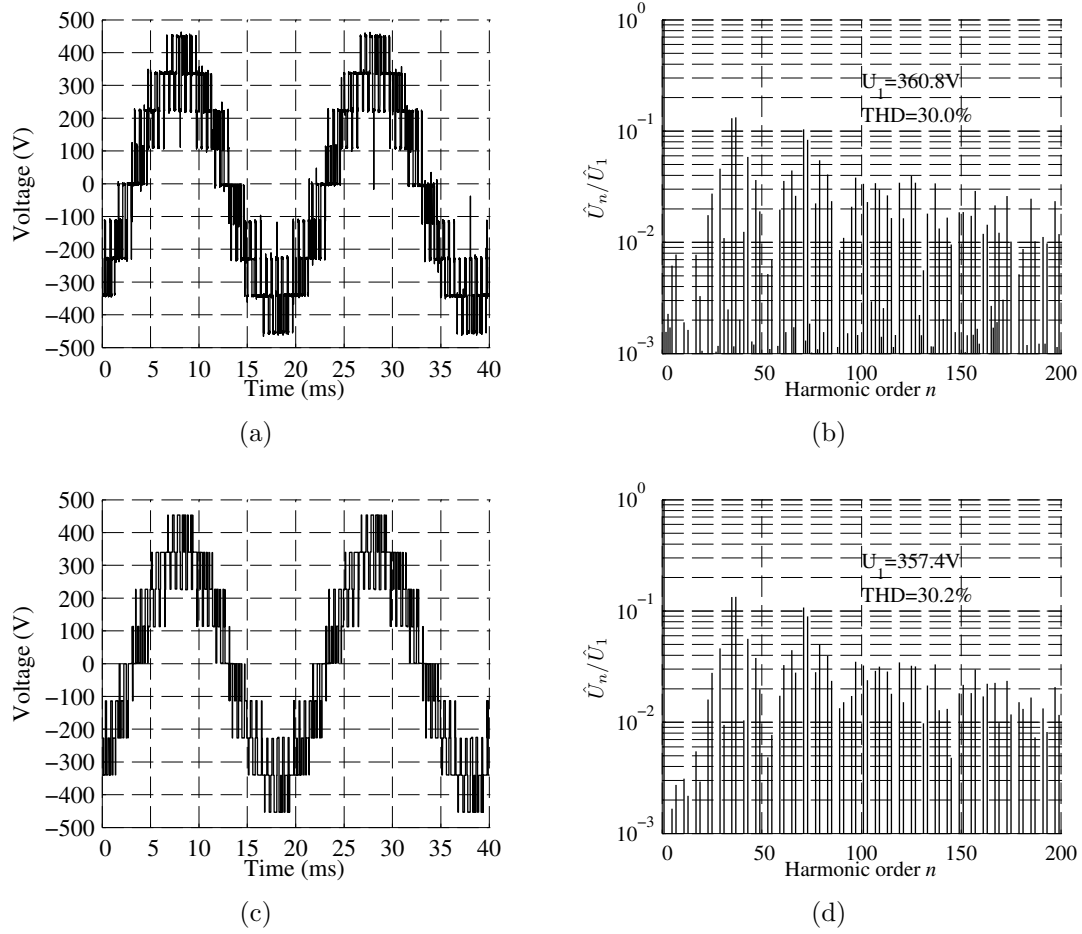


Fig. 6.6: (a)-(b) Experimental voltage u_{aN} and spectrum up to 10 kHz, (c)-(d) simulated waveform and spectrum.

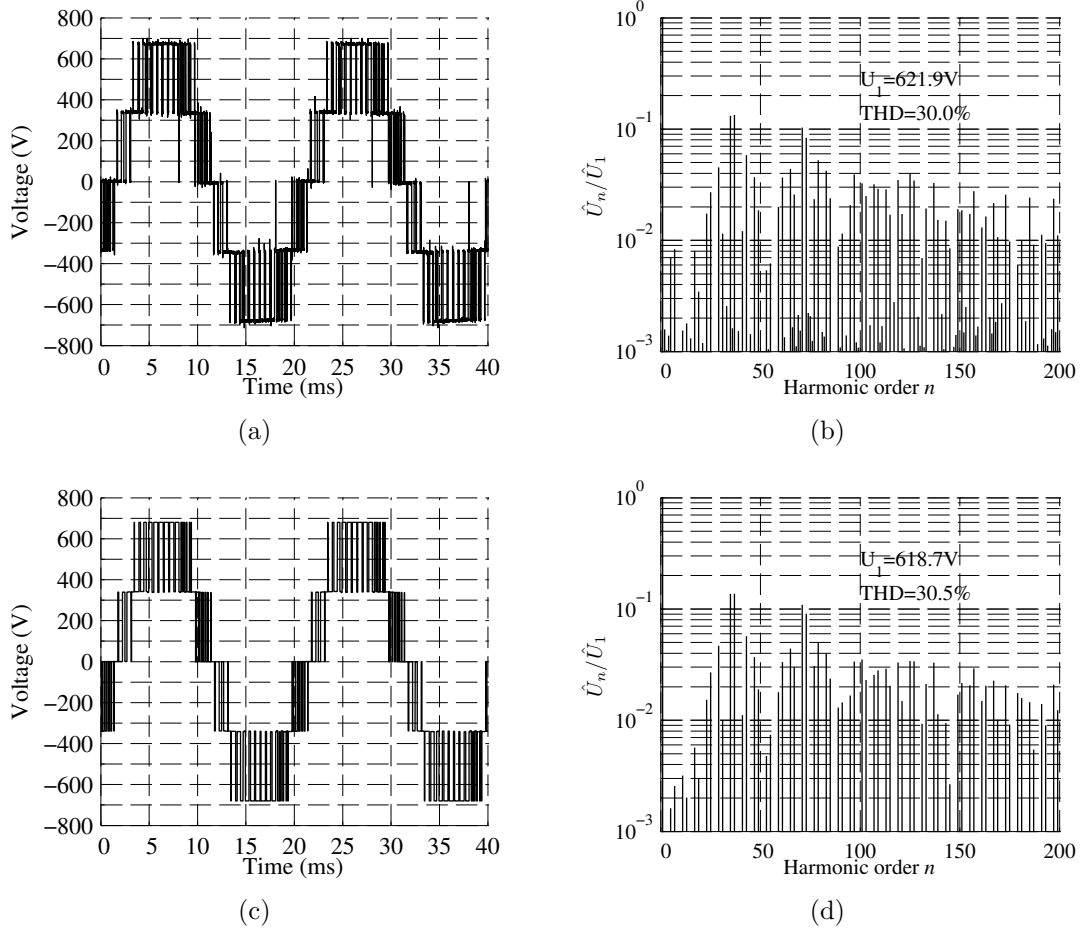


Fig. 6.7: (a)-(b) Experimental voltage u_{ab} and spectrum up to 10 kHz, (c)-(d) simulated waveform and spectrum.

6.3.2 DC capacitor voltage balancing

The simulated waveforms presented in Figs. 6.8(a)-6.8(c) exemplify the dynamics of the capacitor voltage balancing algorithm. The initial capacitor voltages are $u_{C1} = 260$ V and $u_{C2} = 420$ V. The DC bus voltage reference is 680 V and the STATCOM is controlled to generate 19 A of capacitive reactive current. The waveforms show that the control balances the capacitor voltages within approximately 1 s. The grid currents in the beginning of the simulation are depicted in Fig. 6.8(b), and in the end of the simulation in Fig. 6.8(c). Despite the capacitor voltage imbalance, the grid currents remain sinusoidal because the duty cycles solution algorithm compensates the effects of the neutral-point voltage variation on the rectifier output voltage.

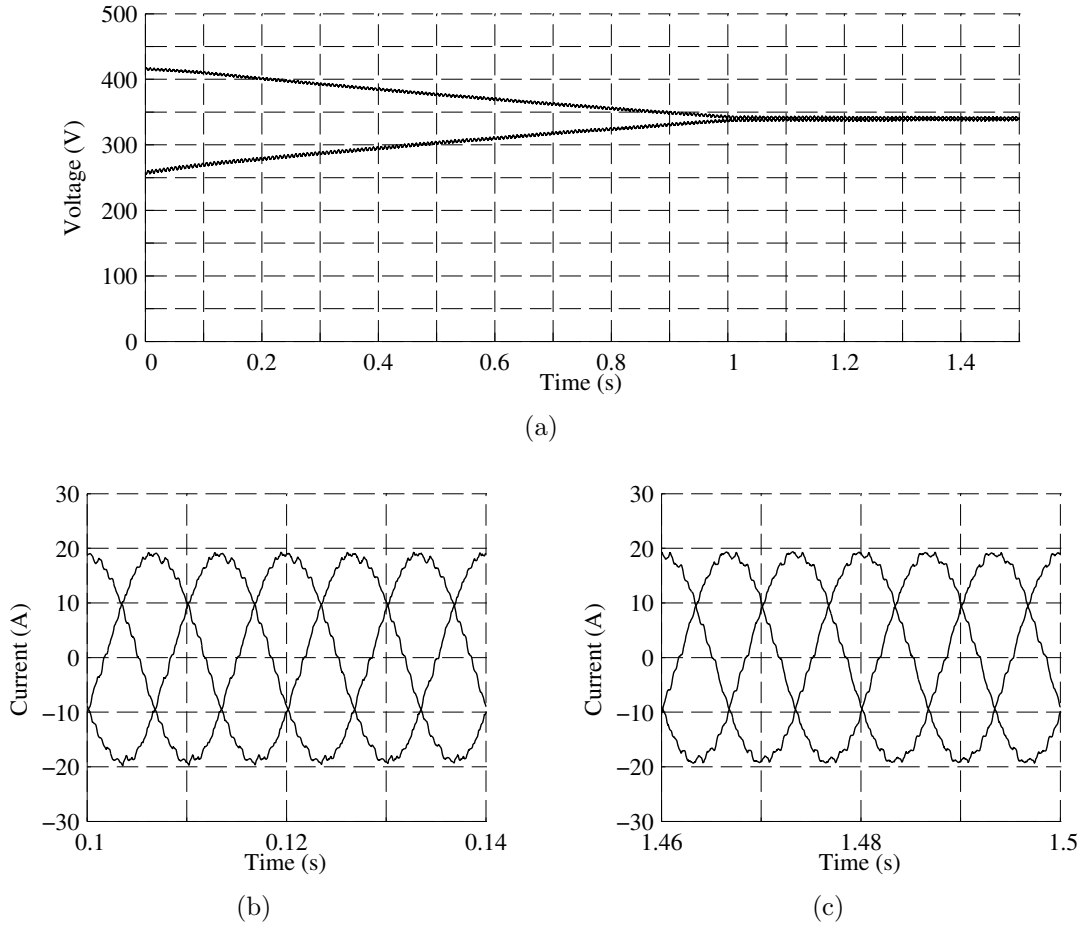


Fig. 6.8: Simulated operation of the capacitor voltage balancing algorithm. (a) Capacitor voltages. (b) Grid currents during $t = 0.1$ s...0.14 s, when the capacitor voltages are unbalanced. (c) Grid currents in the end of the simulation, during $t = 1.46$ s...1.5 s, when the capacitor voltages are balanced.

6.3.3 Switching sequence arrangement

Next, the operation of the proposed switching sequence arrangement method is demonstrated. The rectifier is controlled to generate 19 A (peak) of capacitive

reactive current and the PI current control strategy is enabled. The DC bus voltage reference is 680 V. Figs. 6.9(a) and 6.9(c) present the experimental current waveforms when the switching sequences are arranged to minimise the number of switched transitions during the transition between adjacent switching periods. The grid current oscillations are caused by the loss of PWM voltage waveform symmetry between two adjacent switching periods, as discussed in Chapter 4.

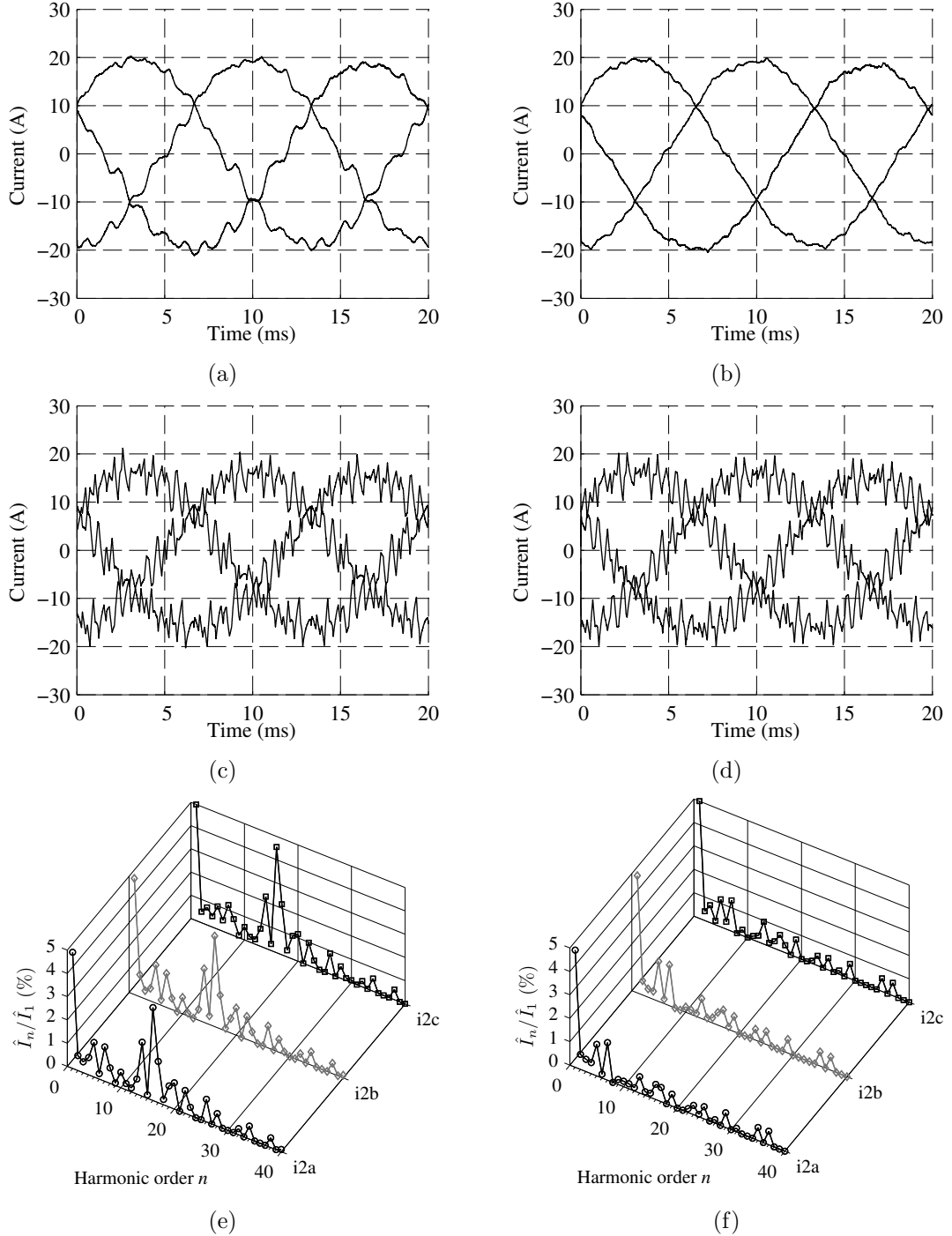


Fig. 6.9: Experimental grid currents and rectifier currents (a), (c) when the switched transitions are minimised and (b), (d) when the proposed design method is used. (e) Spectra of the currents in (a) up to 2 kHz. (f) Spectra of the currents in (b) up to 2 kHz.

In Figs. 6.9(b) and 6.9(d), the vector sequences are arranged in line with the design method proposed in Section 4.5. The grid current oscillation is significantly reduced. Figs. 6.9(e) and 6.9(f) present the frequency spectra of the grid currents. In Fig. 6.9(e) the THDs up to 2 kHz are $\text{THD}_{i_{2a}} = 6.1\%$, $\text{THD}_{i_{2b}} = 5.9\%$, $\text{THD}_{i_{2c}} = 6.4\%$. In Fig. 6.9(f) the THDs are $\text{THD}_{i_{2a}} = 2.9\%$, $\text{THD}_{i_{2b}} = 3.2\%$, $\text{THD}_{i_{2c}} = 2.8\%$. The results show that the increment of the THD is caused by the harmonics near the resonant frequency of the *LCL* filter circuit. The results prove the necessity to use the proposed arrangement method.

6.3.4 Nonlinearity compensation

In this section, the operation of the nonlinearity compensation function is demonstrated. During the simulations and experimental tests it was observed that the nonlinearities are causing only a minor steady-state error to the fundamental frequency grid current. Therefore, the operation of the nonlinearity compensation function is firstly demonstrated by means of a Simulink simulation, where the blanking times have been set longer than in the prototype, to give a better figure on the operation of the method. The simulation uses the following parameters: $i_{2q}^* = 21 \text{ A}$, $u_{\text{DC}}^* = 680 \text{ V}$, $T_{\text{d(on)},S1/S4} = 7 \mu\text{s}$, $T_{\text{d(off)},S1/S4} = 1 \mu\text{s}$, $T_{\text{d(on)},S2/S3} = T_{\text{d(off)},S2/S3} = 3.5 \mu\text{s}$. The threshold voltages of the rectifier bridge model are parametrised using the typical values of the SK75MLI066T modules: $U_{\text{CE0}} = 0.8 \text{ V}$, $U_{\text{F0,fwd}} = 1 \text{ V}$, and $U_{\text{F0,c}} = 1 \text{ V}$ [191].

Fig. 6.10 presents the simulated grid and the rectifier current waveforms which are obtained using the predictive vector current controller, and with the nonlinearity compensation function enabled and disabled. Without the compensation, a steady-state error remains in the grid currents. The error disappears when the nonlinearity compensation function is enabled. The steady-state error is caused by the blanking times and threshold voltage drops which deviate the actual rectifier voltage from the reference voltage. The voltage reference is an input of the state observer and should be equal to the actual rectifier voltage to avoid estimation errors.

In the prototype tests, the control software parameters are initialised using the typical threshold voltages of the SK75MLI066T modules and the switching delays described in Section 6.2. Fig. 6.11 presents the experimental results obtained using the predictive vector current controller with references $i_{2q}^* = 21 \text{ A}$ and $u_{\text{DC}}^* = 680 \text{ V}$. In Fig. 6.11(e), the THDs up to 2 kHz are $\text{THD}_{i_{2a}} = 5.1\%$ ($\hat{I}_{2a} = 18.7 \text{ A}$), $\text{THD}_{i_{2b}} = 4.6\%$ ($\hat{I}_{2b} = 19 \text{ A}$), $\text{THD}_{i_{2c}} = 4.3\%$ ($\hat{I}_{2c} = 18.9 \text{ A}$). In Fig. 6.11(f), the THDs are $\text{THD}_{i_{2a}} = 4.9\%$ ($\hat{I}_{2a} = 19.5 \text{ A}$), $\text{THD}_{i_{2b}} = 4.3\%$ ($\hat{I}_{2b} = 19.6 \text{ A}$), $\text{THD}_{i_{2c}} = 4.7\%$ ($\hat{I}_{2c} = 19.6 \text{ A}$).

According to the results, the amplitude of the fundamental grid current component increases slightly when the compensation method is enabled, because the estimation error caused by the switching delays and the threshold voltage drops reduces. Otherwise, the nonlinearity compensation function does not have a significant effect on the current waveforms. To some extent, the steady-state error of the grid current can be caused by the parametric uncertainty of the observer model, as revealed in

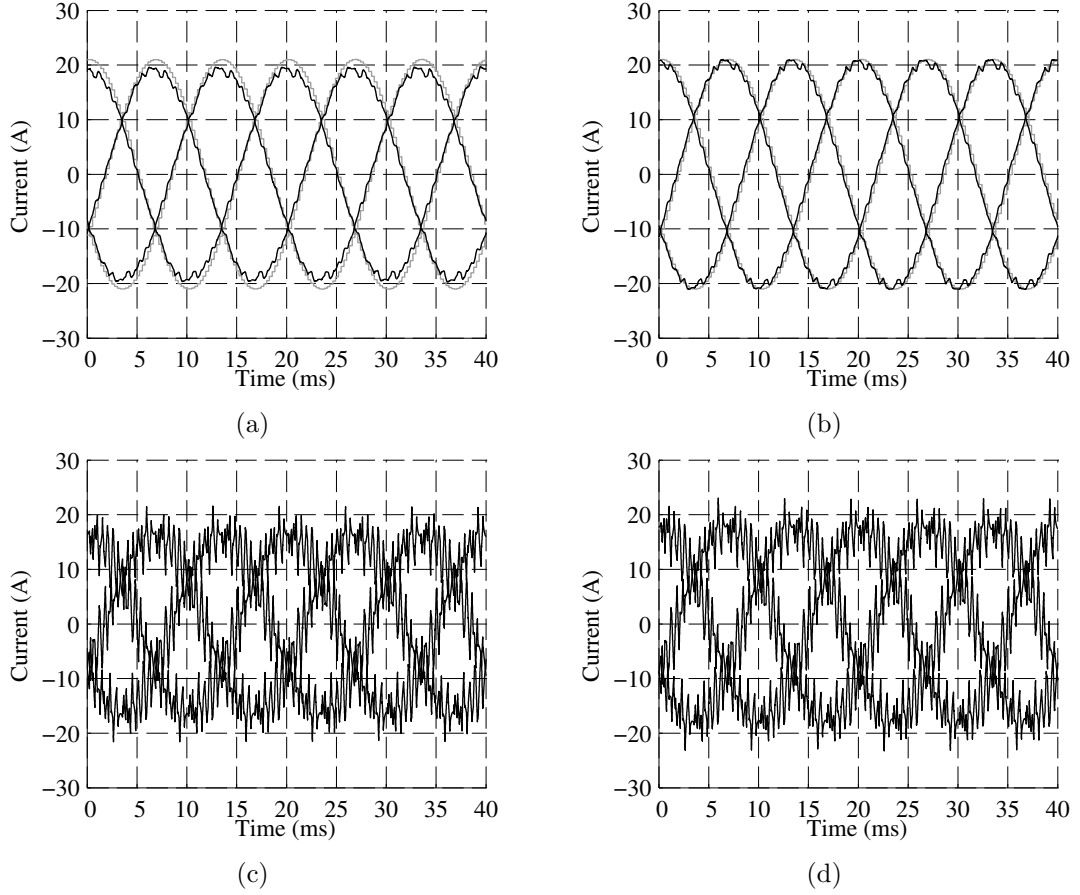


Fig. 6.10: Simulated grid currents and rectifier currents (a), (c) when the nonlinearity compensation function is disabled, and (b), (d) when the compensation function is enabled.

Chapter 5. Another possible reason for the steady-state error is the nonlinearity of the current transducers which could not be completely compensated by adjusting the measurement signal scaling and offset removal. The fifth harmonic present in the grid current waveforms is caused by the background grid voltage distortion.

The experimental tests support the simulation results. The steady-state grid current error is reduced when the nonlinearity compensation algorithm is enabled. Therefore the proposed algorithm could be beneficial in observer-based control applications. However, the algorithm should be optimised to reduce the computational burden. Moreover, the accuracies of the current polarity detection and the error voltage vector calculation should be analysed in detail.

6.4 Step-response tests

The dynamic behaviour of the grid current controllers is demonstrated with step-response tests. A step-change is programmed to occur in the q -axis current reference at the zero-crossing (- to +) of grid voltage u_{2a} . In the case of PI current control strategy, the references are $i_{1q}^* = 21\text{A}/-15\text{A}$. Furthermore, a -3A offset is added to

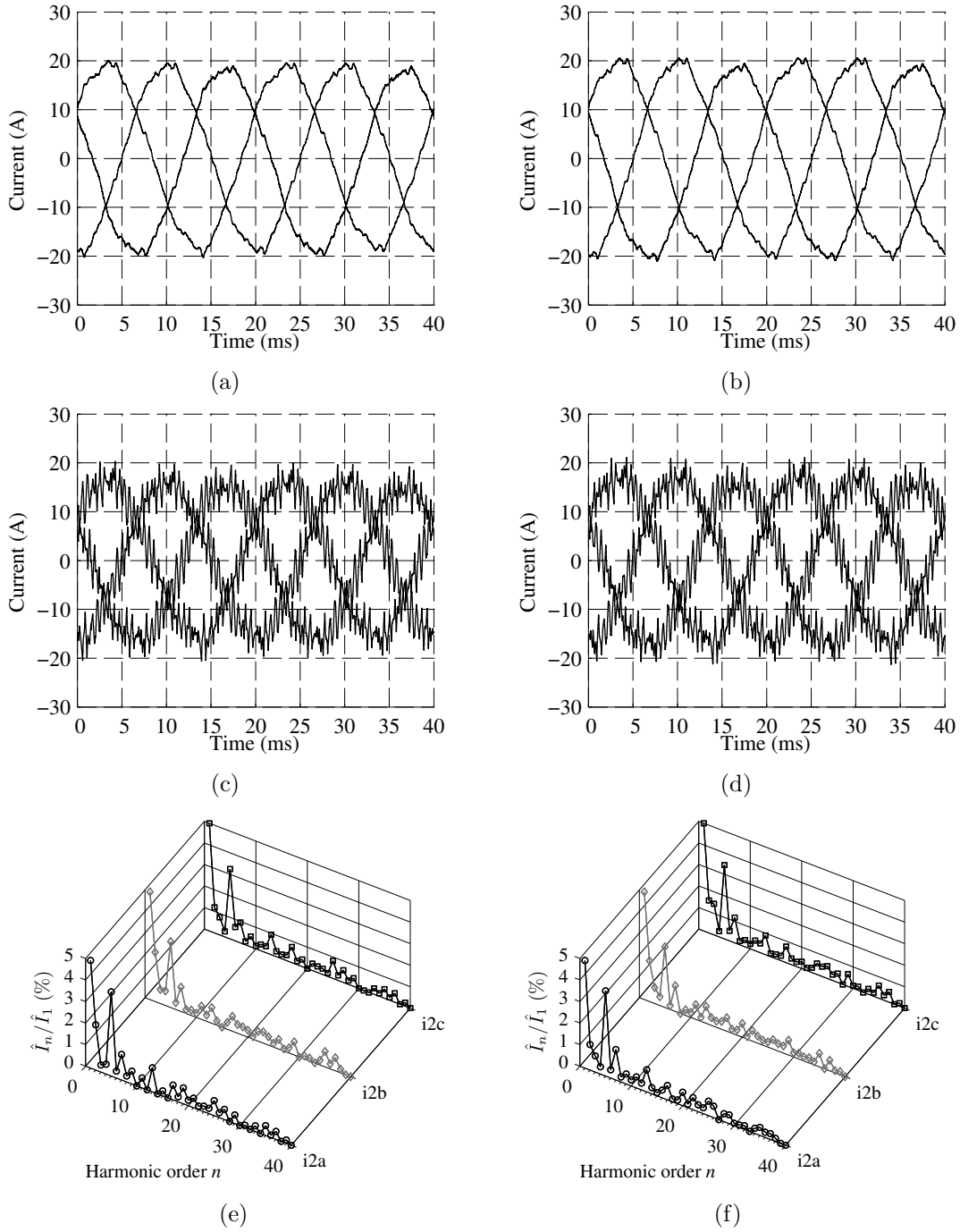


Fig. 6.11: Experimental grid currents and rectifier currents when (a), (c) the nonlinearity compensation function is disabled and when (b), (d) the compensation function is enabled. (e) Spectra of the currents in (a) up to 2 kHz. (f) Spectra of the currents in (b) up to 2 kHz.

i_{1q}^* to compensate the reactive current drawn by the LC filter. The q -axis references for the predictive vector current controller (PVCC) are $i_{2q}^* = 21 \text{ A} / -15 \text{ A}$. This way the both control schemes yield approximately the same grid and rectifier current amplitudes. The DC bus voltage reference is 680 V during the tests. The controllers are parametrised similarly as described in Chapter 5.

Fig. 6.12 presents the step responses of the three-phase grid currents. The waveforms have been filtered with DLPFs ($f_c = 100$ kHz) to remove the measurement noise. It can be seen that the step responses are nearly similar in terms of rise-time. Fig. 6.13 illustrates the normalised amplitude spectra of the steady-state grid and rectifier currents. The waveforms obtained with the PI current control strategy contain harmonics near the LCL filter resonance which implies poorer resonance damping compared with the PVCC. The same observation was made in Chapter 5 based on the dynamic models. By contrast, the amplitude spectra of the predictive controllers contain more low frequency harmonics, namely the 5th and the 7th. The amplitudes of 50 Hz current components and the THDs up to 5 kHz are presented in Table 6.2. The current THDs obtained with the PVCC are higher compared with the PI current control because of the low-frequency harmonics and slightly smaller fundamental frequency component.

Table 6.2: The amplitudes of 50 Hz current components (capacitive and inductive) and the THD in the range of 50 Hz to 5 kHz.

	PI control		PI control + Smith		PVCC		PVCC + Smith	
	Cap.	Ind.	Cap.	Ind.	Cap.	Ind.	Cap.	Ind.
\hat{I}_{1a} (A)	17.2	17.4	17.3	17.4	16.3	16.8	16.7	17.0
THD(%)	14.7	19.0	17.6	19.1	18.6	19.6	18.0	19.3
\hat{I}_{1b} (A)	17.1	17.7	17.1	17.7	16.1	17.4	16.5	17.5
THD(%)	16.8	18.5	16.3	18.6	18.1	18.9	17.6	18.8
\hat{I}_{1c} (A)	17.0	17.6	17.1	17.6	16.3	16.9	16.7	17.2
THD(%)	15.5	18.7	16.1	18.7	19.7	19.3	19.5	19.0
\hat{I}_{2a} (A)	20.0	14.1	20.1	14.2	19.2	13.6	19.6	13.8
THD(%)	3.3	4.8	3.4	5.0	5.0	6.2	4.6	5.6
\hat{I}_{2b} (A)	20.3	14.8	20.3	14.8	19.3	14.5	19.7	14.6
THD(%)	3.5	4.5	3.4	4.8	4.2	5.4	3.9	5.3
\hat{I}_{2c} (A)	20.1	14.5	20.2	14.5	19.3	13.9	19.8	14.2
THD(%)	3.4	4.3	3.5	4.4	4.7	5.3	4.5	5.0

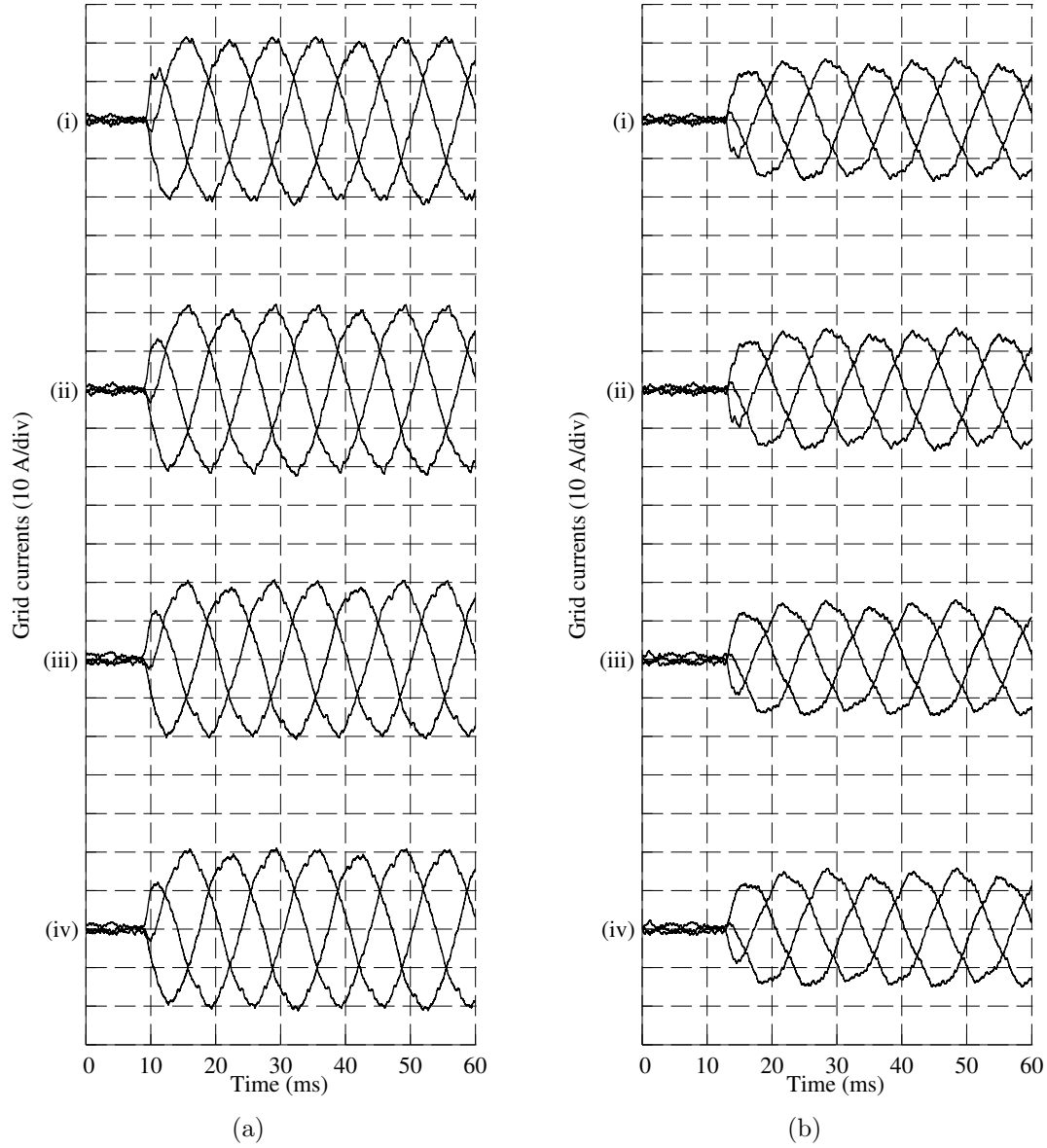


Fig. 6.12: Experimental grid current responses to (a) positive and (b) negative step-change of q -axis reference; (i) PI current control, (ii) PI current control with the Smith predictor, (iii) PVCC, (iv) PVCC with the Smith predictor.

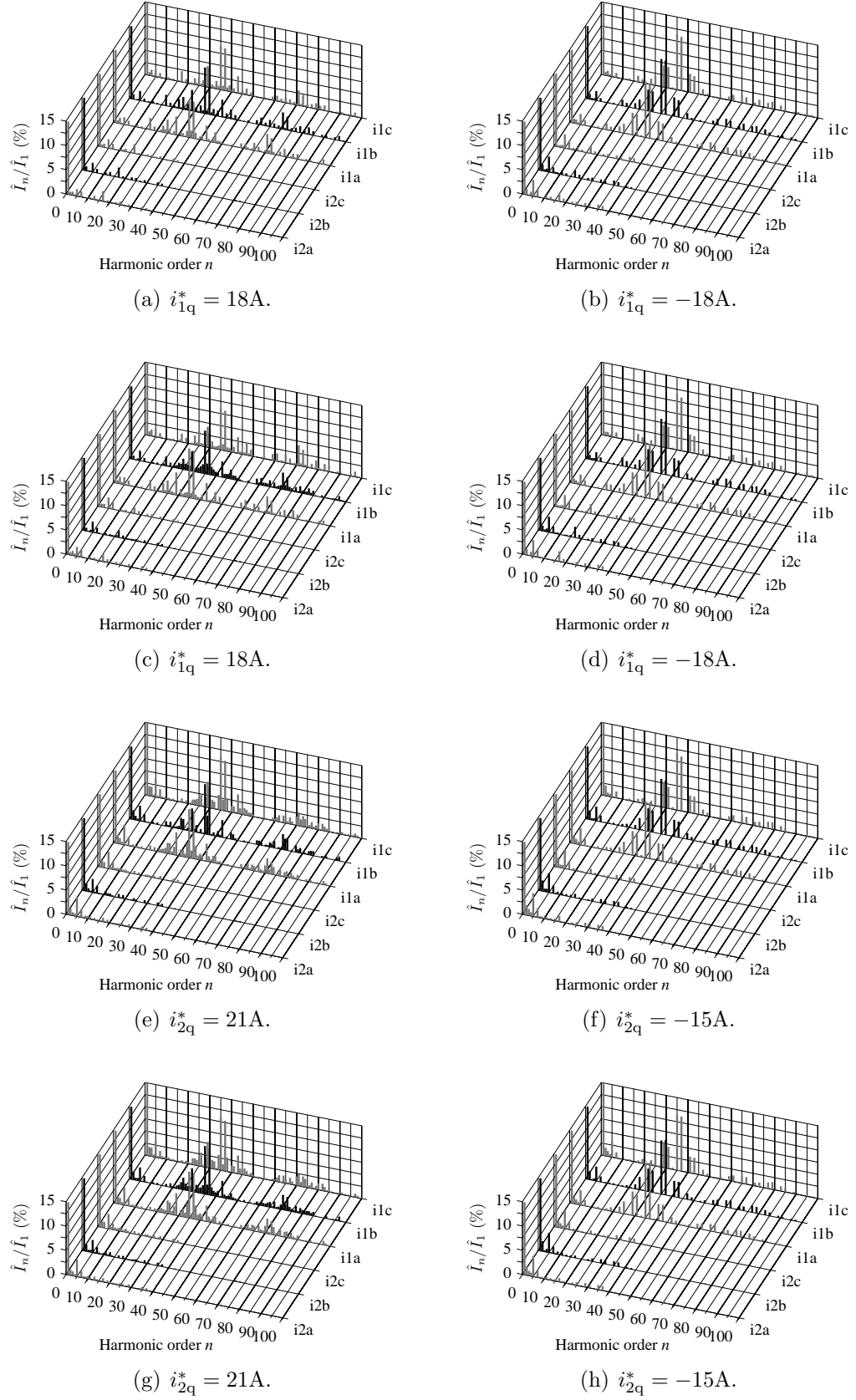


Fig. 6.13: Frequency spectra of the currents. (a)-(b) PI current control, (c)-(d) PI current control with the Smith predictor, (e)-(f) PVCC, (g)-(h) PVCC with the Smith predictor.

Figs. 6.14 to 6.17 present the step responses of the grid currents in the dq reference frame. It can be seen that a steady-state error remains in the responses of predictive vector current controllers. Similar behaviour was detected in the average models analysed in Chapter 5. Regarding the average models, the error was caused by the parametric uncertainty of the process model, which resulted in an estimation error. In the case of prototype tests, also the nonlinearity of the current transducers and other measurement errors, inaccuracy in the nonlinearity compensation, and numerical rounding errors in the software code can contribute to the final error.

All the grid current responses presented in Figs. 6.14 to 6.17 include a 300 Hz oscillation in both the d and the q axis current. The oscillation is caused by the 5th (negative sequence) and the 7th (positive sequence) three-phase harmonics which superimpose on the 6th harmonic frequency in the synchronous reference frame. Fig. 6.18 presents the phase-to-neutral grid voltage waveforms at the STATCOM's connection point, the voltage waveforms in the dq reference frame, and the phase voltage FFTs. The 300 Hz component is present in Figs. 6.18(b) and 6.18(c) which verifies that the grid voltages contain the 5th and the 7th harmonics. The result implies that the low frequency grid current harmonics are caused by the background grid voltage distortion. The grid current FFTs in Fig. 6.13 show that the amplitude of the 300 Hz oscillation is larger in the case of PVCCs, when compared to the PI current controls. As a result, the PVCCs yield inferior disturbance rejection capability. Similar behaviour was predicted based on the frequency response analyses performed in Chapter 5, which indicates that the dynamic models captured the behaviour of the experimental system with a sufficient accuracy.

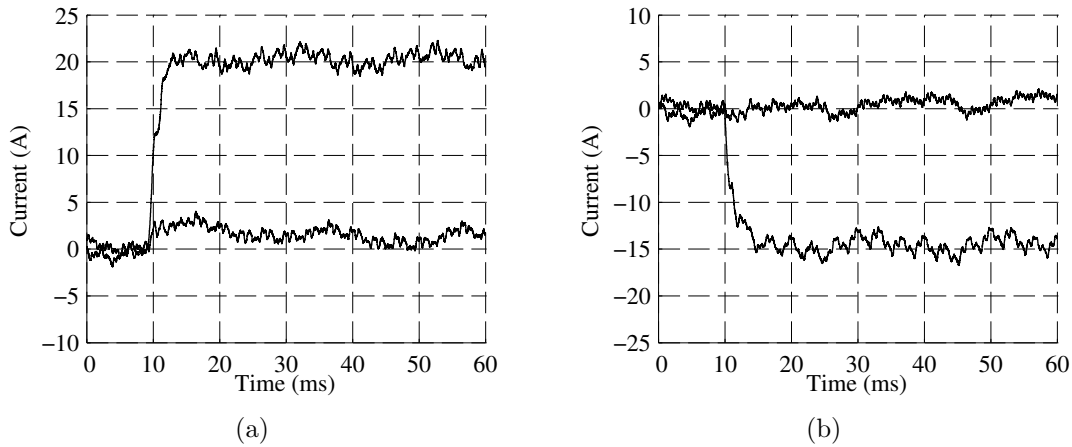


Fig. 6.14: The grid current response to the (a) positive and (b) negative step-change of i_{lq}^* in the case of PI current control strategy.

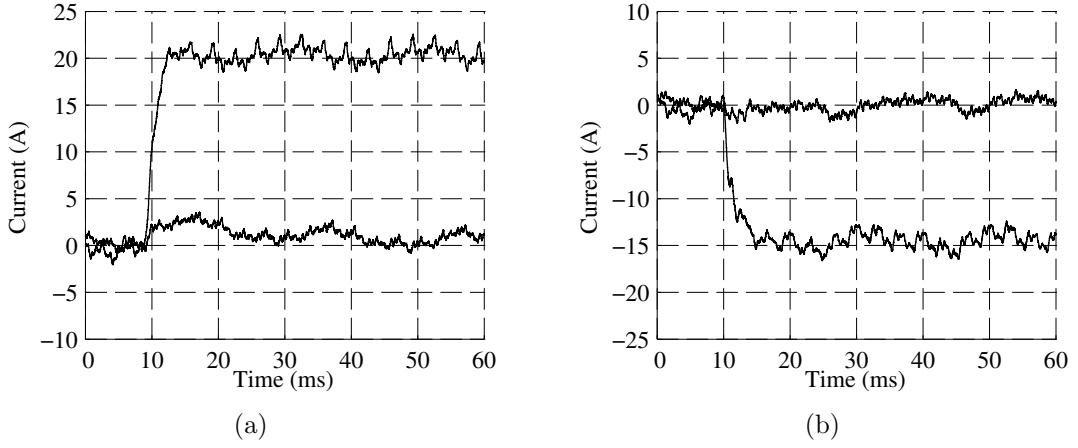


Fig. 6.15: The grid current response to the (a) positive and (b) negative step-change of i_{1q}^* in the case of PI current control strategy with the Smith predictor.

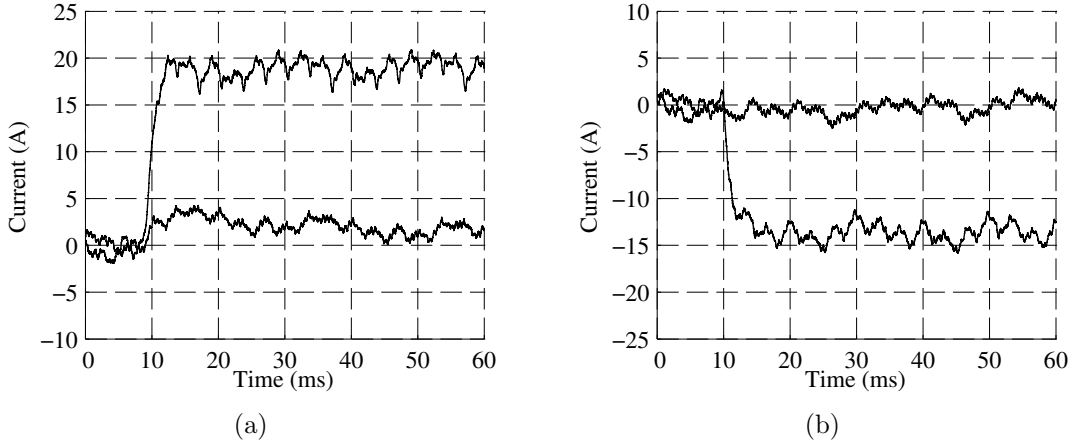


Fig. 6.16: The grid current response to the (a) positive and (b) negative step-change of i_{2q}^* in the case of predictive vector current control scheme.

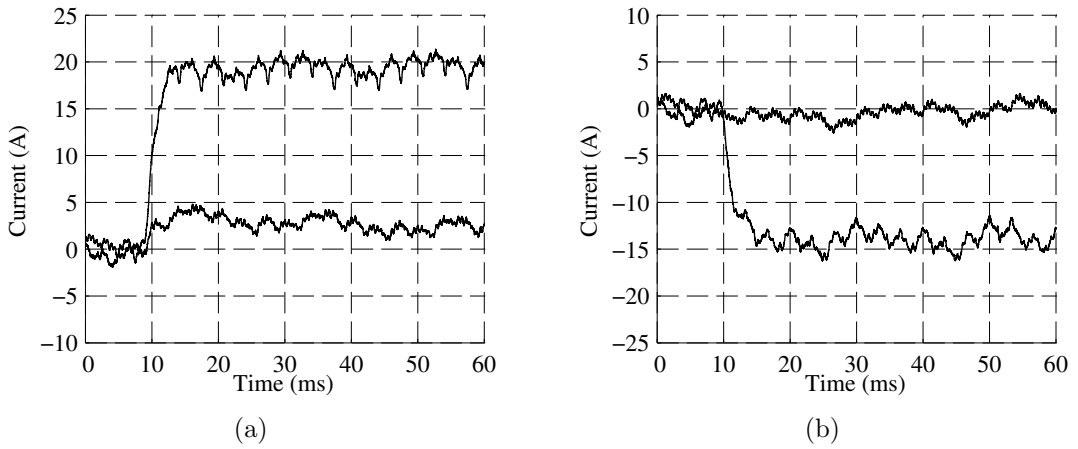


Fig. 6.17: The grid current response to the (a) positive and (b) negative step-change of i_{2q}^* in the case of predictive vector current control scheme with the Smith predictor.

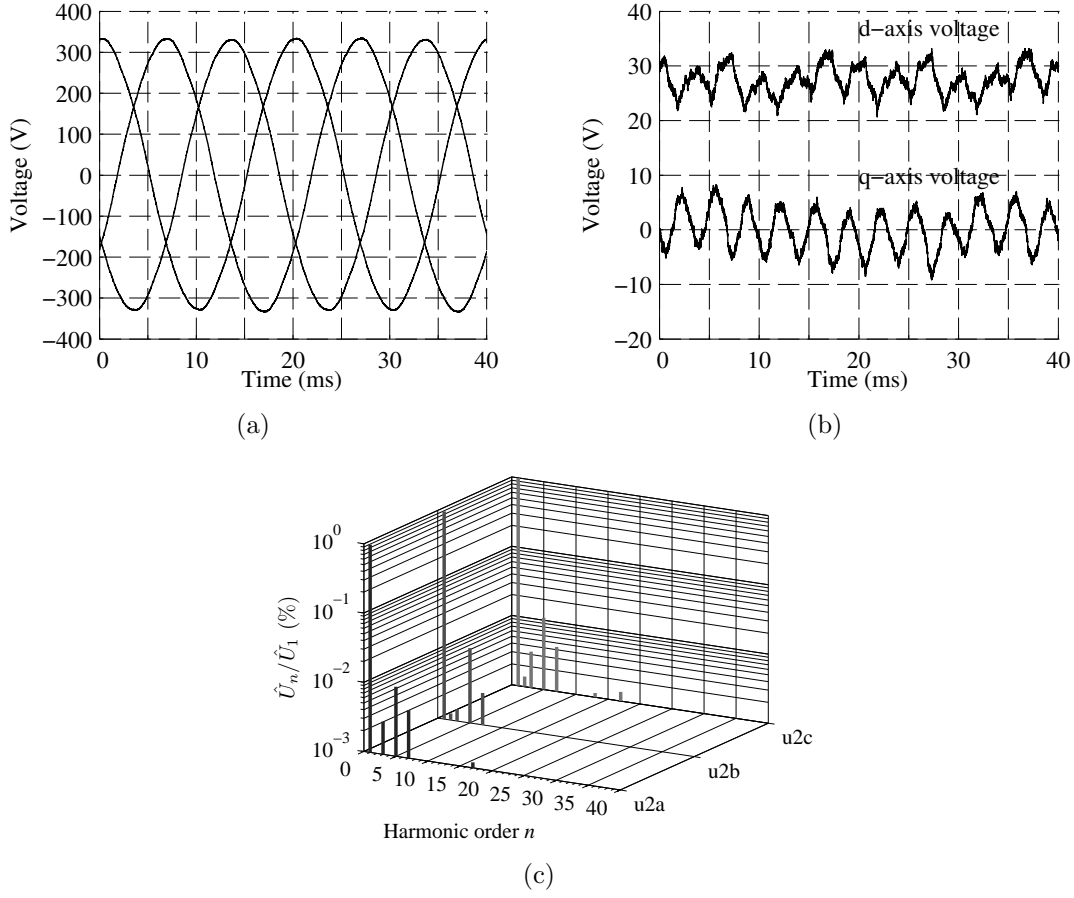


Fig. 6.18: Grid voltage at the STATCOM's connection point. (a) Three-phase voltages. (b) Grid voltage components in the synchronous reference frame (d -axis offset: -300 V). (c) Frequency spectra of the phase voltages. The fundamental frequency amplitudes and the THDs up to 2 kHz; $\hat{U}_{1a} = 328.1$ V, THD = 1.21%; $\hat{U}_{1b} = 327.2$ V, THD = 1.29%; $\hat{U}_{1c} = 329.6$ V, THD = 1.27%.

6.5 Conclusions

The steady-state test results of the 10 kVA three-level STATCOM prototype revealed that the modulation algorithm operates as intended. Moreover, the simulated waveforms showed a good match with the experimental results. Secondly, the dynamics of the capacitor voltage balancing algorithm was revealed with simulations. The results showed that the balancing algorithm eliminates the average neutral-point voltage offset. The grid currents remained sinusoidal, despite the voltage imbalance, because the duty cycles solution algorithm compensates the effects of the neutral-point voltage offset. Thirdly, the effect of switching sequence arrangement on the grid current waveforms was demonstrated. It was shown that the minimisation of switched transitions excites the *LCL* filter resonance which distorts the grid current waveform. Sinusoidal grid currents were achieved when the proposed switching sequence arrangement method was enabled. The results verify the usefulness of the proposed method.

After that, it was shown with Simulink simulations that the blanking times and semiconductor threshold voltage losses cause an estimation error which creates a steady-state error in the grid current. The error was eliminated when the proposed nonlinearity compensation algorithm was enabled. In the simulations, the blanking times were set longer than in the laboratory prototype to give a better picture on the performance of the compensation method. In the experimental tests, the fundamental frequency grid current increased slightly when the nonlinearity compensation method was enabled. However, the steady-state grid current error was not completely eliminated because of other nonidealities in the prototype setup. It was concluded that the remaining error is at least partially caused by the inaccuracies of the observer model and the measurement signals. Furthermore, the implemented compensation algorithm considered only the semiconductor voltage losses caused by the threshold voltages.

Finally, the dynamic behaviour of the current controllers was examined with step response tests. The response times of the controllers were quite similar. The steady-state current waveforms obtained with the PI current control strategy included a harmonic component near the *LCL* filter resonant frequency. Similar characteristic was shown by the dynamic models studied in Chapter 5. The controllers were incapable to reject the fifth and the seventh harmonics present in the grid voltage. The disturbance rejection capability of the predictive vector current control scheme was inferior to that of the PI current control strategy. The result agrees with the behaviour of the dynamic models studied in Chapter 5.

In conclusion, the results of this chapter confirm that the objectives of the thesis, presented in Chapter 1, are fulfilled. However, there is clearly a need for further investigation and improving of the control algorithms. For example, the observer sensitivity to modelling errors should be reduced and the current controllers' capability to reject background grid voltage distortion should be improved.

Chapter 7

Conclusions

7.1 Summary

The dynamic behaviour of a static reactive power compensator (STATCOM) is primarily determined by the control which reacts based on the internal measurements taken from the converter and the external measurements taken from the network. According to the open literature, the two core control functions are pulse-width modulator and grid current control, which include a variety of important and challenging research problems. Considering high power STATCOM applications, the multilevel converter topologies have gained special interest because they can generate low-harmonic voltage and current waveforms by using lower switching frequencies and with no need for complex transformer circuits.

This thesis focused on the digital control of a STATCOM based on the three-wire three-level neutral-point-clamped rectifier. The goal was to investigate the problems affiliated with the pulse-width modulation and grid current control, by using a suitable combination of fundamental theory, computer-aided modelling and simulations, and laboratory experiments. The objectives of the thesis were defined as follows: (i) To implement a discontinuous space-vector modulation algorithm that compensates the voltage errors caused by blanking times, semiconductor voltage losses, and capacitor voltage imbalance, and also controls the capacitor voltage balance. Also the switching sequence arrangement was to be studied. (ii) To study the dynamic behaviour of two grid current control strategies and the effects of a control delay compensation algorithm. (iii) To verify the theoretical considerations using simulations and laboratory experiments.

Chapter 1 starts with an introduction to power quality problems and gives an overview on the development of power quality conditioners. After that, the status of the research on STATCOMs based on multilevel converters was provided. Thirdly, an overview on the STATCOM control was given, and it can be said to consist of six functional layers, namely (i) the system control, (ii) the application control, (iii) the converter control, (iv) the switching control, (v) the hardware con-

trol. The task and the main functions of each layer were described. Also, the main categories of grid current control strategies and pulse-width modulation methods were introduced.

Chapter 2 provided the theoretical background of the three-level neutral-point-clamped rectifier. The voltage errors caused by blanking times and voltage losses across the power semiconductors were described and their compensation strategies were reviewed. After that, the fundamentals of three-level discontinuous space-vector modulation were reviewed. The switching patterns used in this thesis were presented and the theories behind duty cycles computation and reference length limiting were studied. Finally, the STATCOM vector control scheme studied in this thesis and the main control functions were presented. Also, the effects of control delays and their compensation were discussed.

In Chapter 3, an average dynamic model of the STATCOM under study was presented. The frequency characteristics of the filter inductors were modelled with Foster equivalent circuits. The grid impedance was included in the models to study the effects of nonideal network. The models are used in Chapter 5 to analyse the grid current control loop.

The implemented discontinuous space-vector modulation algorithm was presented in Chapter 4. The applied duty cycle solution algorithm compensates the effects of neutral-point voltage variation on the PWM voltage. The capacitor voltage balancing was implemented by varying the phase-leg discontinuity patterns. The method enables neutral-point voltage balancing on the average basis. After that, the arrangement of adjacent three-vector combinations was studied. It was shown that the minimisation of the number of the switched transitions does not retain the symmetry of the PWM voltage waveform and, therefore, is prone to increase the grid current distortion. An alternative arrangement method was proposed to retain the waveform symmetry and its effect was analysed. Finally, an algorithm was proposed which compensates the voltage error caused by blanking times and voltage losses across the power semiconductors of the rectifier bridge.

Chapter 5 analysed the dynamic behaviour of two grid current control strategies using the models developed in Chapter 3. A problem common to the both controllers was poor capability to reject the low-order grid voltage harmonics. In the case of PI current control strategy, the resonant poles were located near to the unit circle, which can cause oscillatory responses or even lead to instability. The predictive vector current controller provided faster response times but the observer was sensitive to modelling errors which is a major drawback. After that, the Smith predictor was included in the controllers and its effect was analysed. The predictor mitigated the oscillatory behaviour of the PI current control strategy and eliminated the overshoot of the predictive vector current controller. However, the observer's sensitivity to parametric uncertainties hindered the feasibility of the predictor. Finally, it was shown that the grid impedance variations have a significant effect on the control dynamics. If the performance is optimised at a single operating point, a change in the network condition can yield unexpected dynamic behaviour, even instability.

Chapter 6 presented the simulation results and the test results of 10 kVA three-level STATCOM prototype. Firstly, the operation of the modulator was tested and it was shown to operate as intended. After that, it was revealed that the proposed switching sequence arrangement method yields better grid current waveform compared to the conventional arrangement method preferred in open literature, which minimises the number of the switched transitions. Thirdly, it was verified that the proposed nonlinearity compensation algorithm is capable to reduce the steady-state error in the grid current when the studied predictive controller is used. Finally, the dynamic behaviour of the grid current controllers was experimented. They provided quite similar responses to the step-change of q -axis current reference but could not reject the low-order harmonics that were present in the grid voltage. Furthermore, in the case of predictive vector current controller, a steady-state error remained in the grid current. The observed shortcomings were predicted using the dynamic models developed for the STATCOM, which proves that the studied system was modelled with a reasonably good accuracy.

7.2 Future research topics

The research carried out as a part of this thesis elucidated various questions that could be the potential future research topics. By way of examples, some interesting problems and research questions are highlighted below:

- The proposed switching sequence arrangement method improved the voltage and current waveforms but was not optimal. How to minimise the distortion and optimise the switching sequence arrangement? Also, the common-mode voltage generated by the modulation should be studied in detail.
- One challenge of nonlinearity compensation methods is the accuracy of the current polarity detection. At low output current and during the zero-crossings, the polarity can change multiple times during a control update interval which complicates the compensation. This issue requires further research.
- How to improve the grid current controllers' capability to reject the background grid voltage distortion? Also, how to improve the observer's robustness and decrease its sensitivity to modelling errors and grid impedance variation? Alternative observer structures should be studied.
- The impacts of the DC voltage control loop and the phase-locking loop on the dynamic behaviour of the STATCOM should be studied. Furthermore, the dynamics of the STATCOM in distorted and unbalanced grids, and during network faults, should be studied and tested.

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Appendix A

Reference frame transformations

The Clarke transformation

Arbitrary time-variant three-phase quantities x_a , x_b , x_c can be expressed as a complex vector \vec{x} in the stationary $\alpha\beta$ coordinates, see Fig. A.1(a), by using the Clarke transformation [192]

$$\vec{x} = c_1(x_a e^{j0} + x_b e^{j\frac{2\pi}{3}} + x_c e^{j\frac{4\pi}{3}}) = x_\alpha + jx_\beta \quad (\text{A.1})$$

where c_1 is used for normalisation and e^{j0} , $e^{j\frac{2\pi}{3}}$, and $e^{j\frac{4\pi}{3}}$ denote unit vectors. The amplitude invariant transformation is achieved with $c_1 = \frac{2}{3}$ and has been used in this thesis. Alternatively, the power invariant transformation is achieved with $c_1 = \sqrt{\frac{2}{3}}$ [193]. The zero-sequence component is lost during the transformation (A.1) and must be calculated separately

$$x_0 = c_2(x_a + x_b + x_c) \quad (\text{A.2})$$

where $c_2 = \frac{1}{3}$ for the amplitude invariant transformation and $c_2 = \frac{1}{\sqrt{3}}$ for the power invariant transformation.

In matrix form, the Clarke transformation and its inverse with $c_1 = \frac{2}{3}$ are

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} = c_1 \mathbf{T}_{\alpha\beta 0} \begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} \quad (\text{A.3})$$

$$\begin{bmatrix} x_a \\ x_b \\ x_c \end{bmatrix} = c_1^{-1} \mathbf{T}_{\alpha\beta 0}^{-1} \begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} \quad (\text{A.4})$$

$$\mathbf{T}_{\alpha\beta 0} = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}, \mathbf{T}_{\alpha\beta 0}^{-1} = \begin{bmatrix} \frac{2}{3} & 0 & \frac{2}{3} \\ -\frac{1}{3} & \frac{1}{\sqrt{3}} & \frac{2}{3} \\ -\frac{1}{3} & -\frac{1}{\sqrt{3}} & \frac{2}{3} \end{bmatrix} \quad (\text{A.5})$$

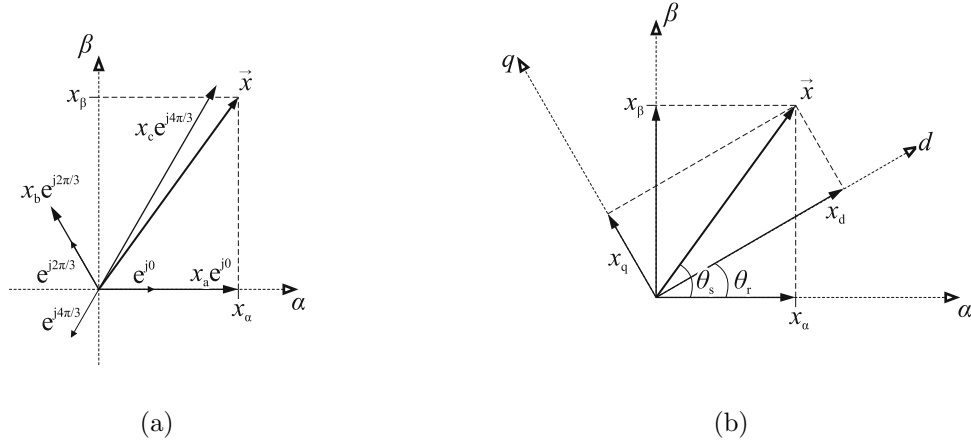


Fig. A.1: (a) The Clarke transformation, (b) the Park transformation

The Park transformation

The Park transformation, depicted in Fig. A.1(b), converts a vector from one orthogonal reference frame to another. The phase angle of the new reference frame can be tied to a given variable such as voltage or current [194]. The benefit of the transformation is that the vectors rotating at the angular frequency of the reference frame are constants.

Let us consider a vector $\vec{x}_s = x_\alpha + jx_\beta = \|\vec{x}_s\|e^{j\theta_s}$ where θ_s is the angle with respect to the α axis. In Fig. A.1(b), the vector \vec{x}_s is transformed into new orthogonal reference frame 'r' as follows

$$\vec{x}_r = \|\vec{x}\|e^{j\theta_s}e^{-j\theta_r} = \vec{x}_s e^{-j\theta_r} = x_d + jx_q \quad (\text{A.6})$$

where θ_r is the angle between the reference frames 'r' and 's'. In matrix form, the $dq0$ transformation and its inverse are

$$\begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} = \mathbf{T}_{dq0} \begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} \quad (\text{A.7})$$

$$\begin{bmatrix} x_\alpha \\ x_\beta \\ x_0 \end{bmatrix} = \mathbf{T}_{dq0}^{-1} \begin{bmatrix} x_d \\ x_q \\ x_0 \end{bmatrix} \quad (\text{A.8})$$

$$\mathbf{T}_{dq0} = \begin{bmatrix} \cos \theta & \sin \theta & 0 \\ -\sin \theta & \cos \theta & 0 \\ 0 & 0 & 1 \end{bmatrix}, \quad \mathbf{T}_{dq0}^{-1} = \begin{bmatrix} \cos \theta & -\sin \theta & 0 \\ \sin \theta & \cos \theta & 0 \\ 0 & 0 & 1 \end{bmatrix} \quad (\text{A.9})$$

The gh transformation

The transformation of $\vec{x} = x_\alpha + jx_\beta$ into gh coordinates, where the h -axis is in 60° angle regarding the horizontal g -axis, is given as

$$\begin{bmatrix} x_g \\ x_h \end{bmatrix} = c \begin{bmatrix} 1 & -\frac{1}{\sqrt{3}} \\ 0 & \frac{2}{\sqrt{3}} \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \quad (\text{A.10})$$

where the coefficient c is used for normalisation. A modification of (A.10) rotates the vector between $0 \dots 60^\circ$ of the coordinate system, and is given as follows

$$\begin{bmatrix} x_g \\ x_h \end{bmatrix} = c \begin{bmatrix} \frac{2}{\sqrt{3}} \sin(\frac{\pi}{3} - (\theta - k\frac{\pi}{3})) \\ \frac{2}{\sqrt{3}} \sin(\theta - k\frac{\pi}{3}) \end{bmatrix} \begin{bmatrix} x_\alpha \\ x_\beta \end{bmatrix} \quad (\text{A.11})$$

where k is the number of the 60° rotations applied on \vec{x} , and c is used for normalisation. Eq. (A.11) can be used to simplify the space-vector modulation algorithms, because it reduces all the computations to Sector 1 of the voltage hexagon [133, 141]. Fig. A.2 depicts graphically both (A.10) and (A.11). The subscripts 'rot' highlight the variables associated with (A.11).

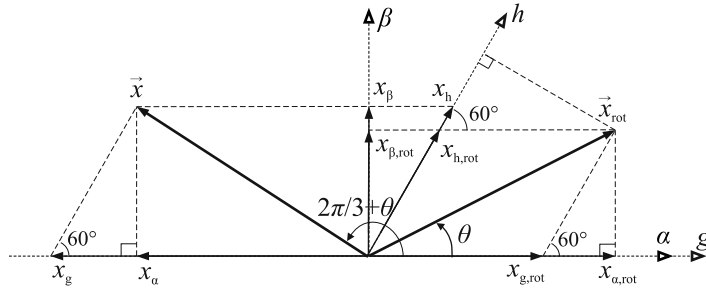


Fig. A.2: Two versions of the gh transformation.

Transformations using 60° symmetry

Stationary $\alpha\beta$ coordinates

Fig. A.3 shows six vectors in the $\alpha\beta$ reference frame. The angle between two adjacent vectors is 60° . Based on (A.6), any of the six vectors can be used to express the other five as follows

$$\vec{x}_{m \rightarrow n} = \frac{2}{3} (x_a e^{j0} + x_b e^{j\frac{2\pi}{3}} + x_c e^{j\frac{4\pi}{3}}) e^{-jk\frac{\pi}{3}} = \vec{x}_m e^{-j(m-n)\frac{\pi}{3}} \quad (\text{A.12})$$

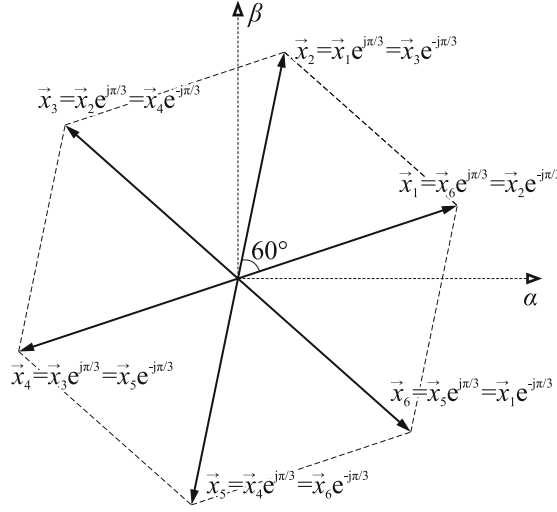


Fig. A.3: Six $\alpha\beta$ plane vectors with 60° displacement.

where k determines the direction and the number of 60° rotations applied, and m and n refer to the vectors' subscripts. For example, when \vec{x}_2 shown in Fig. A.3 is rotated -60° , (A.12) yields

$$\vec{x}_{2 \rightarrow 1} = \frac{2}{3}(x_a e^{j0} + x_b e^{j\frac{2\pi}{3}} + x_c e^{j\frac{4\pi}{3}})e^{-j\frac{\pi}{3}} \quad (\text{A.13a})$$

$$= \frac{2}{3}(x_a e^{-j\frac{\pi}{3}} + x_b e^{j\frac{\pi}{3}} + x_c e^{-j\pi}) \quad (\text{A.13b})$$

Based on Euler's formula, (A.13b) reduces to

$$\vec{x}_{2 \rightarrow 1} = \frac{2}{3}(x_a(\frac{1}{2} - j\frac{\sqrt{3}}{2}) + x_b(\frac{1}{2} + j\frac{\sqrt{3}}{2}) + x_c(-1 + j0)) \quad (\text{A.14a})$$

$$= -x_c + j\frac{1}{\sqrt{3}}(-x_a + x_b) \quad (\text{A.14b})$$

which implicates that the -60° rotation can be done by using the Clarke transformation as follows:

$$\vec{x}_{2 \rightarrow 1} = \frac{2}{3}((-x_c)e^{j0} + (-x_a)e^{j\frac{2\pi}{3}} + (-x_b)e^{j\frac{4\pi}{3}}) \quad (\text{A.15})$$

Yet another method to express the rotation $\vec{x}_{2 \rightarrow 1}$ is by rearranging of the $\alpha\beta$ vector components. If the zero-sequence component is neglected, \vec{x}_2 can be expressed as

$$\vec{x}_2 = x_\alpha + jx_\beta = x_a + j\frac{1}{\sqrt{3}}(x_b - x_c) \quad (\text{A.16})$$

Assuming that $x_a + x_b + x_c = 0$, one can solve x_a , x_b and x_c as follows

$$x_a = x_\alpha \quad (\text{A.17})$$

$$x_b = \frac{1}{2}(-x_\alpha + \sqrt{3}x_\beta) \quad (\text{A.18})$$

$$x_c = -\frac{1}{2}(x_\alpha + \sqrt{3}x_\beta) \quad (\text{A.19})$$

which can be substituted in (A.14b) to perform the rotation $\vec{x}_{2 \rightarrow 1}$. In a similar manner, \vec{x}_2 can be used to express the remaining four vectors. The transformations based on 60° symmetries are summarised in Table A.1.

Table A.1: Transformation of the $\alpha\beta$ coordinate vectors using the 60° symmetry.

$\ \vec{x}\ e^{j(\theta+\pi)}$	$= -x_a + j\frac{1}{\sqrt{3}}(-x_b - (-x_c))$	$= -x_\alpha - jx_\beta$
$\ \vec{x}\ e^{j(\theta+\frac{2\pi}{3})}$	$= x_c + j\frac{1}{\sqrt{3}}(x_a - x_b)$	$= (-\frac{1}{2}x_\alpha - \frac{\sqrt{3}}{2}x_\beta) + j(\frac{\sqrt{3}}{2}x_\alpha - \frac{1}{2}x_\beta)$
$\ \vec{x}\ e^{j(\theta+\frac{\pi}{3})}$	$= -x_b + j\frac{1}{\sqrt{3}}(-x_c - (-x_a))$	$= (\frac{1}{2}x_\alpha - \frac{\sqrt{3}}{2}x_\beta) + j(\frac{\sqrt{3}}{2}x_\alpha + \frac{1}{2}x_\beta)$
$\ \vec{x}\ e^{j\theta}$	$= x_a + j\frac{1}{\sqrt{3}}(x_b - x_c)$	$= x_\alpha + jx_\beta$
$\ \vec{x}\ e^{j(\theta-\frac{\pi}{3})}$	$= -x_c + j\frac{1}{\sqrt{3}}(-x_a - (-x_b))$	$= (\frac{1}{2}x_\alpha + \frac{\sqrt{3}}{2}x_\beta) + j(-\frac{\sqrt{3}}{2}x_\alpha + \frac{1}{2}x_\beta)$
$\ \vec{x}\ e^{j(\theta-\frac{2\pi}{3})}$	$= x_b + j\frac{1}{\sqrt{3}}(x_c - x_a)$	$= (\frac{1}{2}x_\alpha - \frac{\sqrt{3}}{2}x_\beta) + j(-\frac{\sqrt{3}}{2}x_\alpha - \frac{1}{2}x_\beta)$
$\ \vec{x}\ e^{j(\theta-\pi)}$	$= -x_a + j\frac{1}{\sqrt{3}}(-x_b - (-x_c))$	$= -x_\alpha - jx_\beta$

Hexagonal gh coordinates

Fig. A.4 shows the vectors \vec{x}_1 to \vec{x}_6 in the gh coordinates. The displacement between two adjacent vectors is 60° . Any of the six vectors can be used to express the other five by rearranging the vector components as summarised in Table A.2.

Table A.2: Rotation of gh coordinate system vectors using the 60° symmetries

$\ \vec{x}\ \angle(\theta + \pi)$	$(-x_g, -x_h)$
$\ \vec{x}\ \angle(\theta + \frac{2\pi}{3})$	$(-x_g - x_h, x_g)$
$\ \vec{x}\ \angle(\theta + \frac{\pi}{3})$	$(-x_h, x_g + x_h)$
$\ \vec{x}\ \angle(\theta + 0)$	(x_g, x_h)
$\ \vec{x}\ \angle(\theta - \frac{\pi}{3})$	$(x_g + x_h, -x_g)$
$\ \vec{x}\ \angle(\theta - \frac{2\pi}{3})$	$(x_h, -x_g - x_h)$
$\ \vec{x}\ \angle(\theta - \pi)$	$(-x_g, -x_h)$

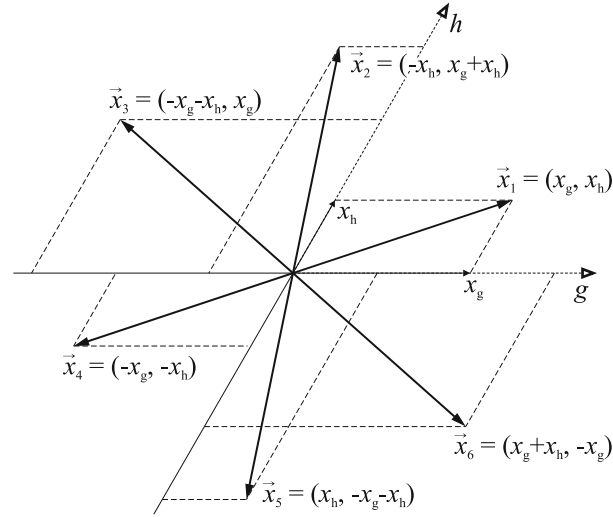


Fig. A.4: Six vectors in the gh coordinates with 60° displacement between two adjacent vectors.

Appendix B

Switching state transformations

Fig. B.1 depicts the positive-sequence three-phase source voltages u_{sa} , u_{sb} , and u_{sc} . The phase voltages have quarter-wave symmetry, and the displacement between the phases is $2\pi/3$. Because of the symmetries, the instantaneous phase voltages after each $\pi/3$ period can be expressed as summarised in Table B.1.

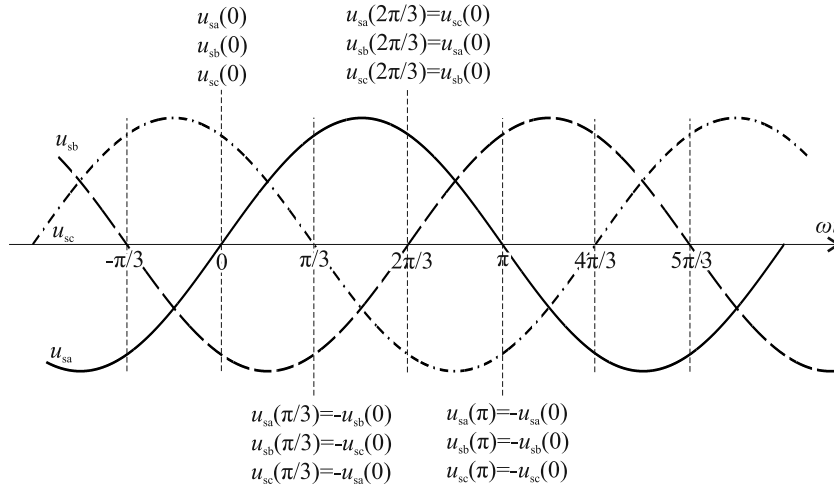


Fig. B.1: Symmetrical and balanced three-phase source voltages.

Table B.1: 60° symmetry between the three-phase source voltages

ωt	ωt_0	$\omega t_0 + \frac{\pi}{3}$	$\omega t_0 + \frac{2\pi}{3}$	$\omega t_0 + \pi$	$\omega t_0 + \frac{4\pi}{3}$	$\omega t_0 + \frac{5\pi}{3}$
$u_{sa}(\omega t)$	$u_{sa}(\omega t_0)$	$-u_{sb}(\omega t_0)$	$u_{sc}(\omega t_0)$	$-u_{sa}(\omega t_0)$	$u_{sb}(\omega t_0)$	$-u_{sc}(\omega t_0)$
$u_{sb}(\omega t)$	$u_{sb}(\omega t_0)$	$-u_{sc}(\omega t_0)$	$u_{sa}(\omega t_0)$	$-u_{sb}(\omega t_0)$	$u_{sc}(\omega t_0)$	$-u_{sa}(\omega t_0)$
$u_{sc}(\omega t)$	$u_{sc}(\omega t_0)$	$-u_{sa}(\omega t_0)$	$u_{sb}(\omega t_0)$	$-u_{sc}(\omega t_0)$	$u_{sa}(\omega t_0)$	$-u_{sb}(\omega t_0)$

The symmetries presented in Table B.1 also apply to the output voltages of three-phase converters. Fig. B.2 shows the 27 switch combinations of the three-level converter in three-dimensional coordinates. By using the principle of Table B.1, one switch combination can be used to express five other, as shown in Table B.2.

When the capacitor voltages are balanced, the six switch combinations obtained using Table B.2 generate six $\alpha\beta$ reference frame voltage vectors of equal lengths and with $\pi/3$ spacing. The voltage hexagon of the three-level converter is depicted in Fig. B.3. Table B.3 summarises how the vectors of Sector 1 can be transformed into Sector 2 to Sector 6 using the principle of Table B.2.

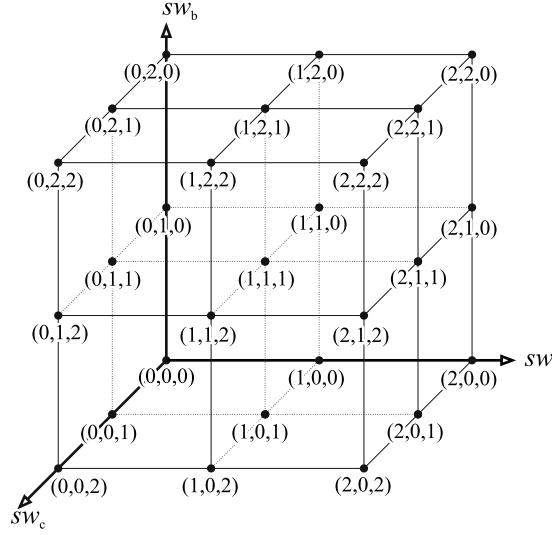


Fig. B.2: Switch combinations of the three-level converter in abc coordinates.

Table B.2: 60° symmetry between the switch combinations

$\ \vec{u}\ e^{j\theta}$	$\ \vec{u}\ e^{j(\theta+\frac{\pi}{3})}$	$\ \vec{u}\ e^{j(\theta+\frac{2\pi}{3})}$	$\ \vec{u}\ e^{j(\theta+\pi)}$	$\ \vec{u}\ e^{j(\theta+\frac{4\pi}{3})}$	$\ \vec{u}\ e^{j(\theta+\frac{5\pi}{3})}$
sw_a	$2 - sw_b$	sw_c	$2 - sw_a$	sw_b	$2 - sw_c$
sw_b	$2 - sw_c$	sw_a	$2 - sw_b$	sw_c	$2 - sw_a$
sw_c	$2 - sw_a$	sw_b	$2 - sw_c$	sw_a	$2 - sw_b$

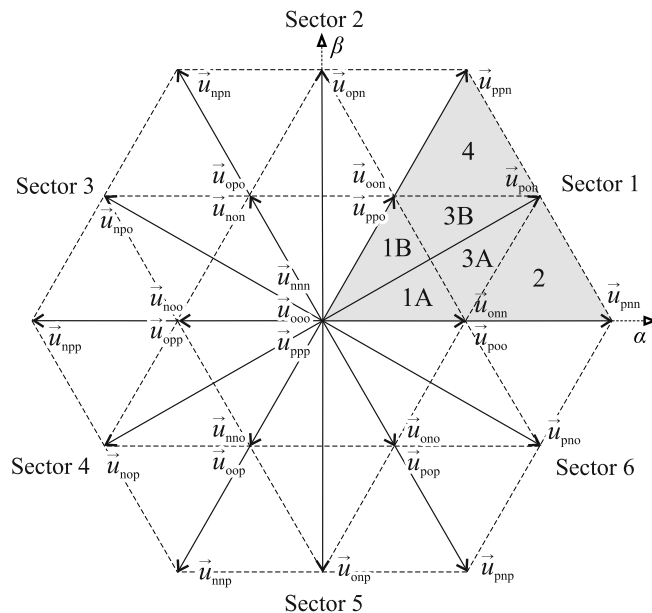


Fig. B.3: Voltage hexagon of the three-level converter.

Table B.3: Transformation of Sector 1 switch combinations and voltage vectors into Sector 2 to Sector 6

Sector 1	Sector 2	Sector 3	Sector 4	Sector 5	Sector 6
\vec{u}_{ppp}	\vec{u}_{nnn}	\vec{u}_{ppp}	\vec{u}_{nnn}	\vec{u}_{ppp}	\vec{u}_{nnn}
\vec{u}_{nnn}	\vec{u}_{ppp}	\vec{u}_{nnn}	\vec{u}_{ppp}	\vec{u}_{nnn}	\vec{u}_{ppp}
\vec{u}_{ooo}	\vec{u}_{ooo}	\vec{u}_{ooo}	\vec{u}_{ooo}	\vec{u}_{ooo}	\vec{u}_{ooo}
\vec{u}_{poo}	\vec{u}_{oon}	\vec{u}_{opo}	\vec{u}_{noo}	\vec{u}_{oop}	\vec{u}_{ono}
\vec{u}_{onn}	\vec{u}_{ppo}	\vec{u}_{non}	\vec{u}_{opp}	\vec{u}_{nno}	\vec{u}_{pop}
\vec{u}_{ppo}	\vec{u}_{non}	\vec{u}_{opp}	\vec{u}_{nno}	\vec{u}_{pop}	\vec{u}_{onn}
\vec{u}_{oon}	\vec{u}_{opo}	\vec{u}_{noo}	\vec{u}_{oop}	\vec{u}_{ono}	\vec{u}_{poo}
\vec{u}_{pon}	\vec{u}_{opn}	\vec{u}_{npo}	\vec{u}_{nop}	\vec{u}_{onp}	\vec{u}_{pno}
\vec{u}_{pnn}	\vec{u}_{ppn}	\vec{u}_{npn}	\vec{u}_{npp}	\vec{u}_{nnp}	\vec{u}_{pnp}
\vec{u}_{ppn}	\vec{u}_{npn}	\vec{u}_{npp}	\vec{u}_{nnp}	\vec{u}_{pnp}	\vec{u}_{pnn}

Appendix C

Inductor modelling and LCL filter frequency responses

In this thesis, the frequency-dependent impedances of the prototype filter inductors are approximated with Foster equivalent circuits [195]. At a given frequency, the impedance of k^{th} order Foster equivalent circuit can be expressed as

$$Z(\omega) = R_0 + \sum_{x=1}^k \frac{j\omega L_x R_x}{R_x + j\omega L_x} \quad (\text{C.1})$$

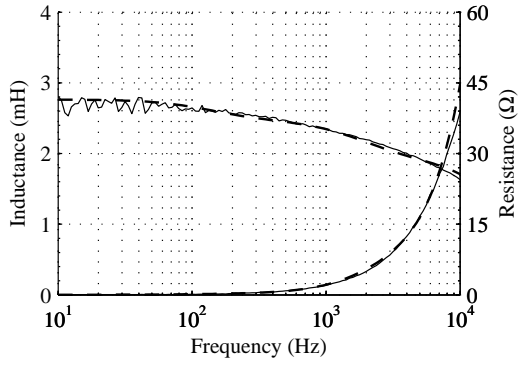
where R_0 is the DC resistance and the sum term is the impedance of k parallel RL elements connected in series. The equivalent circuit does not consider the effects of material nonlinearity, temperature coefficients, and saturation.

In this thesis, the third-order Foster models are studied. They were developed by firstly measuring the impedance responses of the prototype filter inductors using Venable Instruments' frequency response analyser Model 3120 with an impedance measurement kit. The measurements were conducted at room temperature. Finally, the parameters of the Foster equivalent circuits, summarised in Table C.1, were determined using a curve-fitting algorithm implemented in Matlab.

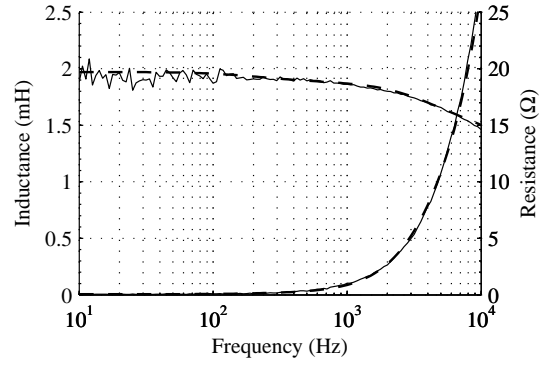
Figs. C.1-C.2 illustrate the measured and the approximated impedance responses, and the fitting errors. It can be seen that good accuracy was achieved up to 10 kHz. It is worth noting that the measured inductance of the 0.26 mH rated inductor is only ca. 0.19 mH around 50 Hz.

Table C.1: Foster equivalent circuit parameters of inductors $L_i, i \in 1, 2, 3$

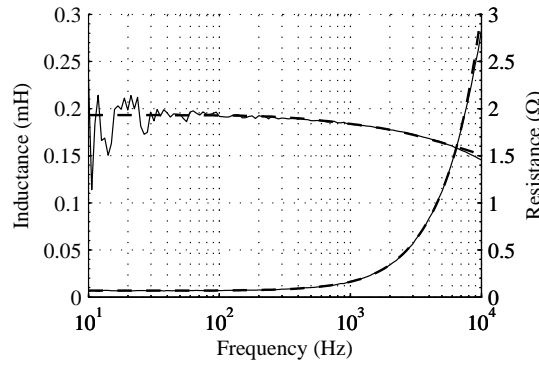
Parameter	$L_1 = 2.8 \text{ mH}$	$L_2 = 2.0 \text{ mH}$	$L_3 = 0.26 \text{ mH}$
L_{i1}	0.30 mH	86.6 μH	9.8 μH
L_{i2}	0.56 mH	389 μH	25.7 μH
L_{i3}	1.90 mH	1.50 mH	157.5 μH
R_{i0}	0.033 Ω	0.055 Ω	0.0685 Ω
R_{i1}	0.264 Ω	0.12 Ω	0.0368 Ω
R_{i2}	6.70 Ω	10.8 Ω	0.5869 Ω
R_{i3}	335.5 Ω	478.2 Ω	38.1 Ω



(a)



(b)



(c)

Fig. C.1: Measured (solid line) and approximated (dashed line) resistance and inductance of the filter inductors. (a) 2.8 mH inductor, (b) 2.0 mH inductor, and (c) 0.26 mH inductor.

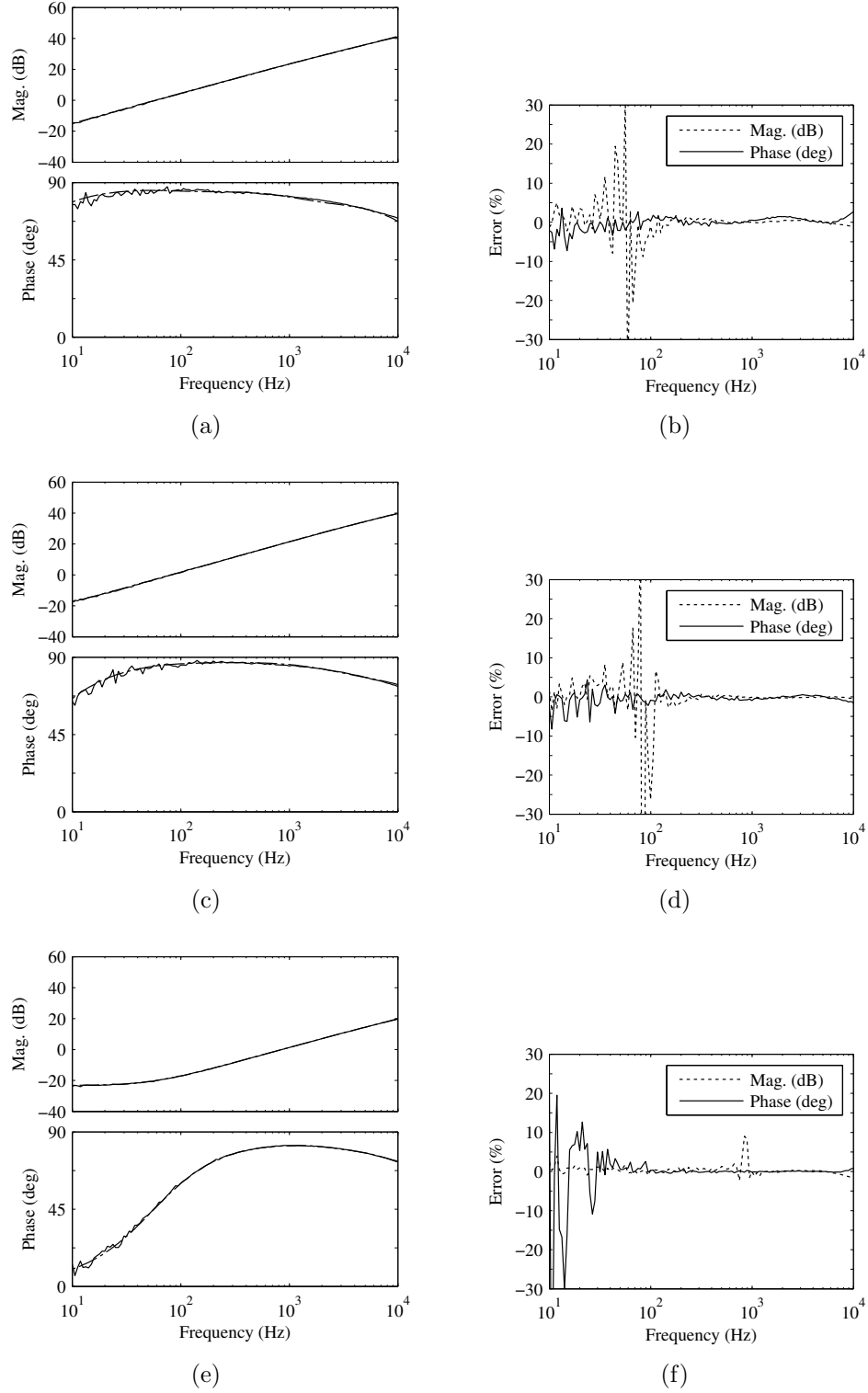


Fig. C.2: Measured (solid line) and approximated (dashed line) filter inductor impedances and the percentage error of magnitude (dotted line) and phase (solid line). (a)-(b) 2.8 mH inductor, (c)-(d) 2.0 mH inductor, and (e)-(f) 0.26 mH inductor.

The frequency responses $I_1(s)/U_1(s)$, $I_2(s)/U_1(s)$, and $I_2(s)/I_1(s)$ of the studied *LCL* filter can be expressed as follows

$$\frac{I_1(s)}{U_1(s)} = \frac{Z_2(s) + Z_3(s)}{Z_1(s)Z_2(s) + Z_2(s)Z_3(s) + Z_1(s)Z_3(s)} \quad (\text{C.2})$$

$$\frac{I_2(s)}{U_1(s)} = \frac{Z_3(s)}{Z_1(s)Z_2(s) + Z_2(s)Z_3(s) + Z_1(s)Z_3(s)} \quad (\text{C.3})$$

$$\frac{I_2(s)}{I_1(s)} = \frac{I_2(s)}{U_1(s)} \frac{U_1(s)}{I_1(s)} = \frac{Z_3(s)}{Z_2(s) + Z_3(s)} \quad (\text{C.4})$$

where

$$Z_1(s) = sL_1 + R_1 \quad (\text{C.5})$$

$$Z_2(s) = sL_2 + R_2 \quad (\text{C.6})$$

$$Z_3(s) = \frac{(sL_3 + R_3)R_d}{sL_3 + R_3 + R_d} + \frac{1}{sC_3} + R_C \quad (\text{C.7})$$

With nominal filter component values ($L_1 = 2.8$ mH, $L_2 = 2.0$ mH, $L_3 = 0.26$ mH, $C_3 = 30$ μ F, $R_d = 10$ Ω , and $R_C = 0.39$ Ω) the resonance and the antiresonance of $I_2(s)/I_1(s)$ occur at

$$f_p = \frac{1}{2\pi\sqrt{(L_2 + L_3)C_3}} \approx 610 \text{ Hz} \quad (\text{C.8})$$

$$f_z = \frac{1}{2\pi\sqrt{L_3C_3}} \approx 1800 \text{ Hz} \quad (\text{C.9})$$

Fig. C.3 shows the measured filter frequency responses, the ideal predicted responses, and the approximated responses based on the Foster equivalent circuits. The approximated responses match with the measured ones with a good accuracy.

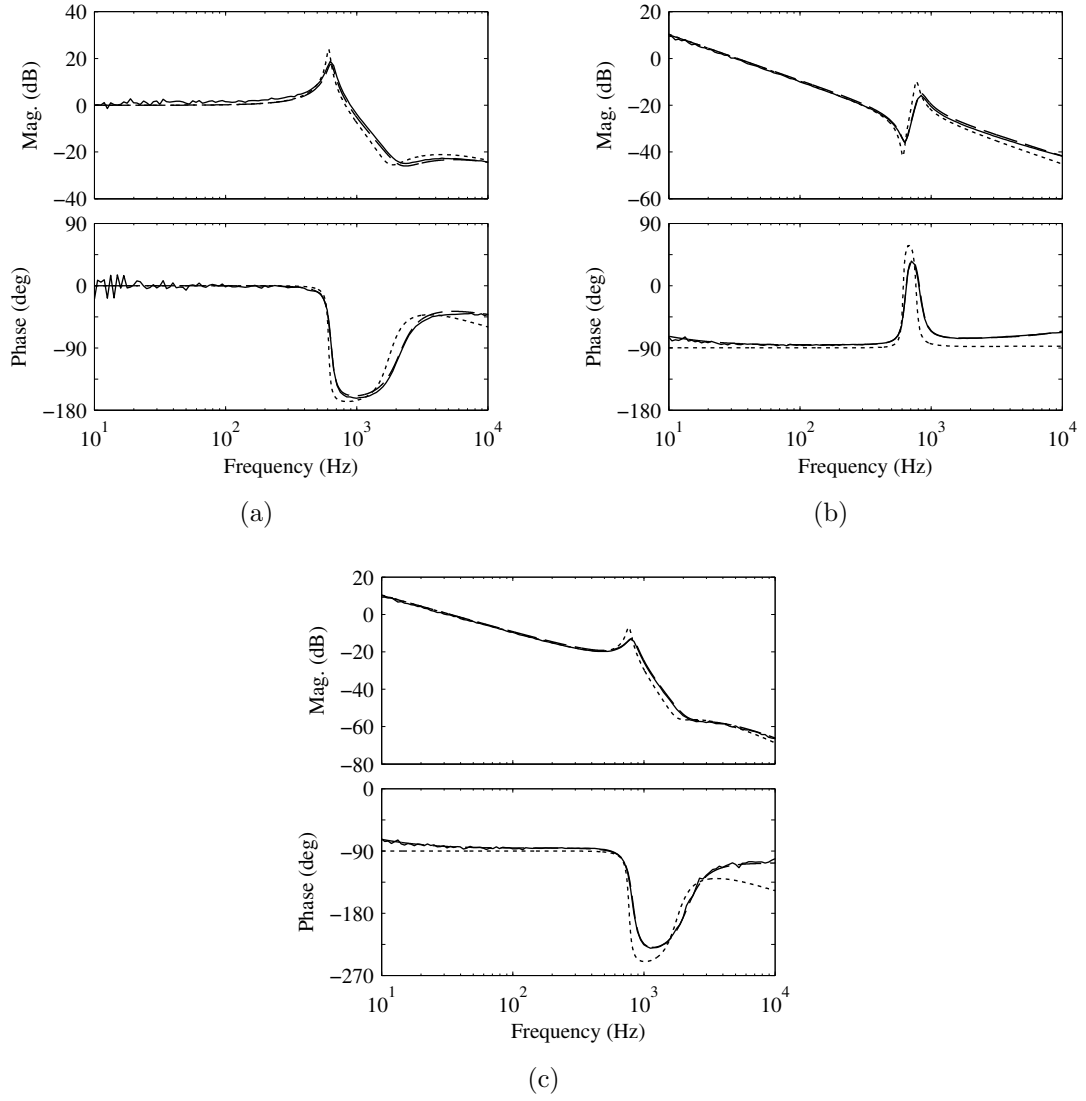


Fig. C.3: *LCL* filter frequency responses. Measured (solid line), ideal predicted (dotted line), approximation based on the Foster models (dashed line). (a) $I_2(s)/I_1(s)$, (b) $I_1(s)/V_1(s)$, (c) $I_2(s)/V_1(s)$.

Appendix D

Simulink model

Fig. D.1 shows the simulation model of the STATCOM. The electrical circuit model is implemented using the components provided in the SimPowerSystems component library. The control system is implemented using the components provided in the Simulink component library. The space-vector modulation algorithm is implemented as a script file, which is executed once per a control computation interval $T_s = \frac{1}{f_s} = \frac{1}{3600}$ s. In Fig. D.1, the filter inductors are modelled with Foster equivalent circuits and the grid is ideal.

The DSOGIFLL was implemented in Simulink by discretising the continuous-time algorithm, presented in Fig. 2.13 of Chapter 2, by using the Tustin's approximation $s \approx \frac{2}{T_s} \frac{z-1}{z+1}$. The parameters of the DSOGIFLL were selected as follows: $K = 1.1$, $K_i = \sqrt{2}$.

The DC bus voltage is controlled using a standard form PI controller. The discrete-time controller was developed by using the Backward Euler method, yielding $G_{PI}(z) = \frac{K_p(1-z^{-1}+K_iT_s)}{1-z^{-1}}$. The controller parameters were selected as follows: $K_p = 0.05$, $K_i = 16.5$, $T_s = \frac{1}{f_s} = \frac{1}{3600}$ s.

The current controllers were parametrised as follows. The PI current controllers: $K_p = 3.25$, $K_i = 40$. The predictive vector current controllers: $K_{i1} = 0.3$, $K_{i3} = K_{u3} = 1$, and $K_{i2} = 0.2$, $K_i = 40$. The Smith predictor: $K_{sp} = 0.39$. The observer gain matrix:

$$\mathbf{L} = \begin{bmatrix} 0.0556 & -0.5776 & 0.0325 & -1.3189 & 0.6078 & 6.4739 \\ -0.5776 & -0.0556 & -1.3189 & -0.0325 & 6.4739 & -0.6078 \end{bmatrix}^T$$

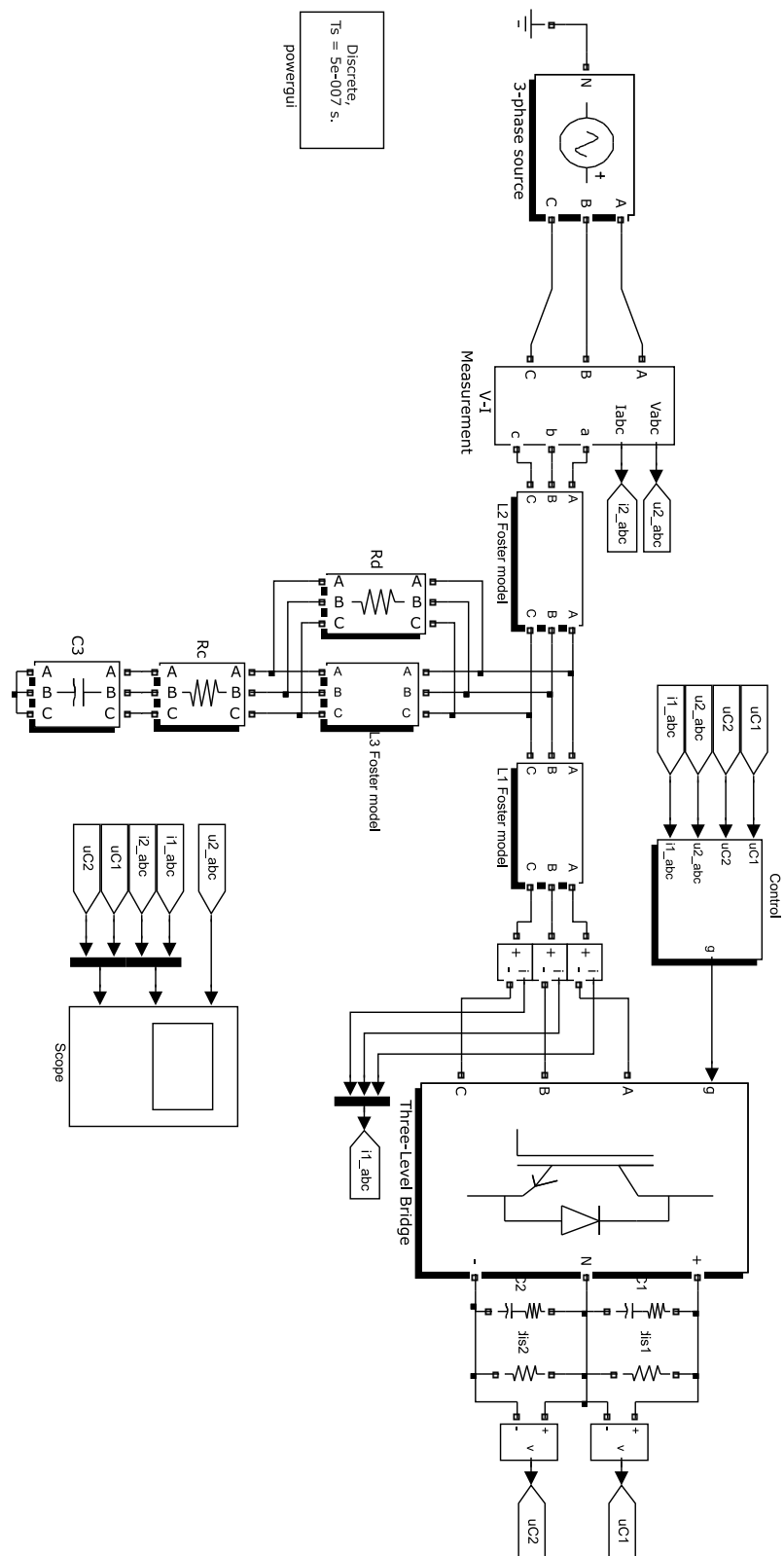


Fig. D.1: The STATCOM simulation model implemented using Simulink and SimPowerSystems.

Appendix E

Hardware-in-the-loop simulator

Fig. E.1 presents the hardware-in-the-loop (HIL) simulator used for real-time prototyping and testing of the STATCOM control [187, 189]. It consists of two rack-assembled hardwares, RTDS and dSPACE. The RTDS (Real-Time Digital Simulator) is a digital multiprocessor power system simulator for analytical network simulations and for testing of relays and control systems. In this thesis, the RTDS was used to solve the AC network model and the main circuit model of the three-level STATCOM. The RTDS simulation was controlled from a PC by using the RSCAD Software Suite. It provides the tools for modelling, monitoring and controlling the simulations, as well as for data recording and analysis. The STATCOM control was implemented in dSPACE by using Simulink and embedded C code. The two hardwares were interconnected as described in Fig. E.1.

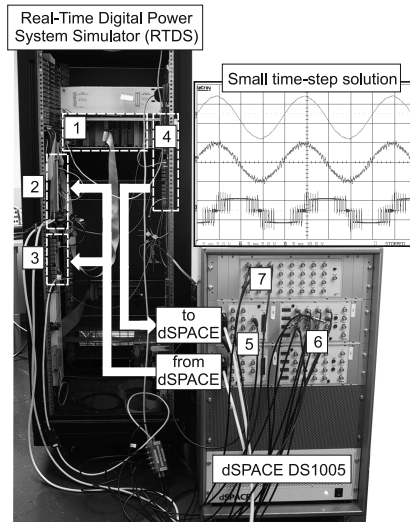


Fig. E.1: Hardware-in-the-loop simulation setup. 1: Processor cards, 2: Digital inputs, 3: Analogue inputs, 4: Analogue outputs, 5: Programmable timing outputs, 6: Analogue inputs, 7: Analogue outputs.

The RTDS rack shown in Fig. E.1 includes two types of processor cards and several I/O cards. The network model is solved with $50 \mu\text{s}$ time-step on six Triple Processor

Cards, each of which comprises three 80 MHz ADSP-21062 floating point DSPs. The time-critical STATCOM model is designated to a Giga processor card (GPC), which includes two 1 GHz IBM PPC750GX processors. The small time-step solution is accessed through Giga transceiver I/O (GTIO) cards. The latency time of the small-time-step simulation is only some microseconds.

The core of the dSPACE DS1005 hardware is a 1 GHz IBM 750GX PowerPC processor, which runs the compiled Simulink models in real-time, and operates as an interface between the I/O boards and the host PC. The I/O's include two DS4002 Timing and DI/O boards providing 16 programmable timing outputs in total, two 16-channel DS2004 AD boards with 16-bit resolution, and a 32-channel DS2103 DA board with 14-bit resolution.

The HIL simulator was used as an intermediate test platform between the Simulink simulations and the 10 kVA laboratory prototype. The space-vector modulation algorithm and the DSOIFLL were tested in dSPACE before implementing them in the laboratory prototype. Fig. E.2 shows the grid current, STATCOM current, and u_{ao} voltage waveforms in the HIL simulation [187]. The waveforms were obtained by measuring the output signals of the RTDS's analogue I/O's by using an oscilloscope. The HIL simulator was also studied in [189].

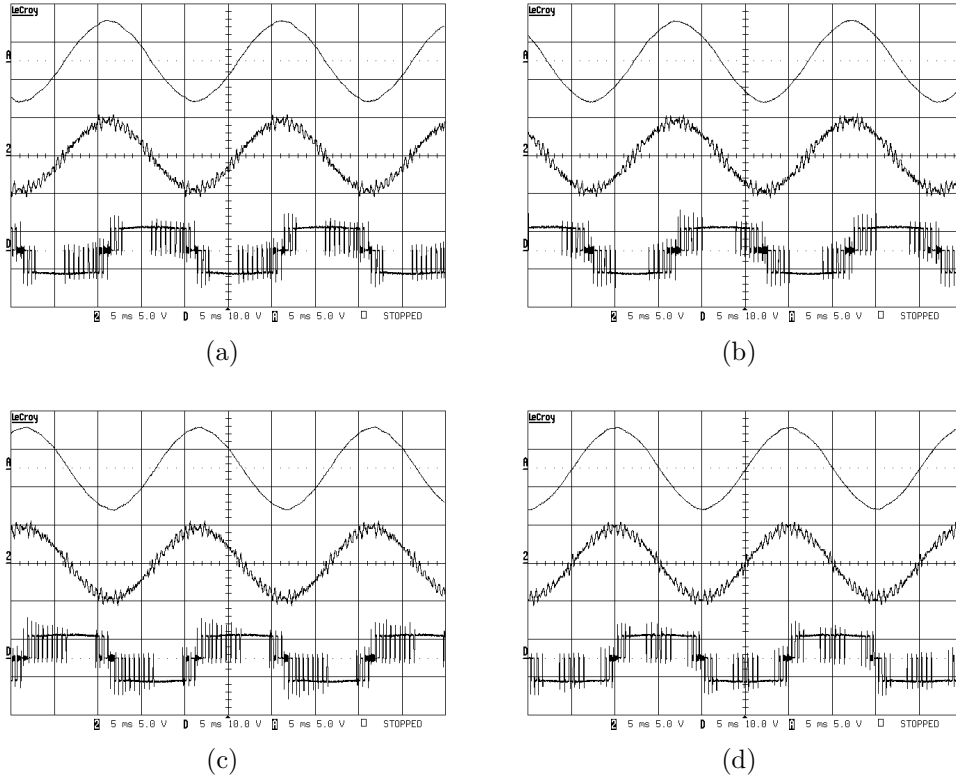


Fig. E.2: Grid current, STATCOM current, and u_{ao} voltage waveforms obtained with discontinuous PWM patterns; (a) DPWM0, (b) DPWM1, (c) DPWM2, (d) DPWM3. The control sampling frequency is 3600 Hz. The voltage and the current scales in the oscilloscope screenshots are 14 kV/div and 900 A/div.

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