A Novel Hybrid Single-Phase Modular Multilevel Inverter Topology with Enhanced Number of Levels Per Number of Devices

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***Abstract*—Inverters are important in the electrical industry, and there have been several advancements in this area. One of these is the multilevel inverter. A new single-phase inverter with seventeen levels is suggested in this study. To spread the load, the DC inputs will be paired in series/parallel. To generate a wider number of output level voltages, a combination of switching devices and DC sources will be utilized. The harmonic components will be lowered by employing the new modulation approach. THD rate analysis for eleven level and seventeen level structure is performed, and THD quality enhancement can be shown herein. The simulation of suggested multilevel converter is performed in Matlab/Simulink.**

Keywords—Multilevel inverter,17-level inverter, Single-phase, Seventeen-level, Hybrid modulation, APOD-PWM, POD-PWM

I. Introduction

Due to appealing features such as enhanced power quality, electromagnetic aspects, and lower power loss, multi-level inverters (MLIs) have been broadly employed, especially in green sources of energy, motor drive purposes, UPS technologies, inductive heating platforms, microgrids, and high voltage DC structures [1,2], [10-14].

Cascaded H-bridge (CHB) with independent DC supplies, Neutral Point Clamped, and Flying Capacitors were the three designs used in commercial MLIs. Because of its excellent reliability, scalable functioning, and high-voltage and power uses (for instance, 13.8 kV, 30 MVA) [3], the CHB is the most frequent industrial design of the three. MLI configurations have many advantages over traditional setups, including limited electromagnetic interference (EMI), decreased voltage stress on the switching devices, low voltage ratings, lesser THD, voltage boosting capability in single-stage operation, and improved grid-integrated power system quality with fewer passive filter components [9].

Numerous hybrid multilevel converters have been documented in literature. They are broadly classified into four types: series connections of three-phase full bridge converters (two or three levels) and single-phase H-bridge converters [4], hybrid cascaded single-phase H-bridge converters [5], hybrid topology [6], and other hybrid converters [7,8]. The amplitudes of the DC voltage sources in hybrid designs are unequal or fluctuate continuously [9]. Because fewer semiconductors and capacitors are employed in this topology, the size and cost of the converter are reduced, and the reliability is improved. Various topologies that can create both poles of the output voltage without the need of a polarity switching circuits have been presented. The packed U cell (PUC) MLI is one of MLI that has been described in [15]. The PUC, on the other hand, need a wide range of DC sources since voltage levels are mostly formed by subtracting two or more sources.

In this study, a novel single-phase seventeen level inverter containing a few switching devices and DC voltage supplies which has load sharing capability by conducting parallel operations of DC voltages and minimizing harmonic content using hybrid modulator is proposed. The key benefits of this topology are as follows:

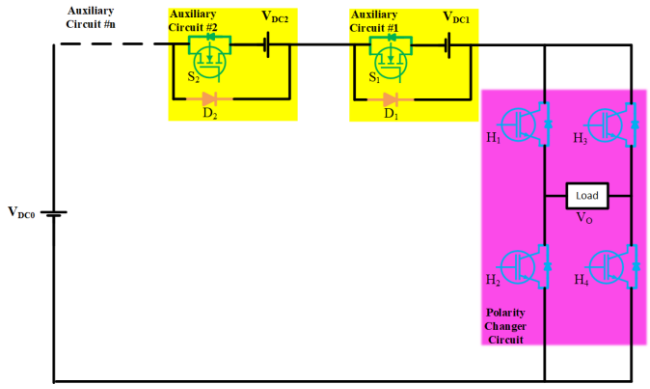
- Modularity configuration: This feature can help designer to increase or decrease output level easily. Besides that, the damaged or failed module can be replaced with a new cell.
- Using a combination of low and high switching frequency devices.
- Low THD voltage due to seventeen-level output voltage.
- The possibility of using the same or different input DC voltage sources.

II. Design Of The Suggested Modular Multilevel Inverter

A. Circuit Configuration

Figure 1(a) depicts a single-phase multilevel inverter which is presented in [9]. In this topology, each cell is made with an active switch and a single diode. By increasing the number of cells, the output voltage level can be increased. However, in this topology the power switches suffer from high current stresses. Therefore, it is necessary to use another modular structure that can increase the number of output levels and use switches with less current stress.

Figure 1(b) shows the recommended inverter power circuit, that is divided into three sections: the polarity changer circuit, main cells and the auxiliary circuit. The polarity changer circuit is made up of four power switching components that work together to produce a complete H-bridge inverter.



(a)

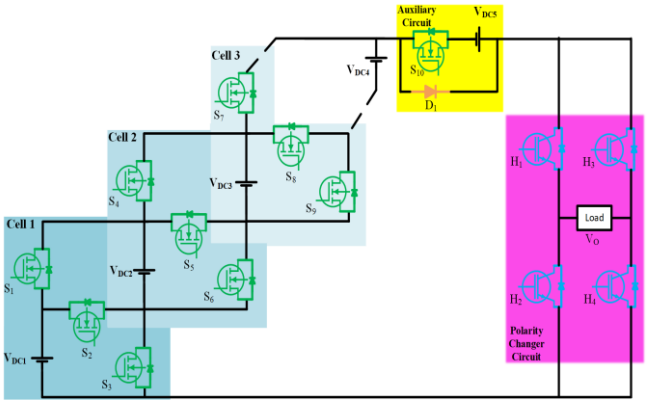


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Fig. 1. a) Circuit in [9], b) Suggested circuit of MLI

The bridge circuit adjusts the polarity of the produced load voltage in the positive half cycle by switching ON (H1, H4) or in the negative half-cycle by switching ON (H2, H3). The zero state load voltage can be achieved whether by switching ON (H_1, H_3) or (H_2, H_4). To prevent voltage supply short circuiting, switches (S_1, S_2) and (S_2, S_3) should operate in complimentary condition.

B. Operation Concepts

Table I shows the switching states, where 1 or 0 indicates whether the switch is switched on or off. As can be found from this table, the status of switches (H_1-H_4) changes once every 50 Hz (output frequency), so we can use switching devices that do not require a high switching frequency capability, such as IGBTs. Figure 2 shows two examples of operation modes. As can be found from this figure, the current stress of switches $S_{4,6}$, $S_{7,9}$ are equal and equal to half of switch S_2.

The voltage of DC source in auxiliary circuit can be equal to or different from the DC sources in the main cells. In the first state, DC sources are equal and in the second state DC voltages are not equal.

1) State 1

In this state, the amplitude of DC source in both main cells and auxiliary circuit are equal.

$$VDC\ AUX = VDC \tag{1}$$

The number of levels produced at the output by main cells are as

$$N = 2(m+1) \tag{2}$$

So the number of levels created by these cells will be,

$$N = 2(3+1) = 8 \tag{3}$$

where, m is number of main cells.

1) State 2

To increase the number of levels, the amplitude of VDC AUX will be lowered to half the amount of VDC. In the main cells, the DC source value will remain the same as before. The number of levels produced at the output in this state is

$$N = 4(m+1) + 1 \tag{4}$$

So by using 3 main cells , the number of levels created will be,

$$N = 4(3+1) + 1 = 17 \tag{5}$$

Furthermore, the total number of high switching devices in this inverter is:

$$N = 3(\mu+2) - 5 = 10 \tag{6}$$

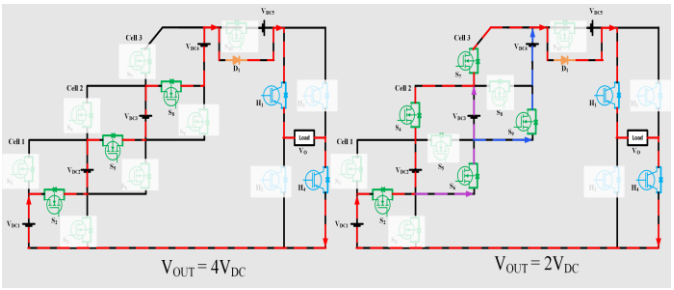
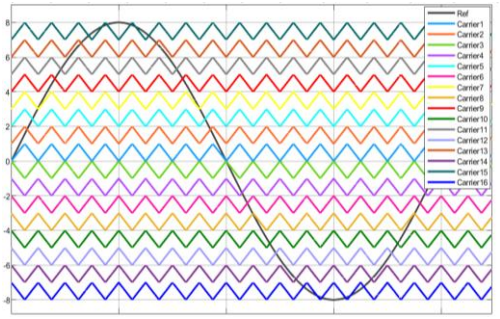


Fig. 2. Two examples of operation modes.

C. PWM Techniques

There are some different PWM techniques proposed for multilevel inverters in the past. Among these methods, Level-shifted and Phase-shifted PWM techniques are most popular ones [1]. Phase Opposition Disposition PWM (POD-PWM) and Alternate Phase Opposed Disposition of PWM (APOD-PWM) has the best performance in terms of THD value. Figure 3 show three PWM techniques based on phase-shifted PWM which is applied on the suggested MLI.



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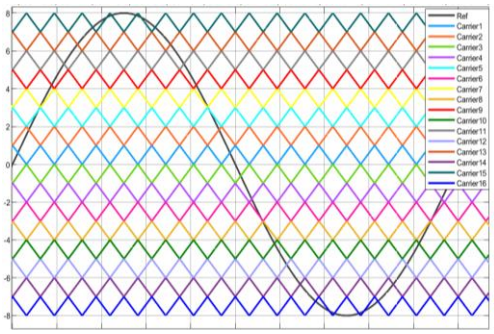

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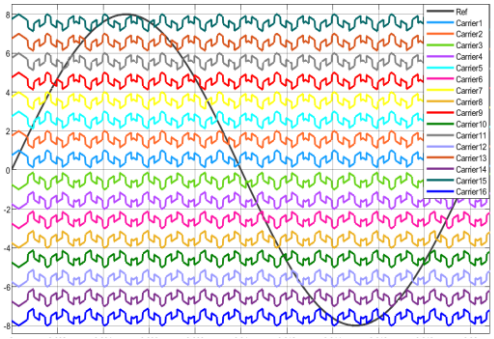


(c)

Fig. 3. PWM techniques: a) POD-PWM, c) APOD-PWM, b) new Hybrid PWM for suggested MLI.

III. Simulation Results

Matlab/Simulink is used to model and evaluate the operation of suggested inverter and three PWM techniques. In this section we considered the following parameters for simulation:

- Voltage of DC Input Sources are 70V, 35V for the first test ($V_{DC1\text{-}4}$ = 70V, V_{DC5} = 35V) and the voltage of input sources is equal for the second test ($V_{DC1\text{-}5}$ =63V).
- Carrier Frequency is 20kHz.
- Output Frequency is 50Hz and RMS of output voltage is 220V.
- The modulation index ($M = \frac{A_{modulation}}{(n-1)A_{carrier}}$) is 0.95 in all simulations (n : number of output level).

Figure 4 shows the 11-level output voltage of suggested single-phase MLI. In this state the DC voltage source of auxiliary circuit is equal to other DC voltage sources in main cells. The FFT analysis of output voltage is depicted in Figures 5(a-c). Figures 5(a,b) show the harmonic components including switching frequency, its multiples and other components when output voltage is 11-level and the modulators are POD-PWM and APOD, respectively. Figure 5(c) shows the harmonic components of output voltage when suggested PWM is applied.

TABLE I. SWITCHING STATES OF THE SUGGESTED HYBRID SEVENTEEN-LEVEL INVERTER

Levels	**S_1, S_3**	**S_2**	**S_4, S_6**	**S_5**	**S_7, S_9**	**S_8**	**S_{10}**	**H_1, $\bar{H}_2$**	**H_3, $\bar{H}_4$**
$4V_{dc1}$ $+V_{dc\,AUX}$	0	1	0	1	0	1	1	1	0
$4V_{dc1}$	0	1	0	1	0	1	0	1	0
$3V_{dc1}$ $+V_{dc\,AUX}$	0	1	0	1	1	0	1	1	0
$3V_{dc1}$	0	1	0	1	1	0	0	1	0
$2V_{dc1}$ $+V_{dc\,AUX}$	0	1	1	0	1	0	1	1	0
$2V_{dc1}$	0	1	1	0	1	0	0	1	0
V_{dc1} $+V_{dc\,AUX}$	1	0	1	0	1	0	1	1	0
V_{dc1}	1	0	1	0	1	0	0	1	0
0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1	1
$-V_{dc1}$	1	0	1	0	1	0	0	0	1
$-V_{dc1}$ $-V_{dc\,AUX}$	1	0	1	0	1	0	1	0	1
$-2V_{dc1}$	0	1	1	0	1	0	0	0	1
$-2V_{dc1}$ $-V_{dc\,AUX}$	0	1	1	0	1	0	1	0	1
$-3V_{dc1}$	0	1	0	1	1	0	0	0	1
$-3V_{dc1}$ $-V_{dc\,AUX}$	0	1	0	1	1	0	1	0	1
$-4V_{dc1}$	0	1	0	1	0	1	0	0	1
$-4V_{dc1}$ $-V_{dc\,AUX}$	0	1	0	1	0	1	1	0	1

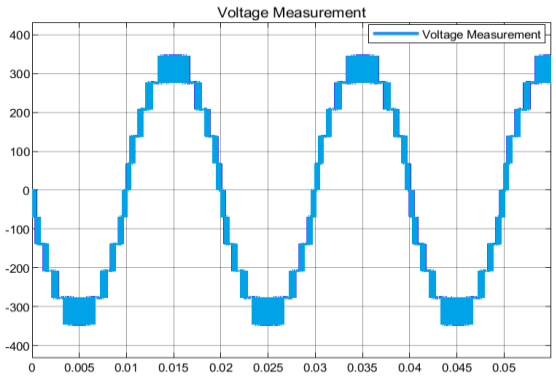
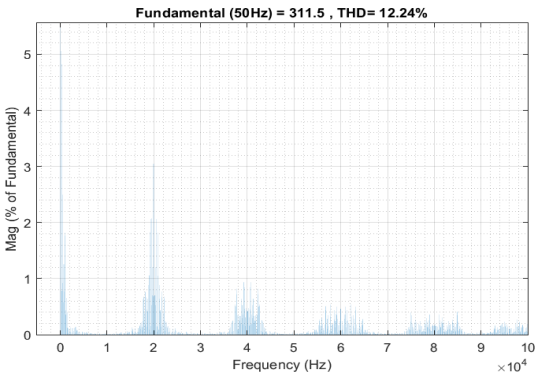


Fig. 4. Output voltage of suggested 11-level MLI when Vdc AUX = Vdc



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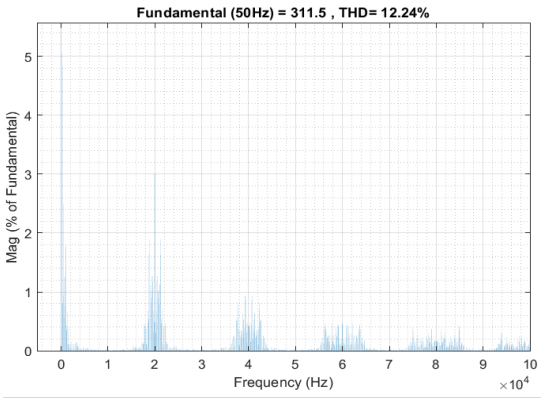

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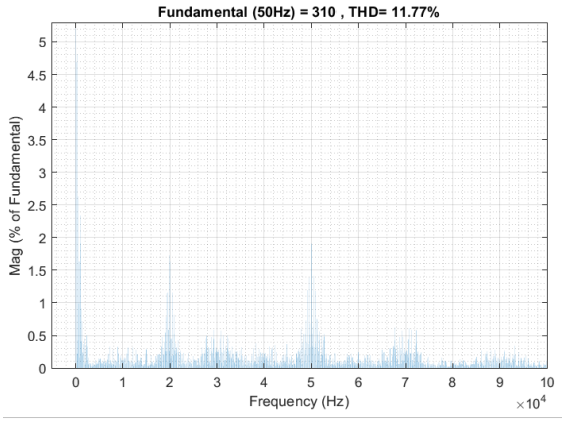


(c)

Fig. 5. FFT analysis of output voltage when Vdc AUX= Vdc using a) POD PWM, b) APOD-PWM, c) Suggested PWM.

Figure 6 shows the 17-level output voltage of suggested single-phase MLI. In this state the DC voltage source of auxiliary circuit is equal to half of other DC voltage sources in main cells. The FFT analysis of output voltage is depicted in Figures 7(a-c).

As it can be found from Fig. 5 and Fig. 7, the THD value in both POD and APOD PWM are the same when the output voltage is 11 level or 17 level. However, the distribution of harmonic components in all three PWMs are different from each other.

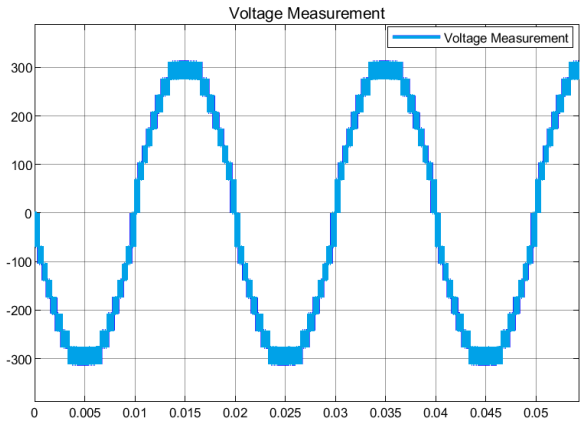
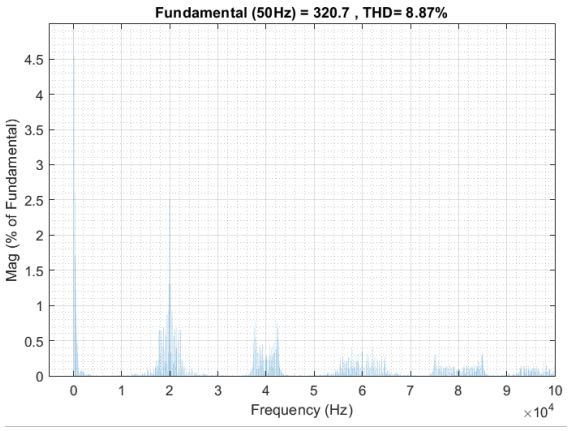
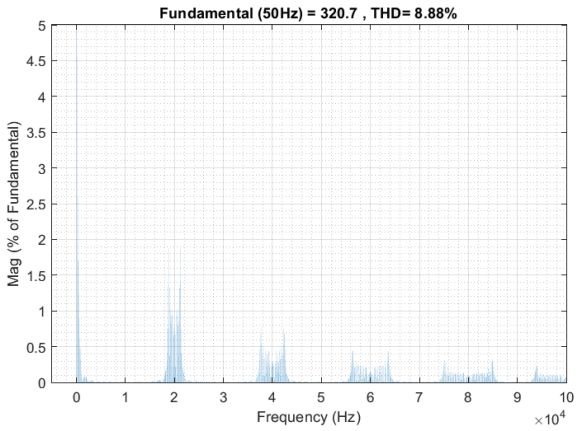


Fig. 6. Output voltage of suggested 17-level MLI when Vdc AUX= 0.5Vdc.



(a)



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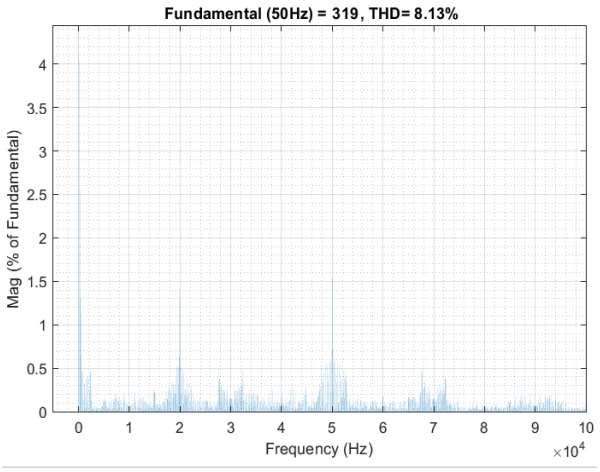

(c)

Fig. 7. FFT analysis of output voltage when Vdc AUX= 0.5Vdc using a) POD-PWM, b) APOD-PWM, c) Suggested PWM.

The THD values of output voltage for different PWM techniques are shown in Table II. By comparing the FFT results, it is obvious that when suggested PWM is applied on the suggested MLI, THD value of output voltage is better in 11-level or 17-level modes.

Furthermore, by using the suggested modulation, the frequency amplitude associated with switching is reduced and a more suitable distribution is made in the range of high-order frequencies. This distribution in harmonic content can be adjusted by the designer and helps reduce problems related to electromagnetic interference in the MLIs. This improvement can be achieved by reducing the system noise range below the standard limits (like CISPR standard) at the switching frequency that often has the maximum range.

TABLE II. COMPARISON OF THD VALUE FOR DIFFERENT PWMS IN SUGGESTED MLI.

	POD-PWM	**APOD-PWM**	**Suggested PWM**
THD 11-Level	12.24 %	12.24 %	11.77 %
THD 17-Level	8.87 %	8.88 %	8.13 %
MMASF 11-level	3.1 %	3.1 %	1.89 %
MMASF 17-level	2.51 %	1.93%	1.54 %

* MMASF: Maximum Magnitude around Switching Frequency (% of Fundamental)

Table III compares the suggested inverter's expanded topology to the expanded inverter designs in [16-18]. According to Table III, whenever the designs provide the same output voltage level, the suggested inverter has fewer parts than other MLIs.

TABLE III. COMPARISON WITH OTHER MLIS

	Suggested Inverter	**Inverter in [16]**	**Inverter in [17]**	**Inverter in [18]**
$\mathbf{N_L}$	$4N_S + 1$	$2N_c + 3$	$2N_c + 3$	$2N_c + 1$
$\mathbf{N_{SW}}$	$3(N_S+1) -1$	$3N_c + 4$	$2N_c + 4$	$3N_c + 5$
$\mathbf{N_D}$	1	0	N_c	$N_c - 2$
$\mathbf{N_C}$	0	N_C	N_C	N_C
$\mathbf{N_s}$	N_S	1	1	1

* NSW: Number of switches, ND: Number of diodes, NC: Number of capacitors, NS: Number of sources.

IV. CONCLUSION

This paper describes the performance of a single-phase seventeen-level inverter with two PWM control approaches. For multilevel output voltage, the suggested inverter reduces the number of circuit elements. The seventeen-level output voltage is generated with just ten high frequency and four low frequency switches and single diode. The suggested topology has a lower total standing voltage than the PUC or other popular MLIs while operating in state 2.

REFERENCES

[1] O. Zolfagharian, M. Farsijani, E. Keyvanloo and M. Tavakoli Bina, "A New Modulation Technique for Improving the Performance of Two-Phase Cascaded H-bridge Multilevel Inverter," 2022 13th Power Electronics, Drive Systems, and Technologies Conference (PEDSTC), 2022, pp. 202-206

[2] T. Roy and P. K. Sadhu, "A step-up multilevel inverter topology using novel switched capacitor converters with reduced components," IEEE Transactions on Industrial Electronics, 2020.

[3] Sandeep N, Yaragatti UR. Operation and control of an improved hybrid nine-level inverter. IEEE Trans Ind Appl. 2017;53:5676-5686.

[4] P. P. Rajeevan, K. Sivakumar, C. Patel, R. Ramchand, and K. Gopakumar, "A seven-level inverter topology for induction motor drive using twolevel inverters and floating capacitor fed h-bridges," IEEE Trans. Power Electron., vol. 26, no. 6, pp. 1733–1740, Jun. 2011.

[5] D. Sixing, J. Liu, J. Lin, and Y. He, "A novel DC voltage control method for STATCOM Based on hybrid multilevel H-bridge converter," IEEE Trans. Power Electron., vol. 28, no. 1, pp. 101–111, Jan. 2013.

[6] H. Akagi and K. Isozaki, "A hybrid active filter for a three-phase 12-pulse diode rectifier used as the front end of a medium-voltage motor drive," IEEE Trans. Power Electron., vol. 27, no. 1, pp. 69–77, Jan. 2012.

[7] J. Liu, J. Wu and J. Zeng, "Symmetric/Asymmetric Hybrid Multilevel Inverters Integrating Switched-Capacitor Techniques," in IEEE Journal of Emerging and Selected Topics in Power Electronics, vol. 6, no. 3, pp. 1616-1626, Sept. 2018.

[8] B. K. Sahana and K. C. Rupesh, "A Single-Phase Hybrid Seventeen Level Multilevel Inverter Topology," 2022 IEEE International Conference on Signal Processing, Informatics, Communication and Energy Systems (SPICES), 2022.

[9] Ali, Ahmed Ismail M., Mahmoud A. Sayed, Takaharu Takeshita, Alaaeldien MM Hassan, and Ahmed M. Azmy. "A single‐phase modular multilevel inverter based on controlled DC‐cells under two SPWM techniques for renewable energy applications." International Transactions on Electrical Energy Systems 31, no. 1 (2021): e12599.

[10] X. Wang, H. J. Kaleybar, M. Brenna and D. Zaninelli, "Power Quality Indicators of Electric Vehicles in Distribution Grid," 2022 20th International Conference on Harmonics & Quality of Power (ICHQP), Naples, Italy, 2022, pp. 1-6.

[11] S. Abbasian, M. Farsijani, M. Tavakoli bina and A. Shahirinia, "A non-isolated Common-Ground High Step-Up Soft Switching DC-DC Converter with Single Active Switch," in IEEE Transactions on Industrial Electronics, 2022.

[12] M. Brenna, H. J. Kaleybar, F. Foiadelli and D. Zaninelli, "Modern Power Quality Improvement Devices Applied to Electric Railway

Systems," 2022 20th International Conference on Harmonics & Quality of Power (ICHQP), Naples, Italy, 2022, pp. 1-6.

[13] M. Farsijani, S. Abbasian, H. Hafezi and A. Abrishamifar, "A High Step-Up Cost Effective DC to DC Topology Based on Three-Winding Coupled-Inductor," in IEEE Journal of Emerging and Selected Topics in Industrial Electronics, 2022.

[14] Kaleybar H. J., Brenna M., Foiadelli F., "Dual-loop generalized predictive control method for two-phase three-wire railway active power quality controller," Transactions of the Institute of Measurement and Control, 2021, vol. 43, no 1, pp. 88-101.

[15] Ounejjar, Y.; Al-Haddad, K. A new high power efficiency cascaded U cells multilevel converter. In Proceedings of the 2009 IEEE International Symposium on Industrial Electronics, Seoul, Korea, 5–8 July 2009; pp. 483–488.

[16] Hinago, Y., Koizumi, H.: 'A switched-capacitor inverter using series/parallel conversion with inductive load', IEEE Trans. Ind. Electron., 2012, 59, (2), pp. 878–887

[17] Babaei, E., Gowgani, S.S.: 'Hybrid multilevel inverter using switched capacitor units', IEEE Trans. Ind. Electron., 2014, 61, (9), pp. 4614–4621

[18] Khenar, M., Taghvaie, A., Adabi, J., & Rezanejad, M. (2018). Multi-level inverter with combined T-type and cross-connected modules. IET Power Electronics,vol. 11(no. 8), pp. 1407–1415.