A Double-Switch High Gain DC-DC Converter Based on Coupled-Inductors

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***Abstract*—An innovative high voltage gain dc to dc boost converter using extendable diode-capacitor voltage multiplier cells (VMC) is discussed and recommendations. Furthermore, the primary and supplemental power MOSFETs of the given converter use zero voltage switching (ZVS). In the described design, diode-capacitor VMC and Coupled inductors (CI) are used to obtain a greater voltage gain. The leakage inductances of the CIs limit the levels of current drop in the diodes of voltage multiplier, significantly lowering its reverse recovery loss. Furthermore, the voltage stress across all capacitors and components are greatly decreased. The offered converter's structure and theoretical analysis are described. Furthermore, the experimental results will validate the theoretical analysis.**

Keywords—high gain topology, DC to DC Converter, coupled-inductor, soft switching

I. INTRODUCTION

The growth and use of sustainable power, such as solar energy, wind energy, tidal energy, and so on, may effectively tackle the issues of environmental damage, temperature increase, and energy crises created by the over-exploitation of fossil fuel energy [1]. Even so, since the generation power of renewable sources varies and is variable due to climate and other climatic circumstances, renewable resources are usually integrated with energy storage technologies, like batteries and ultracapacitors, to provide continuous and secure power supply for consumers, micro-grids, or grid-connected converters [2].

High gain power topologies are necessary for implementations in which renewable energy and energy storage systems are merged into high voltage dc links due to the intrinsic low voltage of solar power energy sources and energy storage equipment (normally tens of volts) and the higher voltage delivered to the load or inverter (roughly 410V) [3-4]. To raise the output voltage value, a traditional boost topology must expand the duty cycle amount, which significantly increases the reverse recovery concern of the diode on the output port. Furthermore, it restricts the voltage gain and raises the normalizing voltage stress on devices, making typical boost converters unsuitable for large power ranges [5].

In overall, high voltage gain dc converters can be made by 1) employing CI techniques, 2) employing VMC strategies like diode/capacitor, diode/capacitor/inductor, diode/capacitor/coupled inductor, and 3) employing a mixture of interleaving methodologies with VMCs and CIs.

By modifying the CI turns ratio without exceeding the duty cycle, CI-based converters offer significant voltage gain while mitigating the reverse-recovery issue of rectifier diodes. Two single-switch high step-up dc–dc topologies similar single-MOSFET high step-up dc–dc topologies are developed in [6], [7], with combined usage of a CI and a VMC, that recycle the leakage inductance energies. But, [6], [7] face with excessive VMC inrush current in switching changes as well as significant output voltage ripples. The presented topology in [8] provides a suitably high voltage gain in a 3-phase interleaved converter. But, using two MOSFETs and one CI for every phase raises the price and volume of the topology. Furthermore, the stored energy of magnetizing inductor isn't recycled effectively.

In [9]-[10], several designs for achieving high voltage gain and ZVS capability are suggested. The power MOSFETs in [9] are soft-switched on and the diodes are turned off with zero currents, that solves typical reverse recovery concerns. The quantity of power MOSFETs and voltage stress along the voltage multiplier capacitors were noted to be excessive in [9]. Moreover, this was noted in [10] that not only the quantity of power MOSFETs is high, but the designing and execution of the CIs is complex. Such drawbacks raise the size, cost, and complexity of the designs.

The suggested converter is described in this study, and its operating modes are explored in section II. The steady state evaluation is described in Section III. In part IV, the suggested topology is compared to various comparable designs. In furthermore, to validate the theoretical background, a laboratory model of the suggested converter is built, and its outcomes are explored in part V. Lastly, in part VII, a brief summary of this work is provided.

II. PROPOSED TOPOLOGY AND OPERATION PRINCIPLES

A novel double switch common ground converter having high voltage gain is originally presented in order to get a high gain dc-dc converter for renewable energies, as illustrated in Fig 1. Two CI with two windings, two switches ($S_{1\text{-}2}$), four diodes ($D_{1\text{-}3}$, D_o), three capacitors $C_{1\text{-}3}$, and one output filter capacitor are used in the proposed converter. The CIs are represented by an idealized transformer (N_p and N_s), with a magnetizing inductance L_m and a leakage inductor L_k($N = \frac{N_S}{N_P}$, $n = \frac{n_S}{n_P}$). There are six operating modes for the suggested converter. Figures 2 and 3 show the main waveforms of the suggested converter and its comparable circuit in various operating modes. The following concepts are provided to ease the circuit analysis:

(1) All intrinsic capacitors of the MOSFETs S and diodes are ignored. The diodes' forward voltage loss is disregarded.

(2) All capacitors are big enough thus the voltages of all capacitors are assumed to be consistent throughout a single switching period.

(3) The CI's turn ratio is determined as $N = \frac{N_S}{N_P}$, $n = \frac{n_S}{n_P}$.

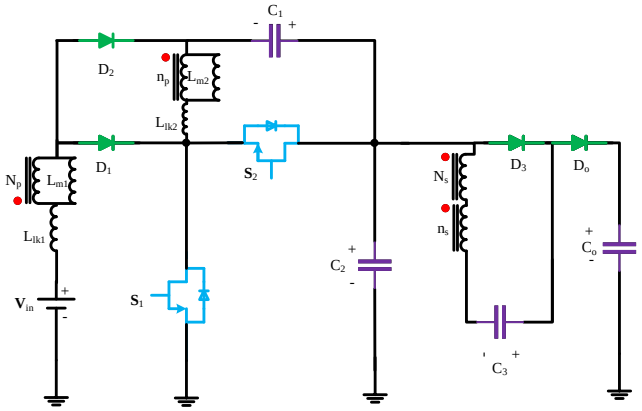


Fig. 1. Suggested step up DC to DC topology

A. *Mode 1:*

At t_0, both the primary MOSFET S_1 and the second MOSFET S_2 are turned off. But, in this condition, the current of (i_{LK1}) is positive, whereas the current through L_{LK2} is negative (i_{LK2}). In this mode the inherent diode of MOSFET S_1 is conducting.

B. *Mode 2:*

At the beginning of this mode power switch S_1 is turned on in ZVS condition and switch S_2 is off. Diodes D_2, D_3, and D_o are reversed biased and Diode D_1 is still conducting. The following equations can be obtained from figure 3(b):

$$V_{Lm1}^{D} = \left[\frac{L_{m1}}{L_{m1}+L_{k1}}\right] V_{in} = kV_{in} \quad (1)$$

$$V_{Lk1}^{D} = \left[\frac{L_{k1}}{L_{m1}+L_{k1}}\right] V_{in} = (1-k)V_{in} \quad (2)$$

$$V_{Lm2}^{D} = \left[\frac{L_{m2}}{L_{m2}+L_{k2}}\right] (V_{C2}-V_{C1}) = k(V_{C2}-V_{C1}) \quad (3)$$

$$V_{Lk2}^{D} = \left[\frac{L_{k2}}{L_{m2}+L_{k2}}\right] (V_{C2}-V_{C1}) = (1-k)(V_{C2}-V_{C1}) \quad (4)$$

C. *Mode 3:*

The only difference between this state and the previous mode is that diode D_3 turns on and capacitor C_3 is charged through it. By using the Kirchhoff's circuit law in the loops of figure 3(c) the following formulas can be obtained:

$$V_{NS}^{D} = NV_{Lm1}^{D} = NkV_{in} \quad (5)$$

$$V_{nS}^{D} = nV_{Lm2}^{D} = nk(V_{C2}-V_{C1}) \quad (6)$$

$$V_{C3} = V_{NS}^{D} + V_{nS}^{D} = k(NV_{in} + nV_{C2} - nV_{C1}) \quad (7)$$

D. *Mode 4:*

This state starts when MOSFET S_1 is turned off and Diode D_1 is reverse biased. During this short interval the energy of L_{lk1} is discharged through internal diode of MOSFET S_2.

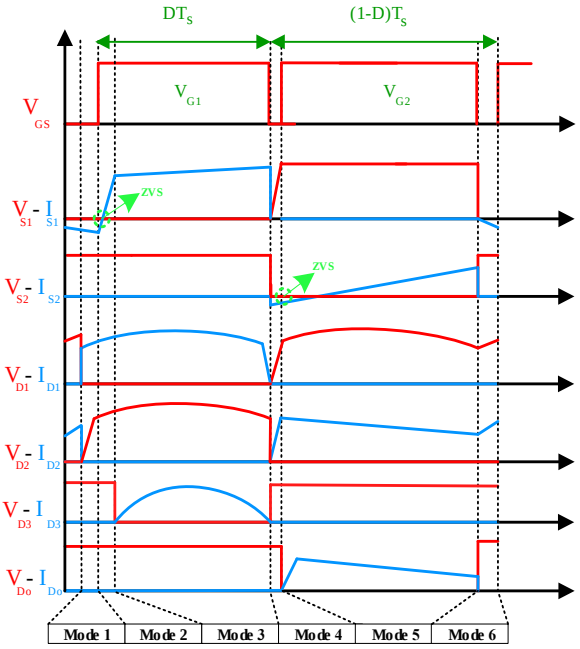


Fig.2. Waveform diagram of the key elements at CCM operating.

E. *Mode 5:*

At the beginning of this situation diode D_2 is turned on and capacitor C_1 is charged through it. Other semiconductors are off except inherent diode of MOSFET S_2. The following equations can be provided using Fig3(e).

$$V_{NS}^{D'} = NV_{lm1}^{D'} = Nk(V_{in} + V_{C1} - V_{C2}) \quad (8)$$

$$V_{nS}^{D'} = nV_{lm2}^{D'} = -nkV_{C1} \quad (9)$$

$$V_O = V_{in} + V_{C1} + V_{C3} - V_{lm1}^{D'} - V_{NS}^{D'} - V_{nS}^{D'} \quad (10)$$

It is important to note that that Y^D indicates the Y value during the MOSFET ON-state time interval.

F. *Mode 6:*

This interval starts when MOSFET S_2 is turned off and output Diode D_o is reverse biased. In this mode the inherent diode of MOSFET S_1 turns on like first mode.

III. ANALYSIS OF THE PRESENT TOPOLOGY

A. $\boldsymbol{Mc}$ ($Voltage\ Gain$) *calculation*

Using the volt-second equilibrium axiom for magnetic inductor (L_{m1}) ((1) and (8)):

$$V_{C2} - V_{C1} = \frac{V_{in}}{D'} \quad (11)$$

Using the volt-second equilibrium axiom for magnetic inductor (L_{m2}) ((3) and (9)):

$$V_{C2} = \frac{V_{C1}}{D} \quad (12)$$

According to (11) and (12):

$$V_{C1} = \frac{DV_{in}}{D'^2} \quad (13)$$

$$V_{C2} = \frac{V_{in}}{D'^2} \quad (14)$$

By substituting (13) and (14) into (7) V_{C3} is obtained:

$$V_{C3} = kV_{in}\left(\frac{ND'^2 - nD + n}{D'^2}\right) \quad (15)$$

By substituting (13) and (14) into (8) $V_{lm1}^{D'}$ and $V_{NS}^{D'}$ are obtained:

$$V_{lm1}^{D'} = kV_{in}\left(\frac{D'^2 + D - 1}{D'^2}\right) \quad (16)$$

$$V_{NS}^{D'} = NkV_{in}\left(\frac{D'^2 + D - 1}{D'^2}\right) \quad (17)$$

By substituting (13) into (9) $V_{nS}^{D'}$ is obtained:

$$V_{nS}^{D'} = -nk\frac{DV_{in}}{D'^2} \quad (18)$$

By substituting (13), (15), (16), (17), and (18) into (10)

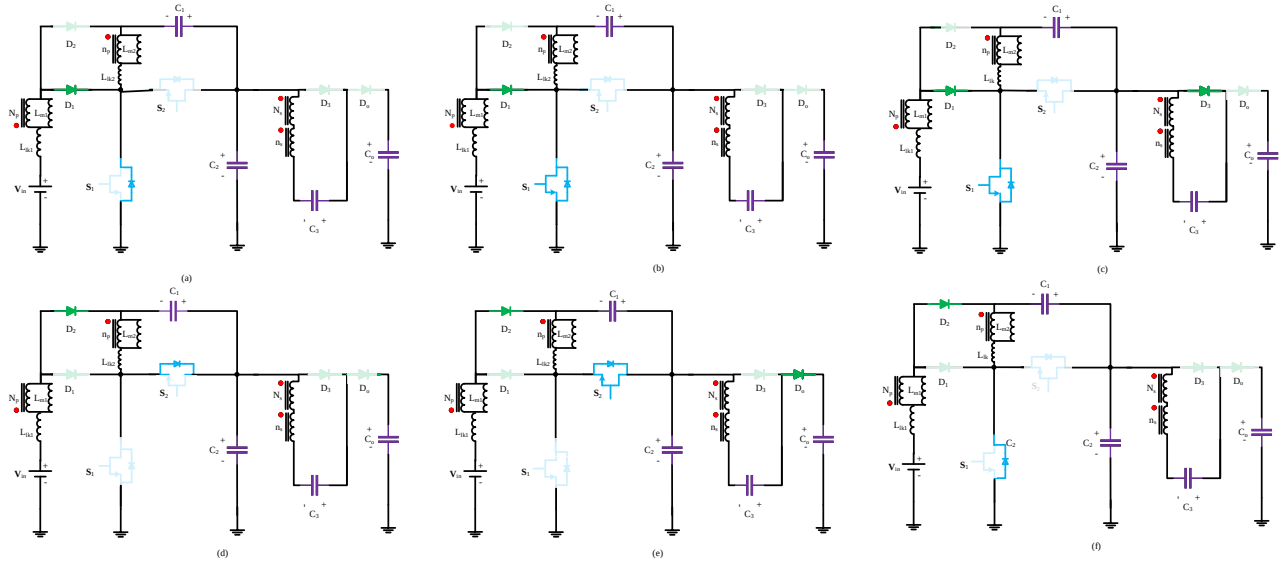


Fig. 3. (a) Current flow path in Mode I, (b) Current flow path in Mode II, (c) Current flow path in Mode III, (d) Current flow path in Mode IV. (e) Current flow path in Mode V, (f) Current flow path in Mode VI.

the nominal gain of proposed topology is obtained:

$$\frac{V_O}{V_{in}} = \frac{D'^2(1-k) + D(1-k-Nk) + Nk + nk + 1}{D'^2} \quad (19)$$

therefore, if the CI leakage inductance is not considered, it means the coupling factor k is around to unity and the recommended topology ideal voltage gain is calculated as follows:

$$\frac{V_O}{V_{in}} = \frac{-ND + N + n + 1}{D'^2} \quad (20)$$

Figure 4 shows Voltage gain of suggested topology in different turns ratio versus duty cycle. As can be found from this figure Using this converter, a very high voltage gain can be obtained with a low turns ratio of CIs.

B. Voltage stress of semiconductors:

The voltage stress of the MOSFETs S_1, S_2 are equal to voltage of capacitor C_2. So, by using (14) the voltage stress of the MOSFETs can be obtained. Also, the voltage stress of diode D_1 is equal to voltage of capacitor C_1 and it can be derived using (13). The voltage stress of diode D_2 can be provided using (13), (14). Finally, the voltage stress of the diodes D_3, D_O can be obtained using (20), (15).

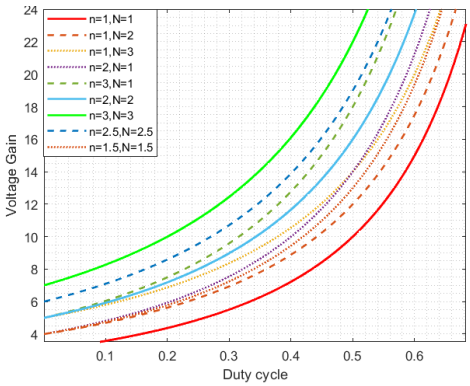


Fig. 4. Voltage gain of suggested topology in different turns ratio versus duty cycle.

$$V_{S1} = V_{S2} = \frac{V_{in}}{D'^2} \quad (21)$$

$$V_{D1} = \frac{DV_{in}}{D'^2} \quad (22)$$

$$V_{D2} = \frac{V_{in}}{D'} \quad (23)$$

$$V_{D3} = V_{DO} = \frac{(-ND + N + n)V_{in}}{D'^2} \quad (24)$$

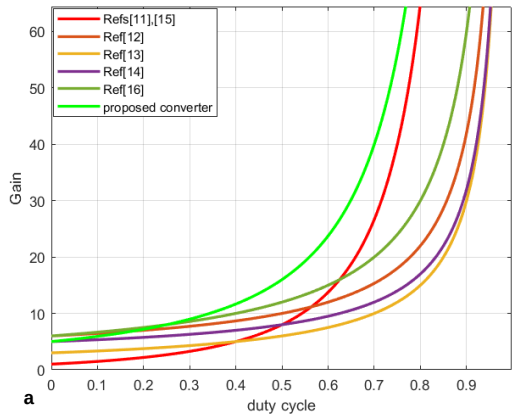
IV. Comparison

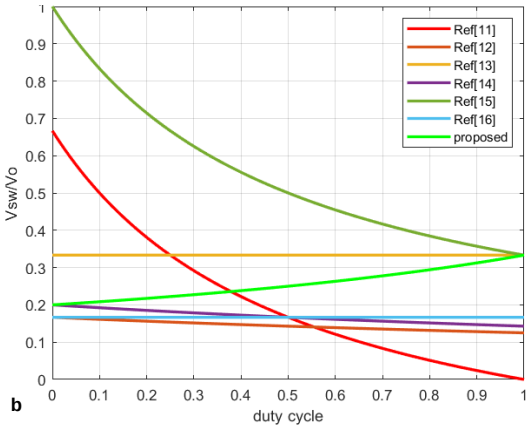
It is practically hard to achieve the optimum results for all design and operating parameters when using power converters. As a result, a trade-off must be established between passive and active elements count, voltage gain, device stresses, and etc. The purpose of this section is to give a balanced comparison between the proposed and other state-of-the-art high step-up dc–dc topologies with CI. Table I shows a comparison between main features of suggested converter and other converters presented in [11-22]. In Fig.

5, some voltage gain, voltage stress on switch and output diode comparisons are expressed. In Fig. 5(a), In respect to duty cycle, the suggested topology has the greatest voltage gain among opponents. The voltage gain of suggested topology is more than 13.5 when duty cycle is around 0.45. This is an appropriate voltage gain in many applications like solar systems. The normalized voltage stress across the MOSFET (V_S/V_o) vs the duty cycle of the MOSFET is depicted in Fig. 5(b). As shown in the figure, the normalized voltage stress of the main switch is lower than 0.35 for every duty cycle values. The normalized voltage stress across the output diodes (V_{Do}/V_o) is shown in Fig. 5(c).The normalized voltage stress on output diode is about 0.75 when duty cycle value is 0.45 in suggested topology. These figure shows that the voltage stress across the power diodes of the proposed converter is within an appropriate limit (lower than 0.8 for every duty cycle values). As a result, by using low voltage rate devices in the suggested converter, it is feasible to reduce conduction losses and costs.

Table I. APTITUDE COMPARISON WITH OTHER CI-based TOPOLOGIES

Ref.	Voltage Gain	Normalized Maximum voltage Stress on switches	Normalized Maximum voltage Stress on diode	Number of				
				CI + I	S	D	C	T
[11]	$\frac{1+nD}{(1-D)^2}$	$\frac{n(1-D)}{(1+n)(1+nD)}$	$\frac{(1+n)(1+nD)-n(1-D)}{(1+n)(1+nD)}$	1+2	1	6	4	14
[12]	$\frac{2+2n-nD}{1-D}$	$\frac{1}{2+2n+nD}$	$\frac{1+n}{2+2n+nD}$	1	1	4	3	9
[13]	$\frac{1+n}{1-D}$	$\frac{1}{1+n}$	$\frac{D}{1+n}$	1	2	2	3	8
[14]	$\frac{1+2n-nD}{1-D}$	$\frac{1}{1+2n+nD}$	$\frac{n}{1+2n+nD}$	1	1	4	4	10
[15]	$\frac{1+nD}{(1-D)^2}$	$\frac{1}{1+nD}$	$\frac{n}{1+nD}$	1+1	1	4	3	10
[16]	$\frac{2(1+n)}{1-D}$	$\frac{1}{2(1+n)}$	0.5	1	2	4	5	12
Proposed Topology	$\frac{-ND+N+n+1}{(1-D)(1-D)}$	$\frac{1}{-ND+N+n+1}$	$\frac{-ND+N+n}{-ND+N+n+1}$	2	2	4	4	12





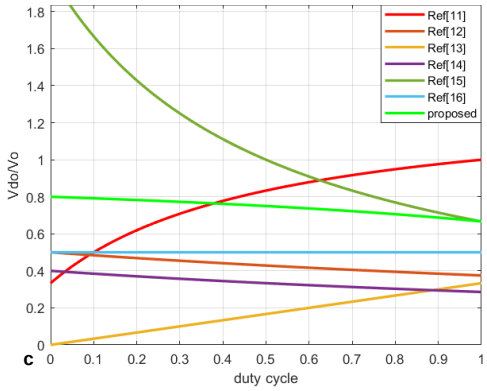


Fig. 5.a) Comparison of voltage gain changes of various converters versus duty ratio D b) comparison Normalized voltage stress of master MOSFET against duty cycle in different topologies. c) comparison Normalized voltage stress of output diode against duty cycle in various topologies.

V. Experimental Results

In this part, a 200 W lab model of the suggested converter is developed to demonstrate the parametric study. Table II displays the characteristics of several elements in this laboratory model. Figure 6 depicts a picture of the laboratory prototype and its components.

The experimental findings are shown in Figs7(a-j) at 200 W output power and 45% duty cycle. Figs. 6(a) show the gate pulse of the MOSFET S_1, S_2 in three forms. In three cases, they show that all these images are conceptually the same and there is a zoom level in them or a waveform shift for better understanding. Fig .6(b) shows the voltage and current of the main MOSFET S_1. This figure can validate the theoretical analysis in (21) and the voltage stress of this MOSFET is around 84V. The same is true for the second MOSFET S_2, whose voltage and current are shown in Figure 7(c). It's

important to note that these two MOSFETs have a ZVS operation in turning on state. So, the switching losses is minimized for these two MOSFETs.

Fig. 7(d) illustrates the voltage and current waveforms of the diode D_1. The voltage stress on this diode is about 41V and this figure can validate the theoretical analysis in (22). Fig. 7(e) depicts the voltage and current waveforms of the second diode D_2 and verify equation (23). The voltage and current of diode D_3 are depicted in Fig. 7(f). This diode has a ZCS functioning in turning on and off. So, the reverse recovery issue is solved. The voltage and current of output diode are demonstrated in Fig. 7(g). This figure can verify (24). The current of leakage inductances are depicted in figs7(h, i).

Fig. 7(j) demonstrates the load and source voltage at 200 W output power. This figure shows that the output voltage ripple is very low.

Table II. specifications of Suggested topology

Parameters	Description/ Value
Switch	
S_1, S_2	HY3912 MOSFET 6.3 mΩ on-resistance
Diodes	
D_1, D_2	STPS4045C
D_3, D_O	SF1006
Magnetic coupled Inductor 1,2	Turns ratio: 2 (N_1:N_2=20:40) Core: PC47ETD44-Z ferrite core Magnetizing inductance: 130 μH With PSPS winding Leakage inductance: 1 μH
Capacitors	
C_1, C_2	10 μF, 100 V (MKT)
C_3	10 μF, 250 V (MKT)
C_O	68 μF, 400 V
Switching Frequency	50 KHz
Output Power	200 W
Input Voltage	20 V
Nominal Gain	13.5

It is important to note that PSPS term in Table II stands for windings sequence and it mean that the half of the primary winding is twisted firstly and then half of the secondary is twisted. After that the rest of primary winding is twisted and in the last, the rest of secondary winding is twisted. This sequence is considered for decreasing the leakage inductance.

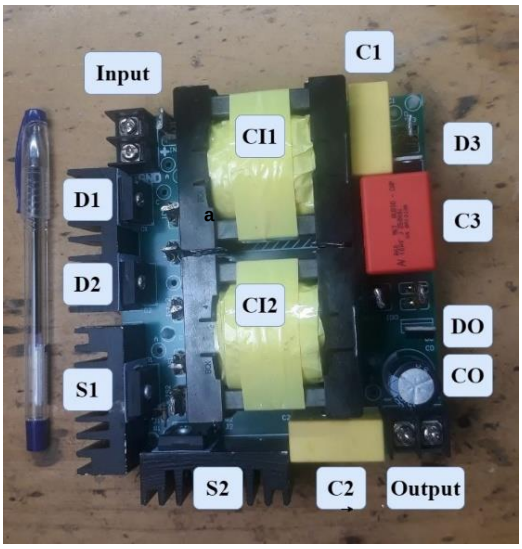
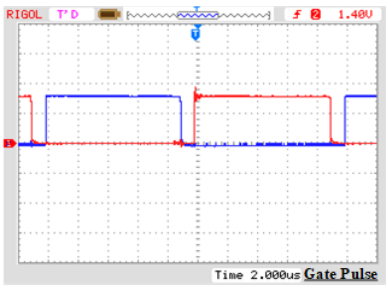
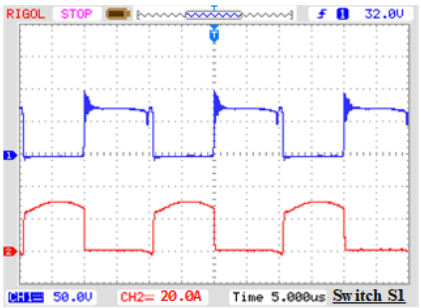


Fig. 6. Experimental setup of the suggested topology.



A



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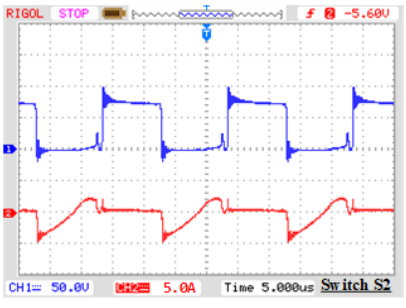

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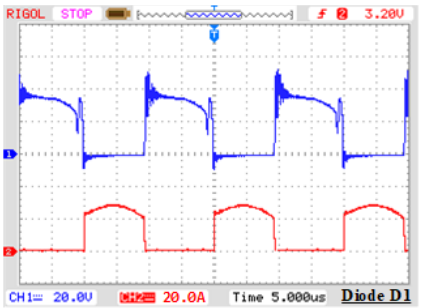

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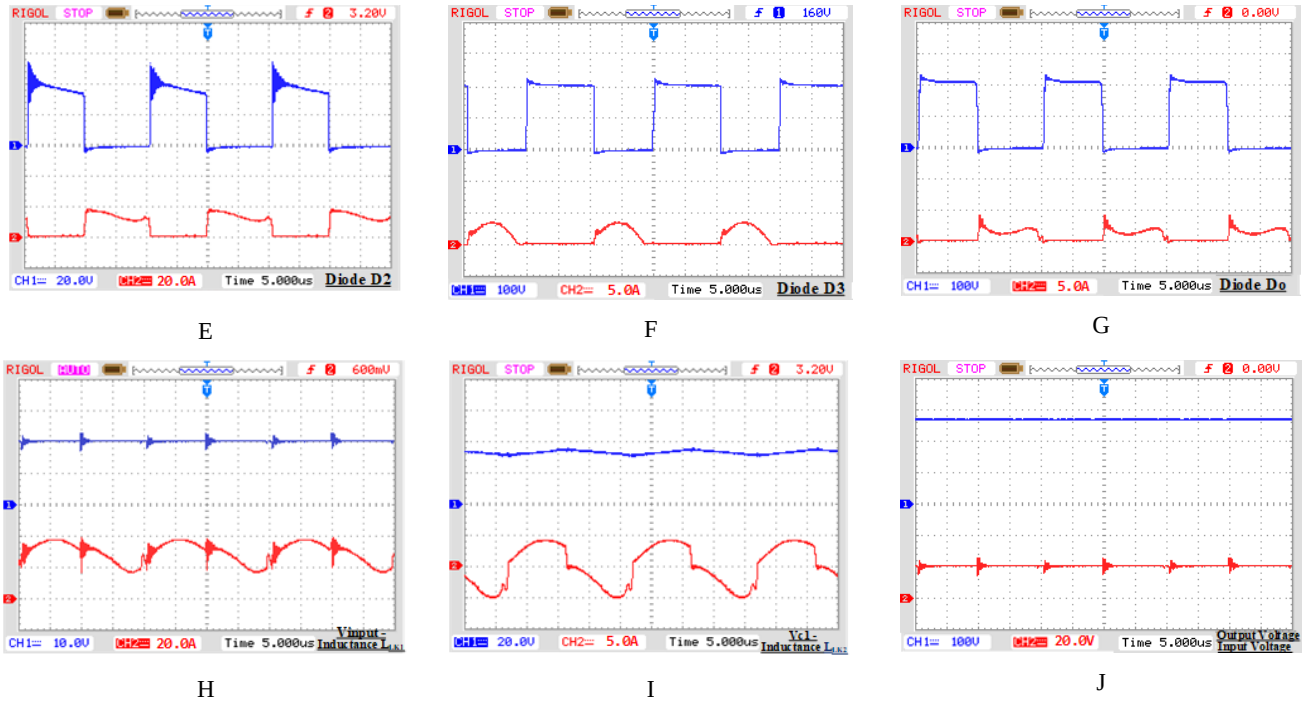

Fig. 7. Experimental Waveforms (a)Gate Pulse (b)Switch S_1 (c) Switch S_2 (d) voltage and current of diode D_1 (e) voltage and current of diode D_2 (f) voltage and current of diode D_3 (g) voltage and current of diode D_o (h)Input voltage and current of Leakage inductance L_{lk1} (i) voltage C_1 and current of Leakage inductance L_{lk2} (j) Input and Output Voltage

VI. CONCLUSION

This work introduces a high step-up DC-DC topology with soft-switching functionality. A thorough examination of several operational modes, voltage stress of various components, and comparison with other topology for the proposed converter are provided. A 200 W prototype with a system efficiency of 93 percent is available. Furthermore, this design may be used to other applications such as solar modules and fuel cells, where greater voltage conversion ratios can be accomplished without increasing stresses and element count, and topology efficiency will be hopeful due to soft switching operation of MOSFETs and diodes.

The proposed converter was compared with similar converters and the soft switching operation of both switches and higher voltage gain are the most important strengths of this converter.

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