

## Guest Editorial: Implementation Issues in System-on-Chip

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We are delighted to present this special issue of the Journal of Signal Processing Systems on Implementation Issues in System-on-Chip.

During the past two decades, System-on-Chip (SoC) has grown from a futuristic idea to a stabilized mainstream paradigm for electronic system design and implementation. However, it keeps posing challenges to the designers and researchers on multiple levels and in multiple disciplines. The aim of this special issue is to provide samples on quality research targeting to solve implementation issues and investigate design case studies from different points of view in SoC design. The issues addressed include power efficiency, complexity management and security in embedded integrated systems.

This issue consists of seven papers that are briefly discussed as follows:

The first article, by Ferial Ben Abdallah, Chiraz Trabelsi, Rabie Ben Atitallah, and Mourad Abed on “Model-Driven Approach for Early Power-Aware Design Space Exploration of Embedded Systems” discusses a model-driven engineering approach for SoC design-space exploration. In “Power Mitigation by Performance Equalization in a Heterogeneous Reconfigurable Multicore Architecture” by M. Waqar Hussain, Henry Hoffmann, Tapani Ahonen and Jari Nurmi, the authors present a self-aware heterogeneous architecture for dynamically managing power and energy consumption of the computing platform. Martin Broich and Tobias G. Noll tackle energy efficiency and design complexity of communications SoCs in their paper “Optimal Datapath Widths within Turbo and Viterbi Decoders for High Area- and Energy-Efficiency.”

In the article “A Customized Many-Core Hardware Acceleration Platform for Short Read Mapping Problems Using Distributed Memory Interface with 3D-stacked Architecture,” the authors Pei Liu, Ahmed Hemani, Kolin Paul, Christian Weis, Mattias Jung and Norbert When apply advanced architecture and implementation techniques to a DNA sequencing problem. Essentially, it is an approach to improve the performance of hash-index based short read mapping algorithm using a hardware acceleration platform. The paper “Design of a Residue Number System Based Linear System Solver in Hardware” by Jiri Bucek, Pavel Kubalik, Robert Lorencz and Tomas Zahradnicky is focused on error-free solution of dense linear systems using residual arithmetic in hardware. Their implementation is useful for solving large nonsingular systems of linear equations with integer, rational or floating-point coefficients with arbitrary precision.

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Christoforos Kachris, Dionysios Diamantopoulos, Georgios Syrakoulis and Dimitrios Soudris present an energy-efficient scheme for MapReduce that is a programming framework for distributed systems that is used for automatically parallelizing and scheduling the tasks to distributed resources, in their paper “An FPGA-based Integrated MapReduce Accelerator Platform.” And finally, security issues are addressed by Elena Dubrova, Mats Näslund, Gunnar Carlsson, John Fornehed and Ben Smeets in the paper “Two Countermeasures Against Hardware Trojans Exploiting Non-Zero Aliasing Probability of BIST.”

The special issue was preceded by the International Symposium on System-on-Chip, held in Tampere, Finland in October 2014. The articles, hand-picked among the top contributions in the symposium, have been substantially extended and thereafter undergone two rounds of rigorous peer-review according to the journal’s high standards. We would like to thank all the reviewers involved for their invaluable input, and to express our appreciation to the authors for their contributions.

We sincerely hope that you enjoy this special issue and can find useful takeaways for your own future research.

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